

14-Stage Binary Ripple Counter With Oscillator

High-Performance Silicon-Gate CMOS

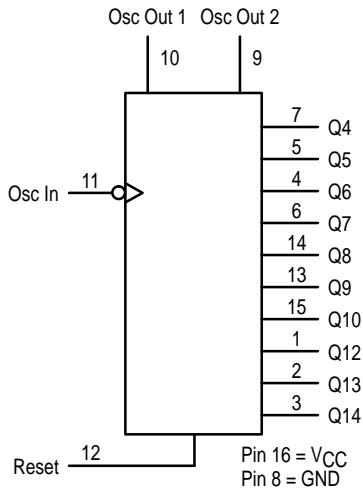
The MC54/74C4060A is identical in pinout to the standard CMOS MC14060B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master-slave flip-flops and an oscillator with a frequency that is controlled either by a crystal or by an RC circuit connected externally. The output of each flip-flop feeds the next and the frequency at each output is half of that of the preceding one. The state of the counter advances on the negative-going edge of the Osc In. The active-high Reset is asynchronous and disables the oscillator to allow very low power consumption during stand-by operation.

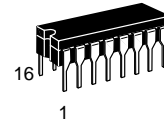
State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with Osc Out 2 of the HC4060A.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 390 FETs or 97.5 Equivalent Gates

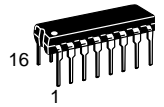
LOGIC DIAGRAM



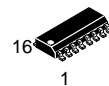
MC54/74HC4060A



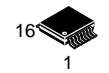
J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



D SUFFIX
SOIC PACKAGE
CASE 751B-05



DT SUFFIX
TSSOP PACKAGE
CASE 748C-03

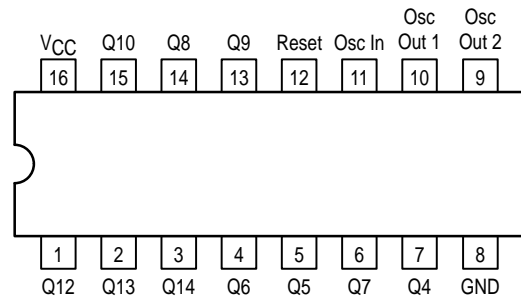
ORDERING INFORMATION

| | |
|---------------|---------|
| MC54HCXXXXAJ | Ceramic |
| MC74HCXXXXAN | Plastic |
| MC74HCXXXXAD | SOIC |
| MC74HCXXXXADT | TSSOP |

FUNCTION TABLE

| Clock | Reset | Output State |
|-------|-------|-----------------------|
| | L | No Change |
| | L | Advance to Next State |
| X | H | All Outputs Are Low |

Pinout: 16-Lead Plastic Package (Top View)



MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|--------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | - 0.5 to + 7.0 | V |
| V _{in} | DC Input Voltage (Referenced to GND) | - 0.5 to V _{CC} + 0.5 | V |
| V _{out} | DC Output Voltage (Referenced to GND) | - 0.5 to V _{CC} + 0.5 | V |
| I _{in} | DC Input Current, per Pin | ± 20 | mA |
| I _{out} | DC Output Current, per Pin | ± 25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ± 50 | mA |
| P _D | Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package† | 750 500 450 | mW |
| T _{stg} | Storage Temperature Range | - 65 to + 150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package Ceramic DIP | 260 300 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
Ceramic DIP: - 10 mW/°C from 100° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | |
|------------------------------------|--|---|-----------------|--------------------|----|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.5* | 6.0 | V | |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V | |
| T _A | Operating Temperature Range, All Package Types | - 55 | + 125 | °C | |
| t _r , t _f | Input Rise/Fall Time (Figure 1) | V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V | 0 0 0 | 1000 500 400 | ns |

* The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 11 with an external clock source.

DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|---|---|----------------------|------------------|-------|--------|------|
| | | | | -55 to 25°C | ≤85°C | ≤125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20µA | 2.0 | 1.50 | 1.50 | 1.50 | V |
| | | | 3.0 | 2.10 | 2.10 | 2.10 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.20 | 4.20 | 4.20 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20µA | 2.0 | 0.50 | 0.50 | 0.50 | V |
| | | | 3.0 | 0.90 | 0.90 | 0.90 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.80 | 1.80 | 1.80 | |
| V _{OH} | Minimum High-Level Output Voltage (Q4-Q10, Q12-Q14) | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20µA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4mA I _{out} ≤ 4.0mA I _{out} ≤ 5.2mA | 3.0 | 2.48 | 2.34 | 2.20 | |
| | | | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | | 6.0 | 5.48 | 5.34 | 5.20 | |

DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|-------|--------|------|
| | | | | -55 to 25°C | ≤85°C | ≤125°C | |
| V _{OL} | Maximum Low-Level Output Voltage (Q4–Q10, Q12–Q14) | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4mA I _{out} ≤ 4.0mA I _{out} ≤ 5.2mA | 3.0 | 0.26 | 0.33 | 0.40 | |
| | | | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | | 6.0 | 0.26 | 0.33 | 0.40 | |
| V _{OH} | Minimum High-Level Output Voltage (Osc Out 1, Osc Out 2) | V _{in} = V _{CC} or GND I _{out} ≤ 20μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{in} = V _{CC} or GND I _{out} ≤ 0.7mA I _{out} ≤ 1.0mA I _{out} ≤ 1.3mA | 3.0 | 2.48 | 2.34 | 2.20 | |
| | | | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | | 6.0 | 5.48 | 5.34 | 5.20 | |
| V _{OL} | Maximum Low-Level Output Voltage (Osc Out 1, Osc Out 2) | V _{in} = V _{CC} or GND I _{out} ≤ 20μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{in} = V _{CC} or GND I _{out} ≤ 0.7mA I _{out} ≤ 1.0mA I _{out} ≤ 1.3mA | 3.0 | 0.26 | 0.33 | 0.40 | |
| | | | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | | 6.0 | 0.26 | 0.33 | 0.40 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0μA | 6.0 | 4 | 40 | 160 | μA |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|--|----------------------|------------------|-------|--------|------|
| | | | -55 to 25°C | ≤85°C | ≤125°C | |
| f _{max} | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4) | 2.0 | 6.0 | 9.0 | 8.0 | MHz |
| | | 3.0 | 10 | 14 | 12 | |
| | | 4.5 | 30 | 28 | 25 | |
| | | 6.0 | 50 | 45 | 40 | |
| | | | | | | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Osc In to Q4* (Figures 1 and 4) | 2.0 | 300 | 375 | 450 | ns |
| | | 3.0 | 180 | 200 | 250 | |
| | | 4.5 | 60 | 75 | 90 | |
| | | 6.0 | 51 | 64 | 75 | |
| | | | | | | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Osc In to Q14* (Figures 1 and 4) | 2.0 | 500 | 750 | 1000 | ns |
| | | 3.0 | 350 | 450 | 600 | |
| | | 4.5 | 250 | 275 | 300 | |
| | | 6.0 | 200 | 220 | 250 | |
| | | | | | | |
| t _{PHL} | Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4) | 2.0 | 195 | 245 | 300 | ns |
| | | 3.0 | 75 | 100 | 125 | |
| | | 4.5 | 39 | 49 | 61 | |
| | | 6.0 | 33 | 42 | 53 | |
| | | | | | | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Q _n to Q _{n+1} (Figures 3 and 4) | 2.0 | 75 | 95 | 125 | ns |
| | | 3.0 | 60 | 75 | 95 | |
| | | 4.5 | 15 | 19 | 24 | |
| | | 6.0 | 13 | 16 | 20 | |
| | | | | | | |

AC CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns) – **continued**

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|---|----------------------|------------------|-------|--------|------|
| | | | –55 to 25°C | ≤85°C | ≤125°C | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 27 | 32 | 36 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| C _{in} | Maximum Input Capacitance | | 10 | 10 | 10 | pF |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

* For T_A = 25°C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$$V_{CC} = 2.0 \text{ V: } t_p = [93.7 + 59.3 (n-1)] \text{ ns}$$

$$V_{CC} = 4.5 \text{ V: } t_p = [30.25 + 14.6 (n-1)] \text{ ns}$$

$$V_{CC} = 3.0 \text{ V: } t_p = [61.5 + 34.4 (n-1)] \text{ ns}$$

$$V_{CC} = 6.0 \text{ V: } t_p = [24.4 + 12 (n-1)] \text{ ns}$$

| CPD | Power Dissipation Capacitance (Per Package)* | Typical @ 25°C, V _{CC} = 5.0 V | | pF |
|-----|--|---|--|----|
| | | 35 | | |
| | | | | |

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|---------------------------------|--|----------------------|------------------|-------|--------|------|
| | | | –55 to 25°C | ≤85°C | ≤125°C | |
| t _{rec} | Minimum Recovery Time, Reset Inactive to Clock (Figure 2) | 2.0 | 100 | 125 | 150 | ns |
| | | 3.0 | 75 | 100 | 120 | |
| | | 4.5 | 20 | 25 | 30 | |
| | | 6.0 | 17 | 21 | 25 | |
| t _w | Minimum Pulse Width, Clock (Figure 1) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 27 | 32 | 36 | |
| | | 4.5 | 15 | 19 | 23 | |
| | | 6.0 | 13 | 16 | 19 | |
| t _w | Minimum Pulse Width, Reset (Figure 2) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 27 | 32 | 36 | |
| | | 4.5 | 15 | 19 | 23 | |
| | | 6.0 | 13 | 16 | 19 | |
| t _r , t _f | Maximum Input Rise and Fall Times (Figure 1) | 2.0 | 1000 | 1000 | 1000 | ns |
| | | 3.0 | 800 | 800 | 800 | |
| | | 4.5 | 500 | 500 | 500 | |
| | | 6.0 | 400 | 400 | 400 | |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

Osc In (Pin 11)

Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter. Osc In may be driven by an external clock source.

Reset (Pin 12)

Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

OUTPUTS

Q4—Q10, Q12—Q14 (Pins 7, 5, 4, 6, 13, 15, 1, 2, 3)

Active-high outputs. Each Q_n output divides the Clock input frequency by 2^N. The user should note the Q1, Q2, Q3 and Q11 are not available as outputs.

Osc Out 1, Osc Out 2 (Pins 9, 10)

Oscillator outputs. These pins are used in conjunction with Osc In and the external components to form an oscillator (See NO TAG and NO TAG). When Osc In is being driven with an external clock source, Osc Out 1 and Osc Out 2 must be left open circuited. With the crystal oscillator configuration in Figure 6, Osc Out 2 must be left open circuited.

SWITCHING WAVEFORMS

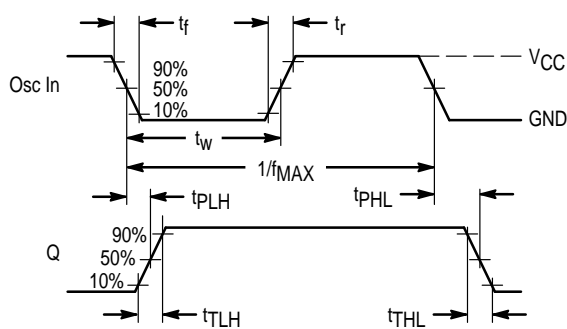


Figure 1.

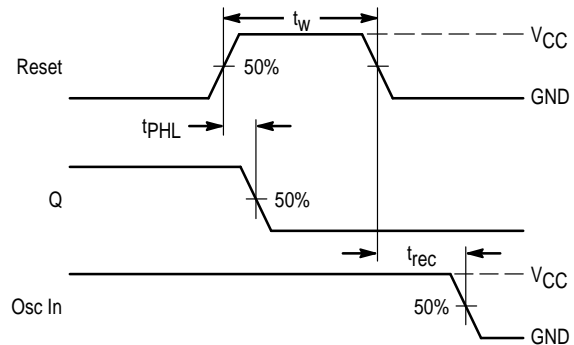


Figure 2.

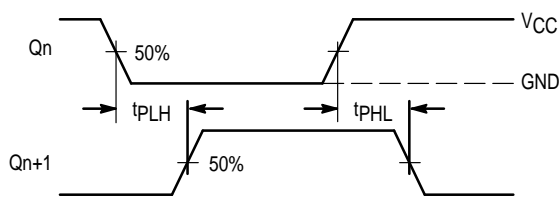
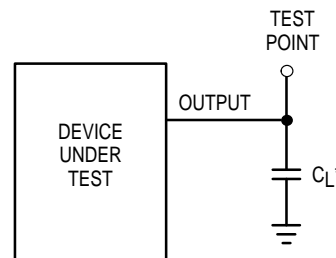


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

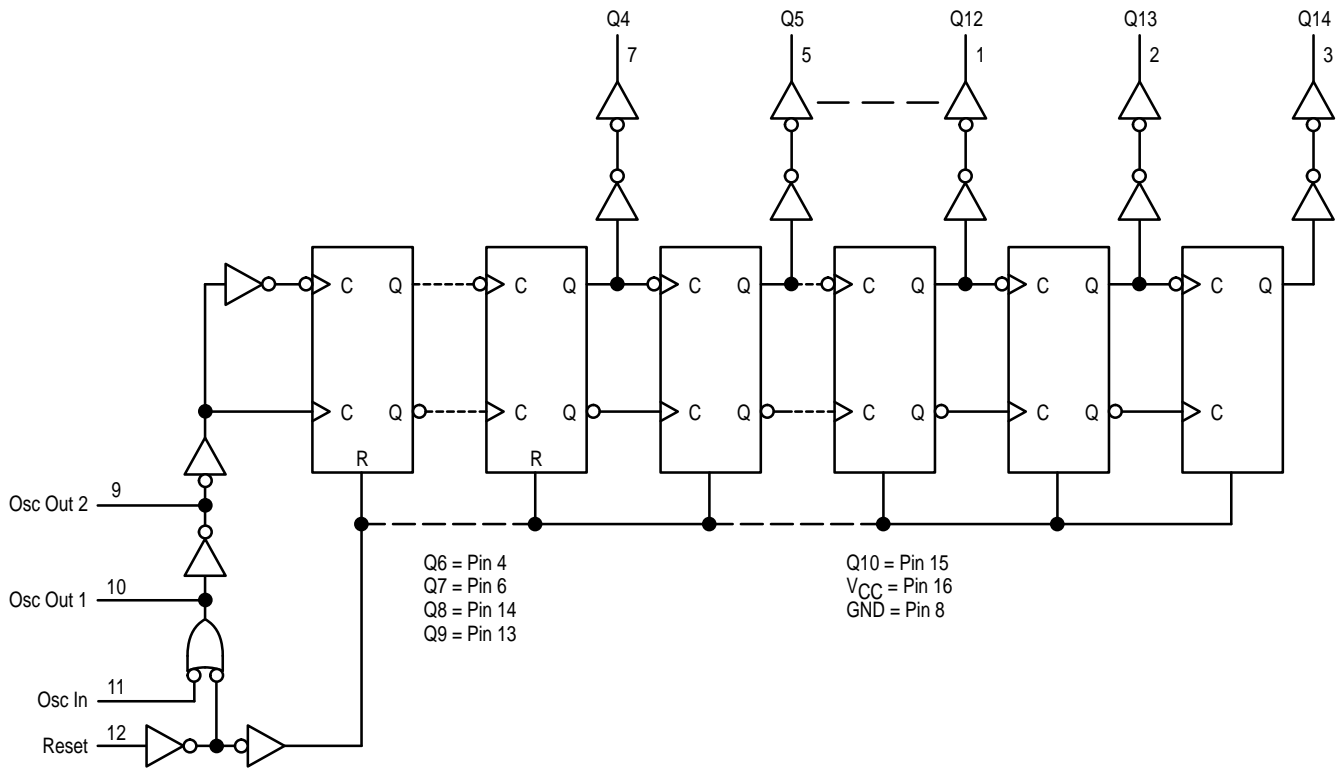


Figure 5. Expanded Logic Diagram

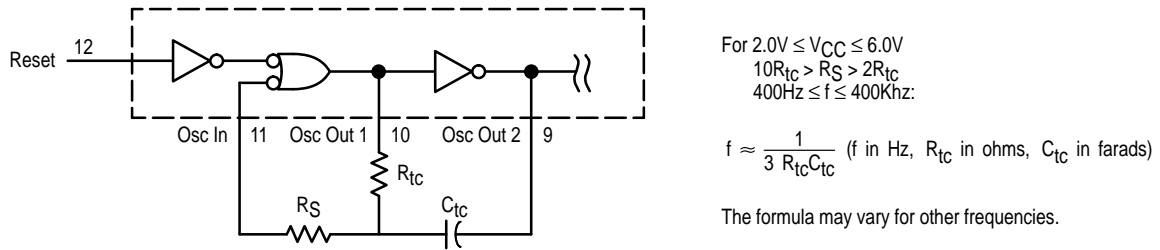


Figure 6. Oscillator Circuit Using RC Configuration

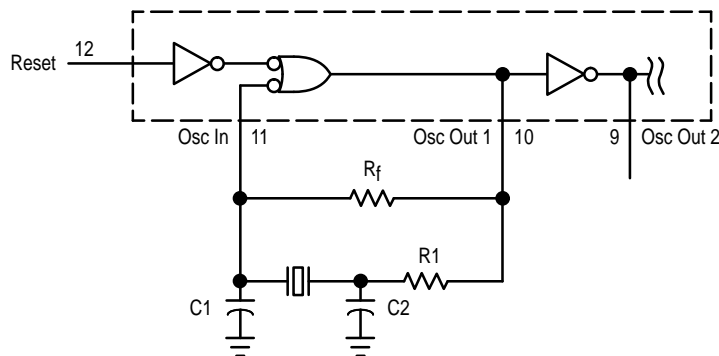
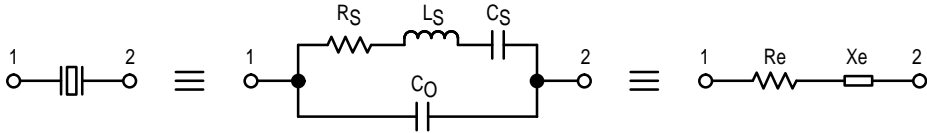


Figure 7. Pierce Crystal Oscillator Circuit

TABLE 1. CRYSTAL OSCILLATOR AMPLIFIER SPECIFICATIONS ($T_A = 25^\circ\text{C}$; Input = Pin 11, Output = Pin 10)

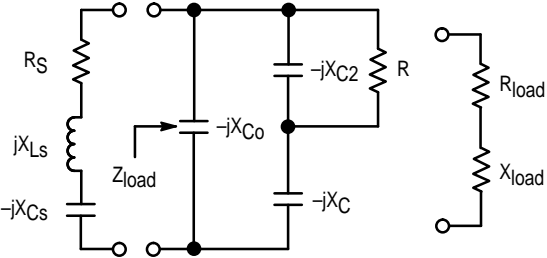
| Type | Positive Reactance (Pierce) | |
|--|-----------------------------|----------------------|
| Input Resistance, R_{in} | 60M Ω Minimum | |
| Output Impedance, Z_{out} (4.5V Supply) | 200 Ω (See Text) | |
| Input Capacitance, C_{in} | 5pF Typical | |
| Output Capacitance, C_{out} | 7pF Typical | |
| Series Capacitance, C_a | 5pF Typical | |
| Open Loop Voltage Gain with Output at Full Swing, α | 3Vdc Supply | 5.0 Expected Minimum |
| | 4Vdc Supply | 4.0 Expected Minimum |
| | 5Vdc Supply | 3.3 Expected Minimum |
| | 6Vdc Supply | 3.1 Expected Minimum |

PIERCE CRYSTAL OSCILLATOR DESIGN



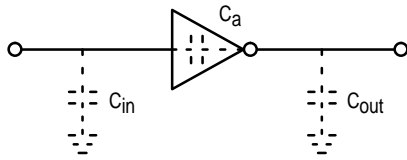
Value are supplied by crystal manufacturer (parallel resonant crystal).

Figure 8. Equivalent Crystal Networks



NOTE: $C = C_1 + C_{in}$ and $R = R_1 + R_{out}$. C_0 is considered as part of the load. C_a and R_f typically have minimal effect below 2MHz.

Figure 9. Series Equivalent Crystal Load



Values are listed in Table 1.

Figure 10. Parasitic Capacitances of the Amplifier

DESIGN PROCEDURES

The following procedure applies for oscillators operating below 2MHz where Z is a resistor R1. Above 2MHz, additional impedance elements should be considered: C_{out} and C_a of the amp, feedback resistor R_f , and amplifier phase shift error from 180°C.

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_e = \frac{-jX_{C_0}(R_s + jX_{L_s} - jX_{C_s})}{-jX_{C_0} + R_s + jX_{L_s} - jX_{C_s}} = R_e + jX_e$$

Reactance jX_e should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum R_s for the crystal should be used in the equation.

Step 2: Determine β , the attenuation, of the feedback network. For a closed-loop gain of 2, $A_V\beta = 2, \beta = 2/A_V$ where A_V is the gain of the HC4060A amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: A manufacturer may specify an external load capacitance of 32pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate R_{load} . For example, a manufacturer specifies a crystal Q of 100,000. In-circuit Q is arbitrarily set at 20% below crystal Q or 80,000. Then $R_{load} = (2\pi f_0 L_s / Q) - R_s$ where L_s and R_s are crystal parameters.

Step 5: Simultaneously solve, using a computer,

$$\beta = \frac{X_C \cdot X_{C2}}{R \cdot R_e + X_{C2} (X_e - X_C)} \quad (\text{with feedback phase shift} = 180^\circ) \quad (\text{Eq 1})$$

$$X_e = X_{C2} + X_C + \frac{R_e X_{C2}}{R} = X_{load} \quad (\text{where the loading capacitor is an external load, not including } C_0) \quad (\text{Eq 2})$$

$$R_{load} = \frac{R X_{C_0} X_{C2} [(X_C + X_{C2})(X_C + X_{C_0}) - X_C(X_C + X_{C_0} + X_{C2})]}{X_{C2}^2 (X_C + X_{C_0})^2 + R^2 (X_C + X_{C_0} + X_{C2})^2} \quad (\text{Eq 3})$$

Here $R = R_{out} + R1$. R_{out} is amp output resistance, R1 is Z. The C corresponding to X_C is given by $C = C1 + C_{in}$.

Alternately, pick a value for R1 (i.e, let $R1 = R_s$). Solve Equations 1 and 2 for C1 and C2. Use Equation 3 and the fact that $Q = 2\pi f_0 L_s / (R_s + R_{load})$ to find in-circuit Q. If Q is not satisfactory pick another value for R1 and repeat the procedure.

CHOOSING R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at Osc Out 2 (Pin 9). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

SELECTING R_f

The feedback resistor, R_f , typically ranges up to 20M Ω . R_f determines the gain and bandwidth of the amplifier. Proper bandwidth insures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as

the first overtone. R_f must be large enough so as to not affect the phase of the feedback network in an appreciable manner.

ACKNOWLEDGEMENTS AND RECOMMENDED REFERENCES

The following publications were used in preparing this data sheet and are hereby acknowledged and recommended for reading:

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

ALSO RECOMMENDED FOR READING:

E. Hafner, "The Piezoelectric Crystal Unit-Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", Electro-Technology, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

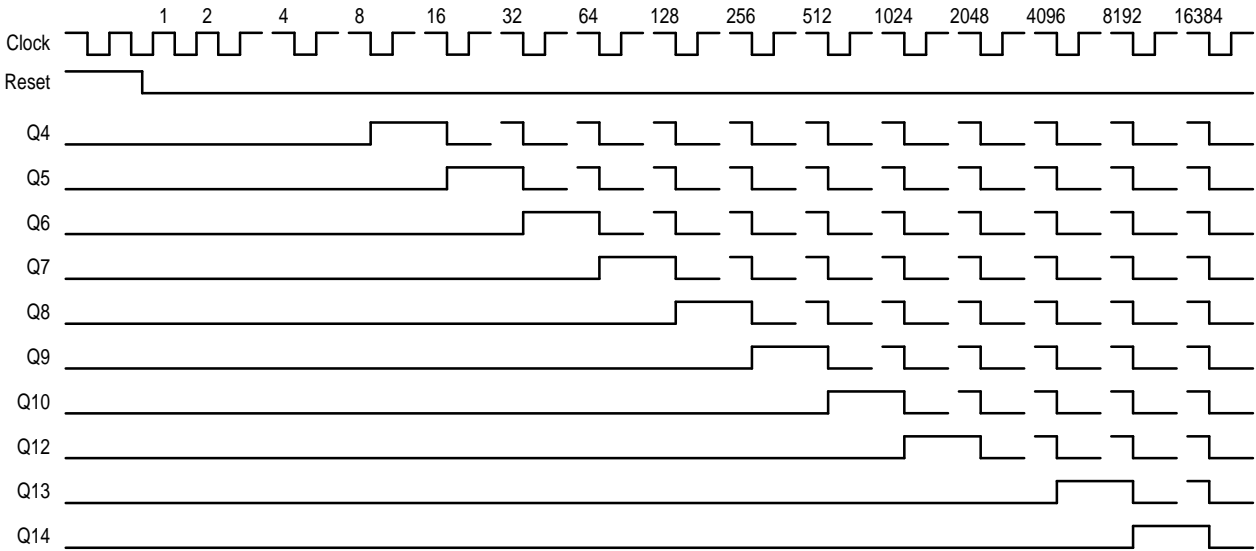
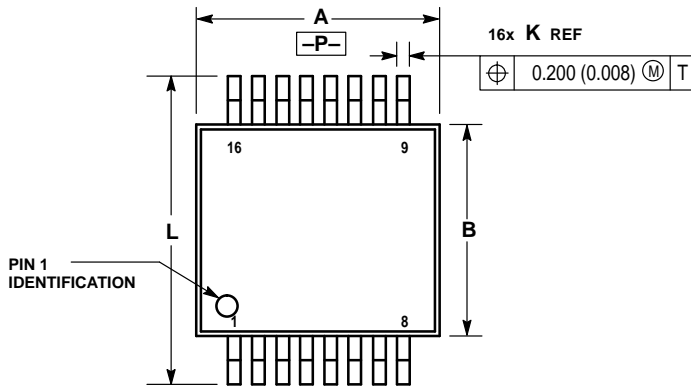


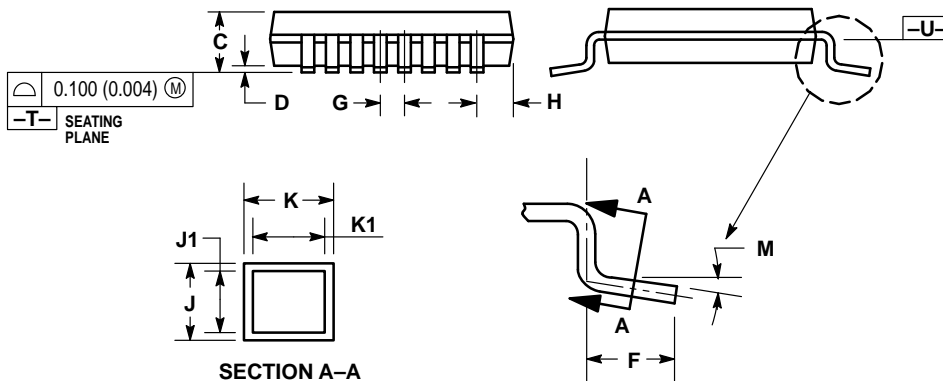
Figure 11. Timing Diagram

OUTLINE DIMENSIONS

DT SUFFIX
TSSOP PACKAGE
CASE 948C-03
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -U-.



| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | — | 5.10 | — | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | — | 1.20 | — | 0.047 |
| D | 0.05 | 0.25 | 0.002 | 0.010 |
| F | 0.45 | 0.55 | 0.018 | 0.022 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.22 | 0.23 | 0.009 | 0.010 |
| J | 0.09 | 0.24 | 0.004 | 0.009 |
| J1 | 0.09 | 0.18 | 0.004 | 0.007 |
| K | 0.16 | 0.32 | 0.006 | 0.013 |
| K1 | 0.16 | 0.26 | 0.006 | 0.010 |
| L | 6.30 | 6.50 | 0.248 | 0.256 |
| M | 0° | 10° | 0° | 10° |

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