MOTOROLA

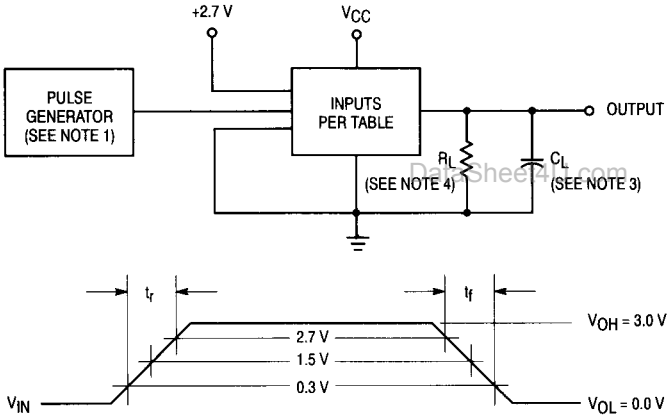
Synchronous 4-Bit Decade Counter (Asynchronous Master Reset)

ELECTRICALLY TESTED PER:
MIL-M-38510/34301

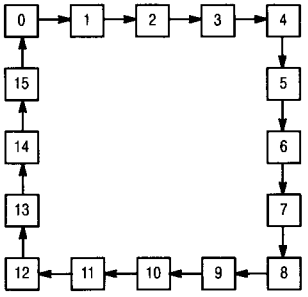
The 54F161A is a high-speed synchronous modulo-16 binary counter. It is synchronously presettable for application in programmable dividers and has two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The F161A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Frequency of 120 MHz

TEST CIRCUIT AND WAVEFORMS



STATE DIAGRAM



REFERENCE NOTES ON PAGE 4-76

Military 54F161A

MPO

AVAILABLE AS:

1) JAN: JM38510/34301BXA
2) SMD: N/A
3) 883: 54F161A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{MR}$	1	1	2	GND
CP	2	2	3	V_{CC}
P_0	3	3	4	V_{CC}
P_1	4	4	5	V_{CC}
P_2	5	5	7	V_{CC}
P_3	6	6	8	V_{CC}
CEP	7	7	9	V_{CC}
GND	8	8	10	GND
$\overline{PE}$	9	9	12	V_{CC}
CET	10	10	13	V_{CC}
Q_3	11	11	14	OPEN
Q_2	12	12	15	OPEN
Q_1	13	13	17	OPEN
Q_0	14	14	18	OPEN
TC	15	15	19	OPEN
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

$\overline{MR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n - Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Charge (Hold)
H	H	X	L	No Charge (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

FUNCTIONAL DESCRIPTION

The 54F161A can count modulo-16 binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, (synchronous reset for F163A), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{MR}$, F161A), Synchronous Reset ($\overline{SR}$, F163A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (F161A) or $\overline{SR}$ (F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

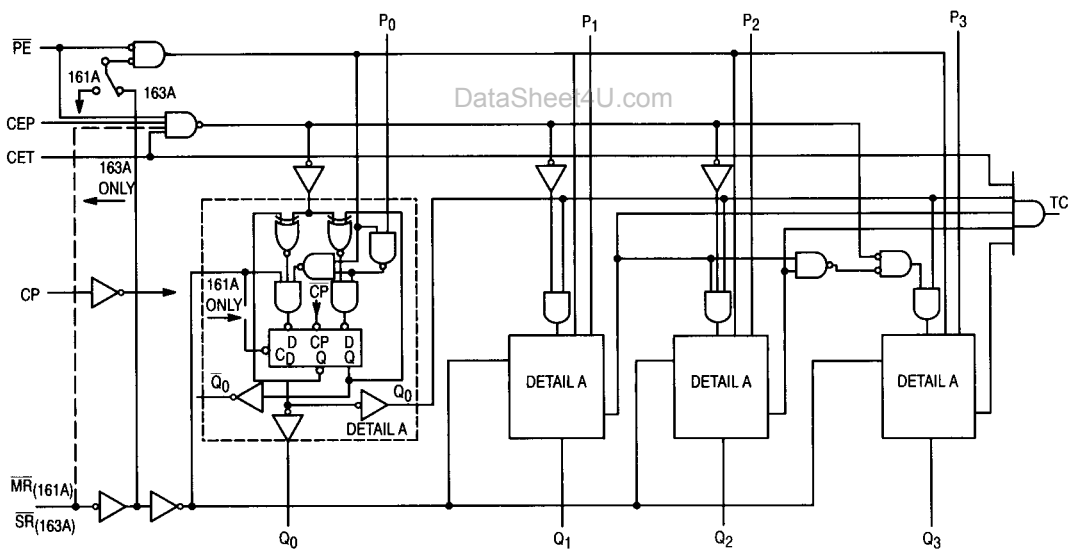
The 54F161A and 54F163A use D-type edge triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

LOGIC DIAGRAM



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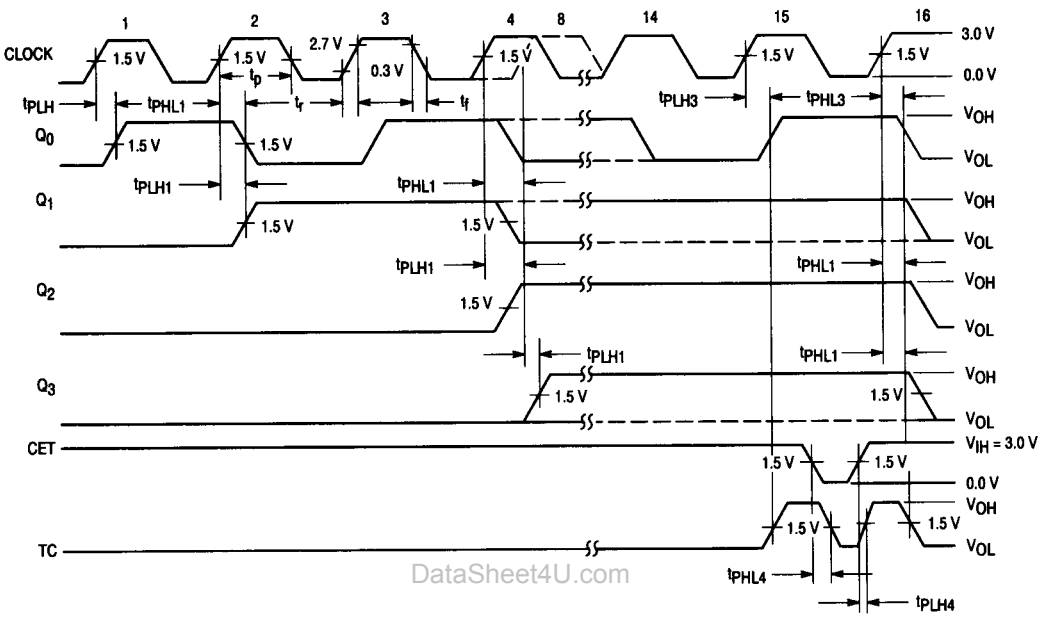
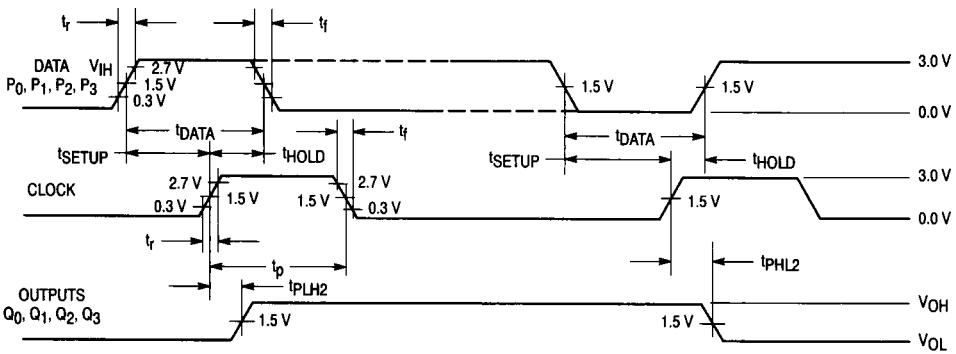
SWITCHING WAVEFORMS

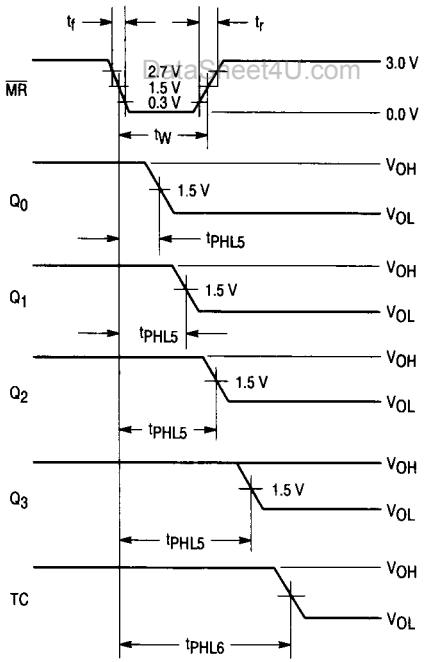


NOTES:
1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR $\leq$ 1.0 MHz, $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high $\geq$ 2.0 V, low $\leq$ 0.8 V, or open).
3. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. $R_L = 499\ \Omega \pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.

WAVEFORMS



NOTE:
The data pulse generator has the following characteristics:
V_{GEN} = 3.0 V, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, t_{DATA} = 7.0 ns, t_{SETUP} = 5.0 ns, t_{HOLD} = 2.0 ns.

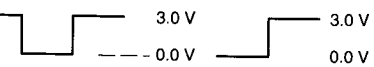


54F161A

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IN} = 2.0 V or 5.5 V, $\overline{MR}$ & CP = (See Note 1), $\overline{PE}$ = 0.8 V or 0 V, CET = 5.5 V or 2.0 V, CEP = 5.5 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IN} = 0.8 V or 5.5 V, $\overline{PE}$ = 0 V, CET = 5.5 V or 0.8 V, CEP & $\overline{MR}$ = 5.5 V, CP = (See Note 1) .
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH1}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, $\overline{PE}$ = 5.5 V, 0 V or (2.7 V), CET = 0 V or (2.7 V), other inputs are open.
I_{IH2}	Logical "1" Input Current		40		40		40	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, $\overline{PE}$ = 5.5 V, 0 V or (2.7 V), CET = 0 V or (2.7 V), other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, $\overline{PE}$ = 5.5 V, 0 V or (7.0 V), CET = 0 V or (7.0 V), other inputs are open).
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are open, $\overline{PE}$ = 0 V, $\overline{MR}$ & CP = (See Note 1), V_{OUT} = 0 V.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, $\overline{PE}$ = 0 V or 5.5 V, CET = open or 5.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−0.06	−1.2	−0.06	−1.2	−0.06	−1.2	mA	V_{CC} = 5.5 V, $\overline{MR}$ = 5.5 V or open, CEP = 5.5 V, $\overline{PE}$ & CET = 0.5 V or 5.5 V, other inputs are open.
I_{CC}	Power Supply Current Off		55		55		55	mA	V_{CC} = 5.5 V, V_{IN} = 0 V, (P_0–P_3), all other inputs = 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (**Repeat at**) V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

NOTE:

1. Apply one pulse prior to measurement.



54F161A

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output CP to Q_n ($\overline{PE}$ Input High)	3.5	10	3.5	11.5	3.5	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output CP to Q_n ($\overline{PE}$ Input High)	2.0	7.5	2.0	9.0	2.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL2}	Propagation Delay /Data-Output CP to Q_n ($\overline{PE}$ Input Low)	4.0	8.5	4.0	10	4.0	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output CP to Q_n ($\overline{PE}$ Input Low)	2.5	8.5	2.0	10	2.0	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL3}	Propagation Delay /Data-Output CP to TC	5.0	16	5.0	18.5	5.0	18.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH3}	Propagation Delay /Data-Output CP to TC	4.5	14	5.0	16.5	5.0	16.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL4}	Propagation Delay /Data-Output CET to TC	2.5	7.5	2.5	9.0	2.5	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH4}	Propagation Delay /Data-Output CET to TC	2.5	7.5	2.5	9.0	2.5	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL5}	Propagation Delay /Data-Output $\overline{MR}$ to Q_n	5.5	12	5.5	14	5.5	14	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL6}	Propagation Delay /Data-Output $\overline{MR}$ to TC	4.5	11.5	4.5	14	4.5	14	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
f_{MAX}	Maximum Clock Frequency	90		70		70		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

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