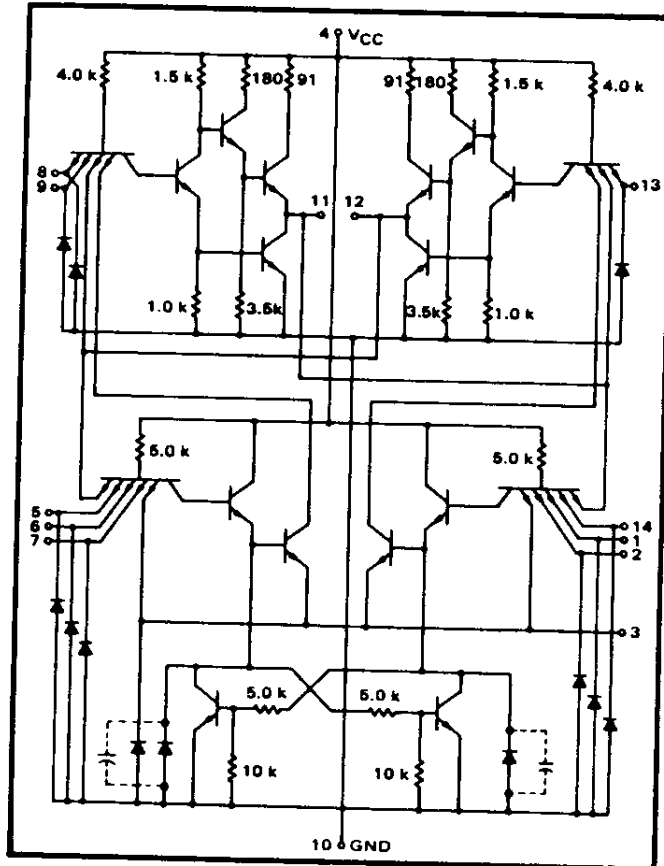


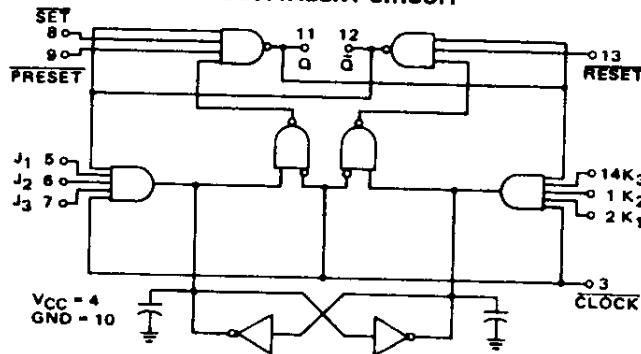
"AND" J-K FLIP-FLOP

MTTL I MC500/400 series

MC515 · MC565
MC415 · MC465



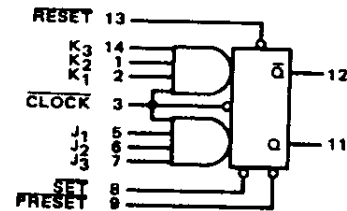
EQUIVALENT CIRCUIT



The MC415, MC465, MC515, and MC565 are clocked flip-flops that trigger on the negative edge and perform the J-K logic function. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gating in counters and certain other applications. A direct SET, PRESET, and RESET are also available.

In normal operation, information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in the high state. When the clock goes low, the information is transferred to the bistable section and the Q and Q-bar outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is in the high state. Each flip-flop can be set or reset directly by applying the low state to the direct SET, PRESET, or RESET inputs.

Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



J	K	Q _n	Q _{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where $J = J_1 \cdot J_2 \cdot J_3$
 $K = K_1 \cdot K_2 \cdot K_3$

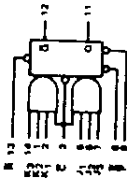
Total Power Dissipation = 40 mW typ/pkg

Switching Times:
 $t_{pd-} = 25$ ns typ
 $t_{pd+} = 13$ ns typ

TYPE NO.	INPUT LOADING FACTOR (I _F)				OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER		
MC515 MC565	1.5	1	(-2.0 mA)	(-1.33 mA)	15 MC500 series Gates (20 mA) 7 MC500 series Gates (10 mA)	-55°C to +125°C
MC415 MC465	1.5	1	(-2.5 mA)	(-1.66 mA)	12 MC400 series Gates (20 mA) 6 MC400 series Gates (10 mA)	0°C to +75°C

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



Characteristic	Symbol	Pin Under Test	TEST CONDITIONS												Grnd				
			mA			Volts													
			I _{OL}		I _{OH}		I _{IN}		2 I _{IN}		V _{IL}	V _{IH}	V _R	V _{TH1}		V _{TH0}	V _{OH1}	V _{OH0}	V _{CC}
			Pr.	Std.	Pr.	Std.	Pr.	Std.	Pr.	Std.	Pr.	Std.	Pr.	Std.		Pr.	Std.	Pr.	Std.
Input Forward Current	I _F	1	Temperature			MC515, MC565			MC415, MC465			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:			1.8, 10				
			-55°C			+25°C			+75°C			I _{OL}				4			
			+25°C			+25°C			+25°C			I _{OH}							
			+25°C			+25°C			+25°C			V _{IL}							
			+25°C			+25°C			+25°C			V _{IH}							
			+25°C			+25°C			+25°C			V _R							
Leakage Current	I _R	1	Temperature			MC515, MC565			MC415, MC465			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:			1.8, 10				
			-55°C			+25°C			+75°C			I _{OL}							
			+25°C			+25°C			+25°C			I _{OH}							
			+25°C			+25°C			+25°C			V _{IL}							
			+25°C			+25°C			+25°C			V _{IH}							
			+25°C			+25°C			+25°C			V _R							
Inverter Beta Current	I _L	1	Temperature			MC515, MC565			MC415, MC465			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:			1.8, 10				
			-55°C			+25°C			+75°C			I _{OL}							
			+25°C			+25°C			+25°C			I _{OH}							
			+25°C			+25°C			+25°C			V _{IL}							
			+25°C			+25°C			+25°C			V _{IH}							
			+25°C			+25°C			+25°C			V _R							
Breakdown Voltage	BV _{in 10}	5	Temperature			MC515, MC565			MC415, MC465			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:			1.8, 10				
			-55°C			+25°C			+75°C			I _{OL}							
			+25°C			+25°C			+25°C			I _{OH}							
			+25°C			+25°C			+25°C			V _{IL}							
			+25°C			+25°C			+25°C			V _{IH}							
			+25°C			+25°C			+25°C			V _R							

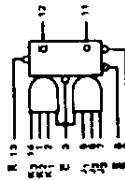
• Prime Fan-Out: (continued)

520

MC515, MC565/MC415, MC465 (continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



Characteristic	Symbol	Pin Under Test	TEST CONDITIONS												V _{OH}	V _{OL}	V _{CC}	V _{EE}
			mA						Volts									
			I _{OH}	I _{OL}	I _{in}	2 I _{in}	V _{ih}	V _{il}	V _{ih}	V _{il}	V _{ih1}	V _{ih0}	V _{ih0}	V _{CC}				
Clock Input Forward Current	I _F	3	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												-	-	-	-
			I _{OH}	I _{OL}	I _{in}	2 I _{in}	V _{ih}	V _{il}	V _{ih}	V _{il}	V _{ih1}	V _{ih0}	V _{ih0}	V _{CC}				
Leakage Current	I _R	3	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												-	-	-	-
			I _{OH}	I _{OL}	I _{in}	2 I _{in}	V _{ih}	V _{il}	V _{ih}	V _{il}	V _{ih1}	V _{ih0}	V _{ih0}	V _{CC}				
Inverse Beta Current	I _L	3	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												-	-	-	-
			I _{OH}	I _{OL}	I _{in}	2 I _{in}	V _{ih}	V _{il}	V _{ih}	V _{il}	V _{ih1}	V _{ih0}	V _{ih0}	V _{CC}				
Breakdown Voltage	BV _{in} (0)	3	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												-	-	-	-
			I _{OH}	I _{OL}	I _{in}	2 I _{in}	V _{ih}	V _{il}	V _{ih}	V _{il}	V _{ih1}	V _{ih0}	V _{ih0}	V _{CC}				
Output Output Voltage	V _{out} (0)	12	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												-	-	-	-
			I _{OH}	I _{OL}	I _{in}	2 I _{in}	V _{ih}	V _{il}	V _{ih}	V _{il}	V _{ih1}	V _{ih0}	V _{ih0}	V _{CC}				
Leakage Current	I _{OLK}	12	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												-	-	-	-
			I _{OH}	I _{OL}	I _{in}	2 I _{in}	V _{ih}	V _{il}	V _{ih}	V _{il}	V _{ih1}	V _{ih0}	V _{ih0}	V _{CC}				
Short-Circuit Current	I _{SC}	12	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												-	-	-	-
			I _{OH}	I _{OL}	I _{in}	2 I _{in}	V _{ih}	V _{il}	V _{ih}	V _{il}	V _{ih1}	V _{ih0}	V _{ih0}	V _{CC}				
Output Voltage	V _{OL}	12	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												-	-	-	-
			I _{OH}	I _{OL}	I _{in}	2 I _{in}	V _{ih}	V _{il}	V _{ih}	V _{il}	V _{ih1}	V _{ih0}	V _{ih0}	V _{CC}				
Power Requirements (Total Device) Power Supply Drain	I _{PD}	4	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												-	-	-	-
			I _{OH}	I _{OL}	I _{in}	2 I _{in}	V _{ih}	V _{il}	V _{ih}	V _{il}	V _{ih1}	V _{ih0}	V _{ih0}	V _{CC}				

@ Test Temperature

MC515^o, MC565

MC415^o, MC465

-55°C

+25°C

+125°C

0°C

+25°C

+75°C

* Prime Fan-Out

MC515, MC565/MC415, MC465 (continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 150 ns.

Triggers on clock pulse widths ≥ 20 ns.

Provides direct **SET**, **PRESET**, and **RESET** inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

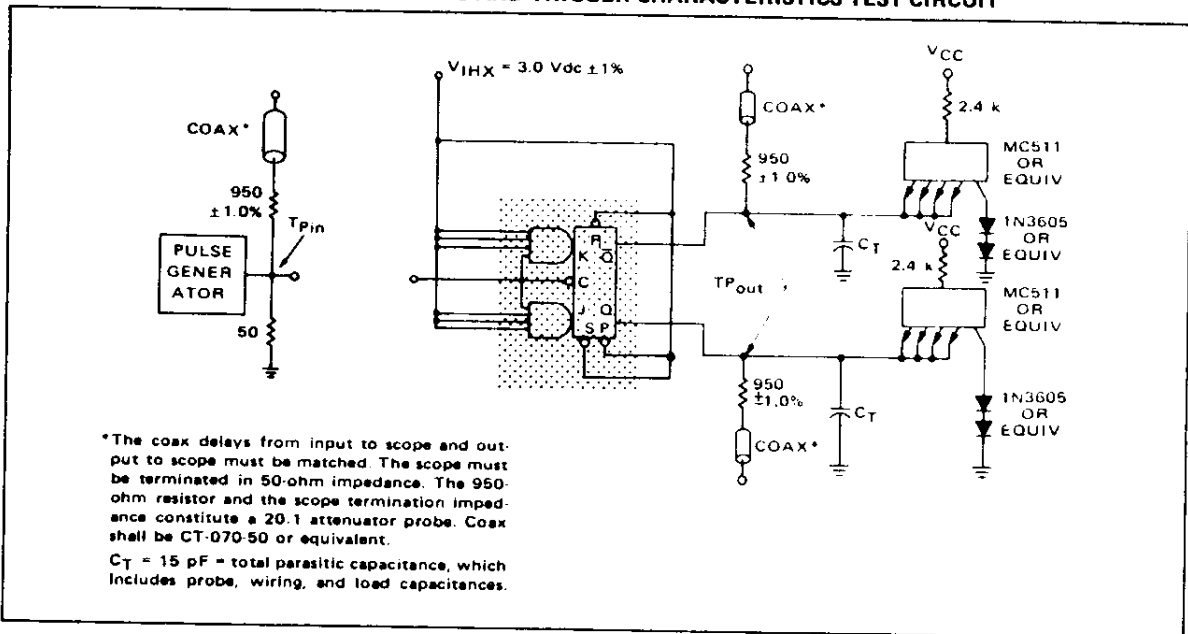
Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1"

state to "0" state information change on the J and K terminals. The flip-flop will require typically 10 ns to recognize a "0" state to "1" state change.

Negative edge triggering – When the clock goes from the high state to the low state, the information in the temporary storage section is transferred and the Q and \bar{Q} outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. **PRESET** and **SET** are tied to \bar{Q} ; **RESET** is tied to Q.

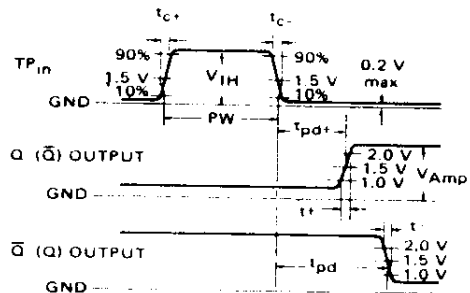
FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{pd+}	V		20	ns
Delay Time On	t_{pd-}	V		40	ns
Rise Time	t_r	V		8.0	ns
Fall Time	t_f	V		5.0	ns
Amplitude	V_{Amp}	V	3.2		Volt
WORST-CASE TESTS (Device must toggle with each clock pulse)					
TEST	SYMBOL	LIMITS	INPUT CONDITIONS		
Toggle Frequency	f_{Toq}	20 MHz max	W		
Pulse Width	PW	20 ns min	X		
Input High Voltage	V_{IH}	1.8 V min	Y		
Fall Time	t_{c-}	150 ns max	Z		

VOLTAGE WAVEFORMS AND DEFINITIONS



INPUT PULSE CONDITIONS

SYMBOL	W	V	X	Y	Z	UNIT
PRF	20	5.0	5.0	5.0	1.0	MHz
PW	20	100	20	100	200	ns
t_{c+}	≤ 10	≤ 10	≤ 10	≤ 10	≤ 50	ns
t_{c-}	≤ 10	≤ 10	≤ 10	≤ 10	≤ 150	ns
V_{IH}	3.5	3.5	3.5	1.8	3.5	Volt

MC515, MC565/MC415, MC465 (continued)

FIGURE 2 - J-K TERMINAL CHARACTERISTICS TEST CIRCUIT

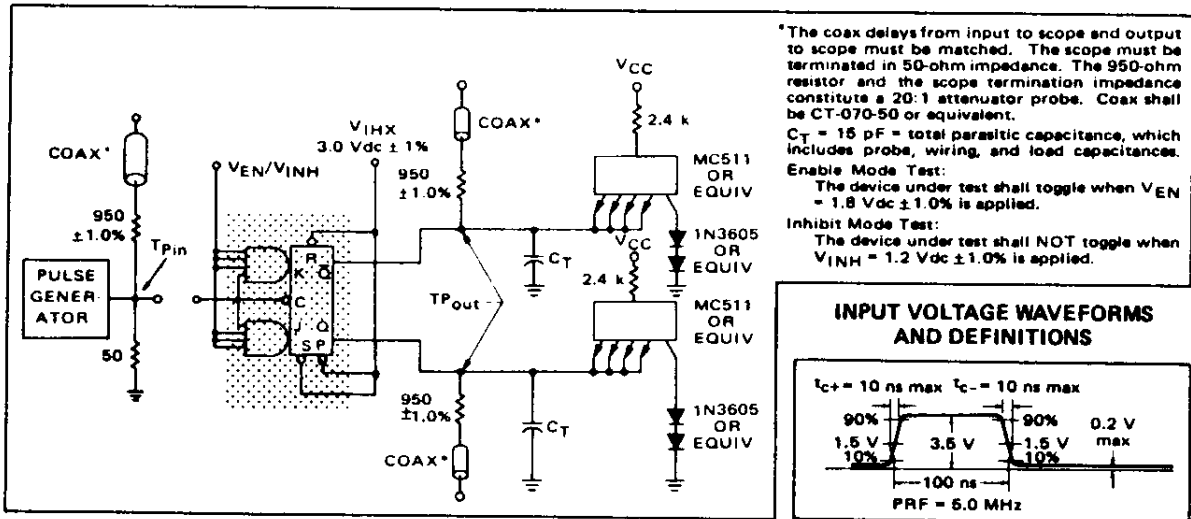


FIGURE 3 - SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT

