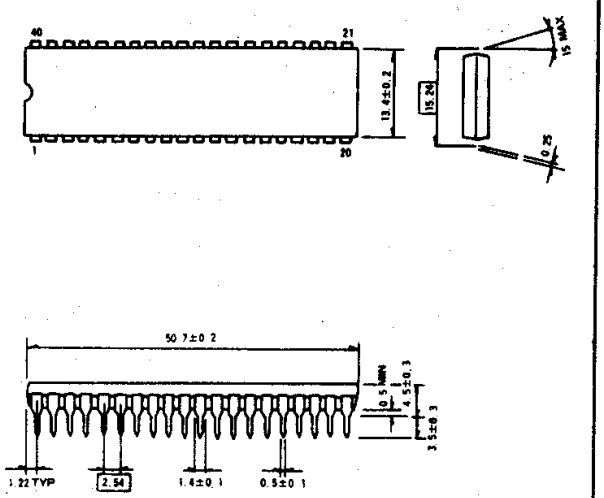
DMC 80C49

CMOS SINGLE-COMPONENT
8-BIT MICROCOMPUTER

40 DIP Unit: mm



☐ FEATURES

- ○ Pin-to-pin compatible with intel's 80C48/80C35/ 80C49/80C39
- ○ 80C48/80C49 Low power mask programmable ROM.
- ○ 80C35/80C39 Low power, CPU only.
- ○ 1.36 μsec instruction cycle.
  All instruction 1 or 2 cycles.
- ○ Ability to maintain operation during AC power line interruptions.
- ○ Exit idle mode with an external or internal interrupt signal.
- ○ Battery operation.
- ○ 3 power consumption selections
  - – Normal operation : 12mA @ 11MHz @5V
  - – Idle mode : 4.8mA @ 11mHz @5V
  - – Power down : 2μA @2V
- ○ 80C49 is also available as a standard cell.
- ○ 11MHz operation @5V ± 10%

☐ MAXIMUM RATINGS

- ○ Ambient temperature under bias : 0℃ ~ +70℃
- ○ Storage temperature : −65℃ ~ +150℃
- ○ Voltage on any pin with respect to ground : −0.5V ~ V_{CC} +1V
- ○ Maximum voltage on any pin with respect to ground : 7V
- ○ Power dissipation : 1.5 Watt.

BLOCK DIAGRAM AND DESCRIPTION

DAEWOO ZyMOS TECHNOLOGY' 80C48/80C35/80C49/80C39 are low power, CHMOS version of the popular MCS-48 HMOS family members. CHMOS is a technology built on HMOS II and features high resistivity P substrate, diffused N well, and scaled N and P channel devices. The 80C48/80C35/80C49/80C39 have been designed to provide low power consumption and high performance.

The 80C48/80C49 contains a 1Kx8/2Kx8 program memory, a 64x8/128x8 RAM data memory, 27 I/O lines, and an 8bit timer/counter in addition to on-board oscillator and clock circuits. The 80C35/80C39 is the equivalent of the 80C48/80C49 without program memory on-board.

The CMOS design of the 80C48/80C49 opens new application areas that require battery operation, low power standby, wide voltage range, and the ability to maintain operation during AC power line interruptions.

These applications include portable and hand-held instruments, telecommunication consumer and automotive.

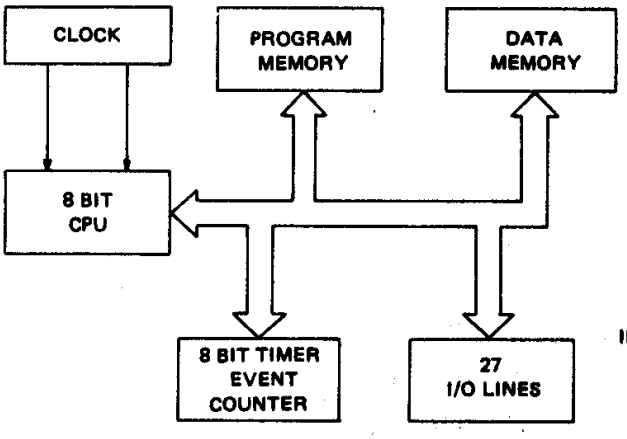


Figure 1.
Block Diagram

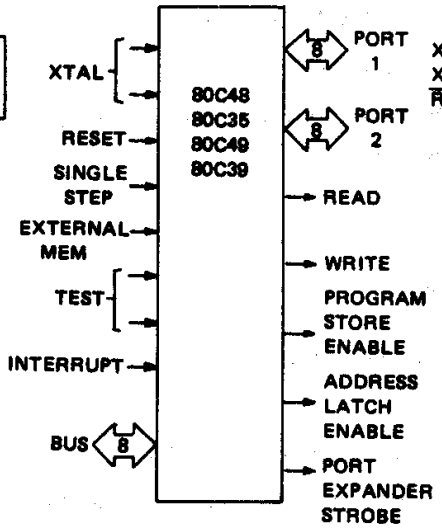


Figure 2.
Logic Symbol

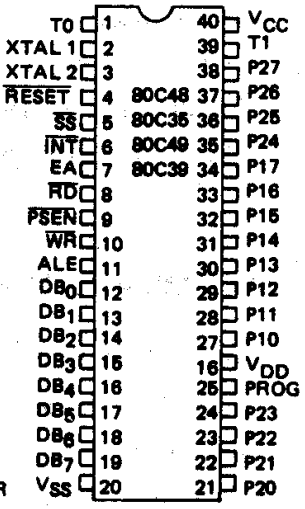


Figure 3.
Pin Configuration

☐ PIN DESCRIPTION

Symbol	Pin No.	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Low Power standby pin
V_{CC}	40	Main power supply ; +5V during operation
PROG	25	Output strobe for 82C43 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port
P20-P23	21-24	8-bit quasi-bidirectional port
P24-P27 Port 2	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the RD, WR strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENTO CLK instuction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
INT	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction.(Active low) Interrupt must remain low for at least 3 machine cycles for proper operation.
RD	8	Output strobe activated during a BUS read. Can be used to enable data onto toe bus from an external device. Used as a read strobe to external data memory. (Active low)
RESET	4	Input which is used to initialize the processor. (Active low)(Non TTL V_{IH})
WR	10	Ouput strobe during a bus write.(Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
PSEN	9	Program store enable. This output occurs only during

☐ PIN DESCRIPTION(Continued)

Symbol	Pin No.	Function
PSEN (Con't)		a fetch to external program memory.(Actibe low)
SS	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification.(Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

☐ IDLE MODE DESCRIPTION

The 80C48/80C35/80C49/80C39, when placed in idle mode, keeps the oscillator, the internal timer and the external interrupt and counter pins functioning, and maintains the internal register and RAM status.

To place the 80C48/80C35/80C49/80C39 in idle mode, a command instruction(op code 01H) is executed. To terminate idle mode, a reset must be performed or interrupts must be enabled and an interrupt signal generated.

There are two interrupt sources that can restore normal operation.

One is an external signal applied to the interrupt pin. The other is form the overflow of the timer/counter. When either interrupt is invoked, the CPU is taken out of Idle mode and vectors to the interrupt's service routine address.

Along with the idle mode, the standard MCS-48 power-down mode is still maintained. During normal operation, V_{CC} serves as the 5V supply pin for the bulk of the circuitry while the V_{DD} pin supplies only the RAM array.

In normal operation both V_{CC} and V_{DD} are at 5V. However, for power-down operation, V_{CC} is at ground and V_{DD} is reduced to its standby value.

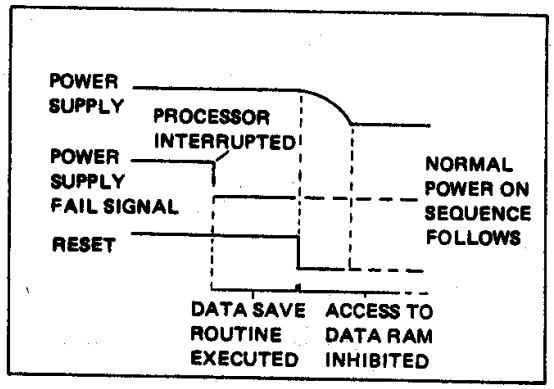
To be certain that RAM is not inadvertently accessed and altered during power down, reset should be applied to the processor until V_{CC} is at ground level.

☐ POWER DOWN MODE DESCRIPTION

Extra circuitry has been added to the 80C48/80C49 ROM version to allow power to be removed from all but the data RAM array for low power standby operation. In the power down mode the contents of data RAM can be maintained while drawing typically 10% to 15% of normal operating power requirements.

V_{CC} serves as the 5V supply pin for the bulk of circuitry while the V_{DD} pin supplies only the RAM array. In normal operation both pins are a 5V while in standby, V_{CC} is at ground and V_{DD} is maintained at its standby value. Applying Reset to the processor through the $\overline{RESET}$ pin inhibits any access to the RAM by the processor and guarantees that RAM cannot be inadvertently altered as power is removed from V_{CC}.

A typical power down sequence occurs as follows :



1) Imminent power supply failure is detected by user defined circuitry.
   Signal must be early enough to allow 80C48 to save all necessary data before V_{CC} falls below normal operating limits.

2) Power fail signal is used to interrupt processor and vector it to a power fail service routine.

3) Power fail routine saves all important data and machine status in the internal data RAM array. Routine may also initiate transfer of backup supply to the V_{DD} pin and indicate to external circuitry that power fail routine is complete.

4) Reset is applied to guarantee data will not be altered as the power supply falls out of limits.

   Reset must be held how until V_{CC} is at ground level.

□ INSTRUCTION SET

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, #data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A, @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL. A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A, P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers

Mnemonic	Description	Bytes	Cycle
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch

Mnemonic	Description	Bytes	Cycle
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JN1 addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Subroutine

Mnemonic	Description	Bytes	Cycle
CALL addr	Jump to subroutine	2	2

□ INSTRUCTION SET (Continued)

Subroutine (Con't)

Mnemonic	Description	Bytes	Cycles
RET	Return	1	2
RETR	Return and restore status	1	2

Flags

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	Clear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Data Moves

Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, # data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	1
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @	Move to A from page 3	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start timer	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNTI	Enable timer/counter interrupt	1	1
DIS TCNTI	Disable timer/counter interrupt	1	1

Control

Mnemonic	Description	Bytes	Cycles
EN I	Enable external interrupt	1	1
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1
IDL	Select Idle Operation	1	1

☐ ELECTRICAL CHARACTERISTICS(D.C)

(T_A=0~70℃, V_{CC}=V_{DD}=5V±10%, $|V_{CC}-V_{DD}|\leqq 1V$, V_{SS}=0V

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except X1, $\overline{RESET}$)	−0.5		0.18V_{CC}	V	
V_{IL1}	Input Low Voltage X1, $\overline{RESET}$	−5		0.13V_{CC}	V	
V_{IH}	Input High Voltage (All Except XTAL1, $\overline{RESET}$)	2		V_{CC}	V	
V_{IH1}	Input High Voltage(X1, $\overline{RESET}$)	0.7V_{CC}		V_{CC}	V	
V_{OL}	Output Low Voltage(BUS)			0.45	V	I_{OL}=2mA
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			0.45	V	I_{OL}=1.8mA
V_{OL2}	Output Low Voltage(PROG)			0.45	V	I_{OL}=1mA
V_{OL3}	Output Low Voltage (All Other Outputs)			0.45	V	I_{OL}=1.6mA
V_{OH}	Output High Voltage(BUS)	0.75V_{CC}			V	I_{OH}=−400μA
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	I_{OH}=−20μA
V_{OH2}	Output High Voltage (All Other Outputs)	0.75V_{CC}			V	I_{OH}=−40μA
I_{LI}	Input Leakage Current(T1, $\overline{INT}$, EA)			±5	μA	$V_{SS}\leqq V_{IN}\leqq V_{CC}$
I_{LI1}	Input Leakage Current (P10-P17, P20-27, $\overline{SS}$)			−500	μA	$V_{SS}\leqq V_{IN}\leqq V_{CC}$
I_{LO}	Output Leakage Current(BUS, TO) (High Impedance State)			±5	μA	$V_{SS}\leqq V_{IN}\leqq V_{CC}$
I_{LR}	Input Leakage Current($\overline{RESET}$)	−20		−300	μA	$V_{SS}\leqq V_{IN}\leqq V_{CC}$
I_{PD}	Power Down Standby Current			2	μA	V_{DD}=2V $\overline{RESET}$ $\leqq V_{IL}$

I_{CC} Active Current(mA)

V_{CC}	4.5V	5V	5.5V
1MHz	2.5	3.3	4
6MHz	5	6.8	8.5
11MHz	9	12	15

V_{CC}	4.5V	5V	5.5V
1MHz	1.7	2	2.2
6MHz	2	3	4
11MHz	3.5	4.8	6

Absolute Maximum Unloaded Current

☐ ELECTRICAL CHARACTERISTICS(A.C)

(T_A=0~70℃, V_{CC}=V_{DD}=5V±10%, $|V_{CC}-V_{DD}|$≦1V, V_{SS}=0V)

Symbol	Parameter	f(t) (Note 3)	11MHz		Unit	Conditions (Note 1)
			Min.	Max.		
t	Clock Period	1/xtal freq.	90.9	1000	ns	(Note 3)
t_{LL}	ALE Pulse Width	3.5t-170	150		ns	
t_{AL}	Addr Setup to ALE	2t-110	70		ns	(Note 2)
t_{LA}	Addr Hold from ALE	t-40	50		ns	
t_{CC1}	Control Pulse Width($\overline{RD}$, $\overline{WR}$)	7.5t-200	480		ns	
t_{CC2}	Control Pulse Width($\overline{PSEN}$)	6t-200	350		ns	
t_{DW}	DAta Setup before $\overline{WR}$	6.5t-200	390		ns	
t_{WD}	Data Hold after $\overline{WR}$	t-50	40		ns	
t_{DR}	Data Hold($\overline{RD}$, $\overline{PSEN}$)	1.5t-30	0	110	ns	
t_{RD1}	RD to Data in	6t-170		350	ns	
t_{RD2}	$\overline{PSEN}$ to Data in	4.5t-170		190	ns	
t_{AW}	Addr Setup to $\overline{WR}$	5t-150	300		ns	
t_{AD1}	Addr Setup to Data($\overline{RD}$)	10.5t-220		730	ns	
t_{AD2}	Addr Setup to Data($\overline{PSEN}$)	7.5t-220		460	ns	
t_{AFC1}	Addr Float to $\overline{RD}$, $\overline{WR}$	2t-40	140		ns	(Note 2)
t_{AFC2}	Addr Float to $\overline{PSEN}$	0.5t-40	10		ns	(Note 2)
t_{LAFC1}	ALE to Control($\overline{RD}$, $\overline{WR}$)	3t-75	200		ns	
t_{LAFC2}	ALE to Control($\overline{PSEN}$)	1.5t-75	60		ns	
t_{CA1}	Control to ALE($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t-40	50		ns	
t_{CA2}	Control to ALE($\overline{PSEN}$)	4t-40	320		ns	
t_{CP}	Port Control Setup to $\overline{PROG}$	1.5t-80	50		ns	
t_{PC}	Port Control Hold to $\overline{PROG}$	4t-260	100		ns	
t_{PR}	$\overline{PROG}$ to P2 Input Valid	8.5t-120		650	ns	
t_{PF}	Input Data Hold from $\overline{PROG}$	1.5t	0	140	ns	
t_{DP}	Output Data Setup	6t-290	250		ns	
t_{PD}	Output Data Hold	1.5t-90	40		ns	
t_{PP}	$\overline{PROG}$ Pulse Width	10.5t-250	700		ns	
t_{PL}	Port 2 I/O Setup to ALE	4t-200	160		ns	
t_{LP}	Port 2 I/O Hold to ALE	1.5t-120	15		ns	
t_{PV}	Port Output from ALE	4.5t+100		510	ns	
t_{OPRR}	T0 Rep Rate	3t	270		ns	
t_{CY}	Cycle Time	15t	1.36	15	μs	

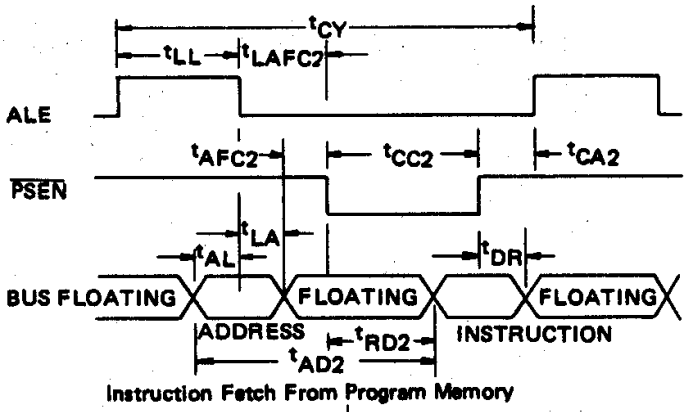
Note : 1. Control output C_L=80pF, Bus outputs C_L=150pF

2. Bus high impedance Load 20pf

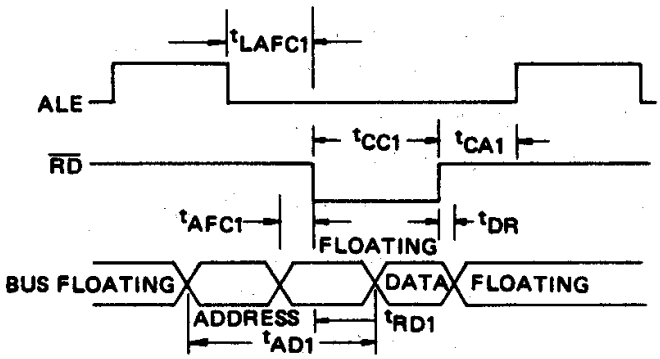
3. f(t) assumes 50% duty cycle on X1, X2 Max. clock period is for a 1MHz crystal input.

☐ TIMING DIAGRAM

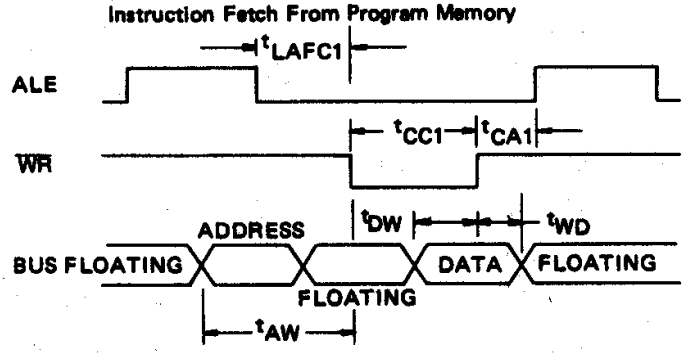
○ Waveforms



Instruction Fetch From Program Memory



Read From External Data Memory

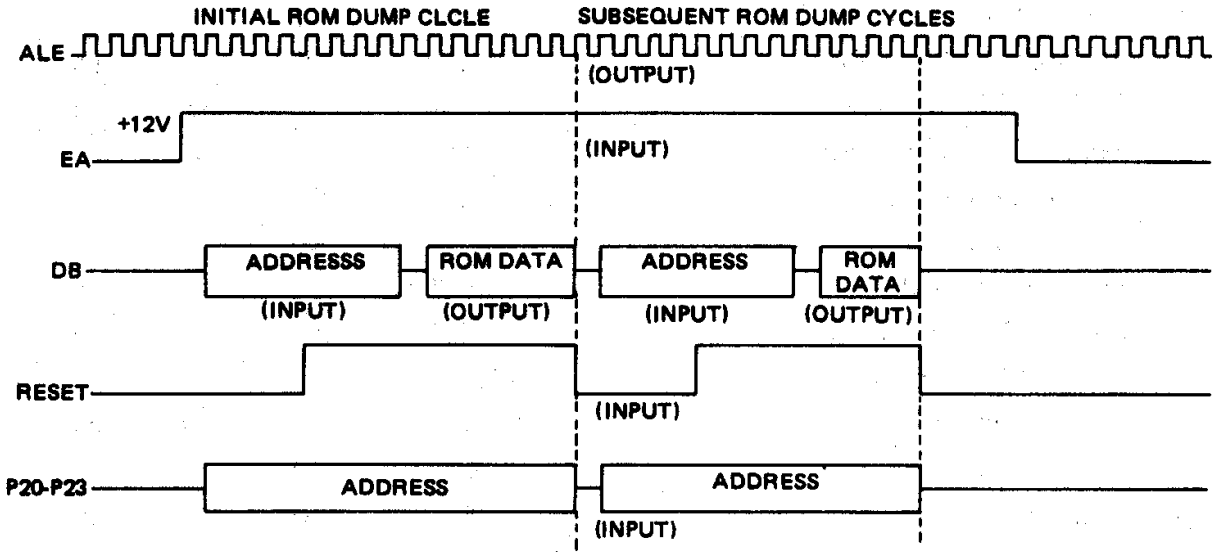


Write To External Data Memory

A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Output timing measurements are made at 2V for a logic "1" and 0.8V for a logic "0".

Input And Output For A.C. Tests

○ Suggested ROM verification algorithm for CMOS devices only



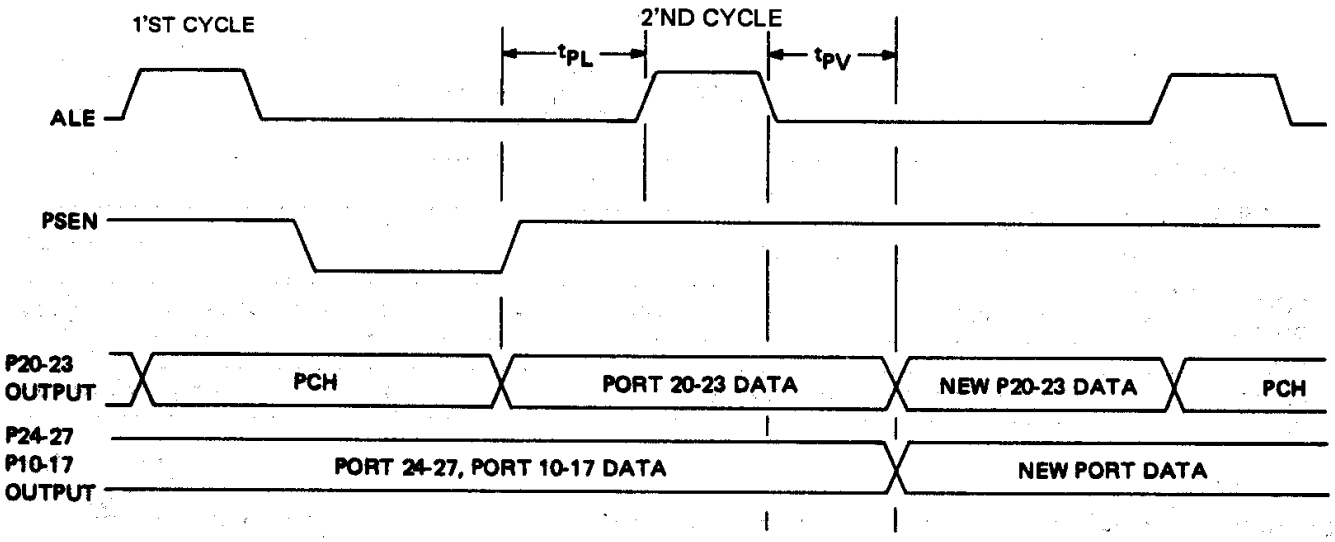
	C48	C49
A10	0	ADDR
A11	0	0

$V_{CC} = V_{DD} = +5V$

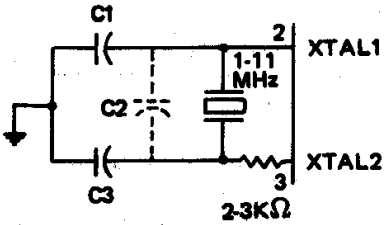
$V_{SS} = 0V$

☐ TIMING DIAGRAM (Continued)

○ I/O Port timing



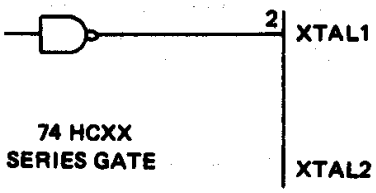
OSCILLATOR MODE



C1 = 20pF ± 2pF - STRAY < 5pF
C2 = CRYSTAL - STRAY < 8pF
C3 = 20pF ± 2pF - STRAY < 5pF

Crystal series resistance should be less than 30Ω at 11 MHz; less than 75Ω at 6 MHz; less than 180Ω at 3.6 MHz.

DRIVING FROM EXTERNAL SOURCE



XTAL1 must be high 35-65% of the period.

Rise and fall times must not be slower than 20 nS.

☐ TIMING DIAGRAM(Continued)

o Port 1/Port 2 timing