October 2002

# National Semiconductor

## LM4866 Boomer® Audio Power Amplifier Series
# 2.2W Stereo Audio Amplifier

## General Description

The LM4866 is a bridge-connected (BTL) stereo audio power amplifier which, when connected to a 5V supply, delivers 2.2W to a 4Ω load (Note 1) or 2.5W to a 3Ω load (Note 2) with less than 1.0% THD+N.

With the LM4866 packaged in the LLP, the customer benefits include low thermal impedance, low profile, and small size. This package minimizes PCB area and maximizes output power.

The LM4866 features an externally controlled, low-power consumption shutdown mode, and thermal shutdown protection. It also utilizes circuitry to reduce "clicks and pops" during device turn-on.

Boomer audio power amplifiers are designed specifically to use few external components and provide high quality output power in a surface mount package.

**Note 1:** An LM4866MTE or LM4866LQ that has been properly mounted to a circuit board will deliver 2.2W into 4Ω. The other package options for the LM4866 will deliver 1.1W into 8Ω. See the Application Information sections for further information concerning the LM4866MTE and LM4866LQ.

**Note 2:** An LM4866MTE or LM4866LQ that has been properly mounted to a circuit board will deliver 2.5W into 3Ω.

## Key Specifications

- $P_O$ at 1% THD+N
- LM4866LQ, 3Ω, 4Ω loads         2.5W(typ), 2.2W(typ)
- LM4866MTE, 3Ω, 4Ω loads        2.5W(typ), 2.2W(typ)
- LM4866MTE, 8Ω load             1.1W(typ)
- LM4866MT, 8Ω load              1.1W(typ)
- Shutdown current               0.7µA(typ)
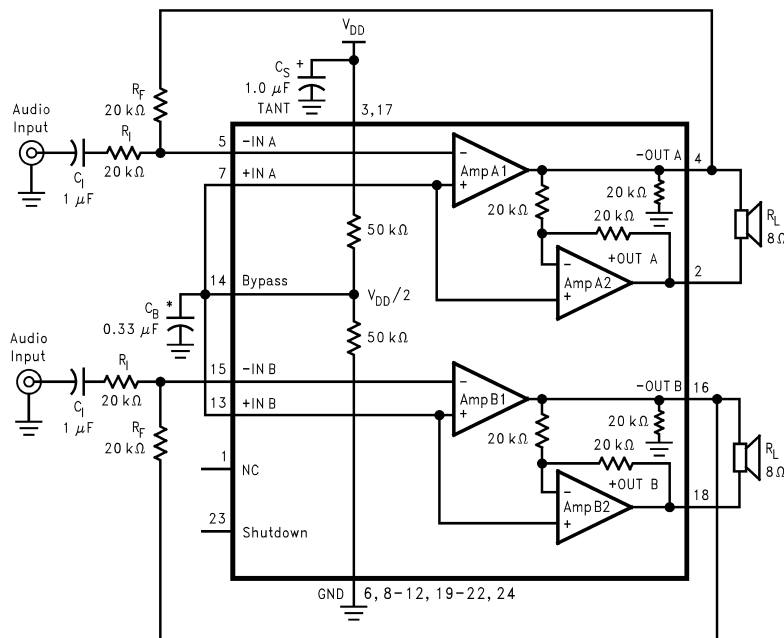- Supply voltage range           2.0V to 5.5V

## Features

- Stereo BTL amplifier mode
- "Click and pop" suppression circuitry
- Unity-gain stable
- Thermal shutdown protection circuitry
- TSSOP and Exposed-DAP LLP packages

## Applications

- Multimedia monitors
- Portable and desktop computers
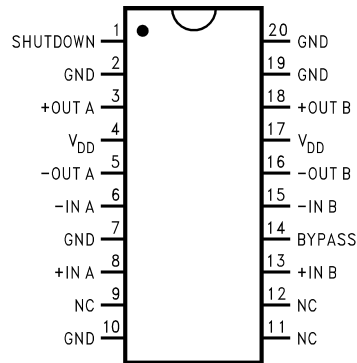- Portable televisions

## Typical Application



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Note: Pin out shown for LLP package. Refer to the Connection Diagrams for the pinout of the TSSOP package.
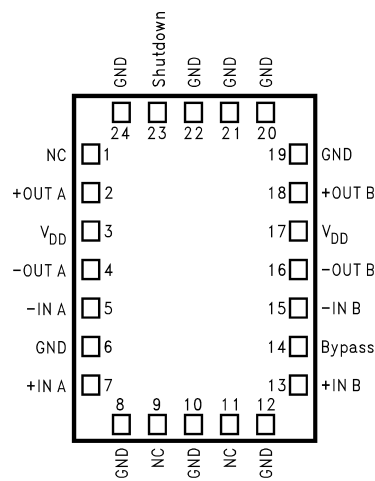
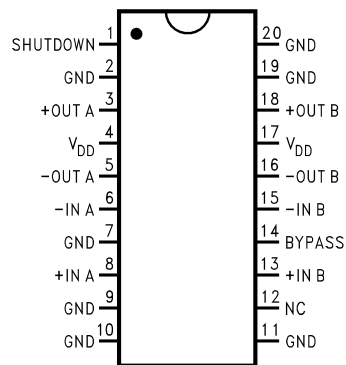Boomer® is a registered trademark of National Semiconductor Corporation.

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# Connection Diagrams



**Top View**
**Order Number LM4866MT**
**See NS Package Number MTC20 for TSSOP**



**Top View**
**Order Number LM4866LQ**
**See NS Package Number LQA24A for Exposed-DAP LLP**



**Top View**
**Order Number LM4866MTE**
**See NS Package Number MXA20A for Exposed-DAP TSSOP**

## Absolute Maximum Ratings (Note 3)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 6.0V |
| Storage Temperature | −65˚C to +150˚C |
| Input Voltage | −0.3V to $V_{DD}$ +0.3V |
| Power Dissipation (Note 4) | Internally limited |
| ESD Susceptibility(Note 5) | 2000V |
| ESD Susceptibility (Note 6) | 200V |
| Junction Temperature | 150˚C |
| Solder Information | |
|   Small Outline Package | |
|     Vapor Phase (60 sec.) | 215˚C |
|     Infrared (15 sec.) | 220˚C |

See AN-450 "Surface Mounting and their Effects on Product Reliablilty" for other methods of soldering surface mount devices.

Thermal Resistance

| | |
|---|---|
| $\theta_{JC}$ (typ) — MTC20 | 20˚C/W |
| $\theta_{JA}$ (typ) — MTC20 | 80˚C/W |
| $\theta_{JC}$ (typ) — LQ24A | 3.0˚C/W |
| $\theta_{JA}$ (typ) — LQ24A | 42˚C/W (Note 7) |
| $\theta_{JC}$ (typ) — MXA20A | 2˚C/W |
| $\theta_{JA}$ (typ) — MXA20A | 41˚C/W (Note 8) |
| $\theta_{JA}$ (typ) — MXA20A | 51˚C/W (Note 9) |
| $\theta_{JA}$ (typ) — MXA20A | 90˚C/W (Note 10) |

## Operating Ratings

Temperature Range

| | |
|---|---|
| $T_{MIN} \leq T_A \leq T_{MAX}$ | −40˚C ≤ $T_A$ ≤ 85˚C |
| Supply Voltage | 2.0V ≤ $V_{DD}$ ≤ 5.5V |

## Electrical Characteristics for Entire IC (Notes 3, 11)

The following specifications apply for $V_{DD}$= 5V unless otherwise noted. Limits apply for $T_A$= 25˚C.

| Symbol | Parameter | Conditions | LM4866 | | Units |
|---|---|---|---|---|---|
| | | | **Typical** | **Limit** | **(Limits)** |
| | | | (Note 12) | (Note 13) | |
| $V_{DD}$ | Supply Voltage | | | 2 | V (min) |
| | | | | 5.5 | V (max) |
| $I_{DD}$ | Quiescent Power Supply Current | $V_{IN}$ = 0V, $I_O$ = 0A (Note 14) | 11.5 | 20 | mA (max) |
| | | | | 6 | mA (min) |
| $I_{SD}$ | Shutdown Current | $V_{DD}$ applied to the SHUTDOWN pin | 0.7 | 2 | µA (min) |

## Electrical Characteristics for Bridged-Mode Operation (Notes 3, 11)

The following specifications apply for $V_{DD}$= 5V unless otherwise specified. Limits apply for $T_A$= 25˚C.

| Symbol | Parameter | Conditions | LM4866 | | Units |
|---|---|---|---|---|---|
| | | | **Typical** | **Limit** | **(Limits)** |
| | | | (Note 12) | (Note 13) | |
| $V_{OS}$ | Output Offset Voltage | $V_{IN}$ = 0V | 5 | 50 | mV (max) |
| $P_O$ | Output Power (Note 15) | THD+N = 1%, f = 1kHz (Note 16) | | | |
| | |   LM4866MTE, $R_L$ = 3Ω | 2.5 | | W |
| | |   LM4866LQ, $R_L$ = 3Ω | 2.5 | | W |
| | |   LM4866MTE, $R_L$ = 4Ω | 2.2 | | W |
| | |   LM4866LQ, $R_L$ = 4Ω | 2.2 | | W |
| | |   LM4866MT, $R_L$ = 8Ω | 1.1 | 1.0 | W (min) |
| | | THD+N = 10%, f = 1kHz | | | |
| | |   LM4866MTE, $R_L$ = 3Ω | 3.2 | | W |
| | |   LM4866LQ, $R_L$ = 3Ω | 3.2 | | W |
| | |   LM4866MTE, $R_L$ = 4Ω | 2.7 | | W |
| | |   LM4866LQ, $R_L$ = 4Ω | 2.7 | | W |
| | |   LM4866MT, $R_L$ = 8Ω | 1.5 | | W |

3

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# Electrical Characteristics for Bridged-Mode Operation (Notes 3, 11) (Continued)

The following specifications apply for $V_{DD}$= 5V unless otherwise specified. Limits apply for $T_A$= 25˚C.

| Symbol | Parameter | Conditions | LM4866 | | Units |
|--------|-----------|-----------|--------|--------|-------|
| | | | **Typical** | **Limit** | **(Limits)** |
| | | | (Note 12) | (Note 13) | |
| THD+N | Total Harmonic Distortion+Noise | $20Hz \leq f \leq 20kHz$, $A_{VD} = 2$ | | | |
| | | LM4866MTE, $R_L = 4\Omega$, $P_O = 2W$ | 0.3 | | |
| | | LM4866LQ, $R_L = 4\Omega$, $P_O = 2W$ | 0.3 | | |
| | | LM4866MT, $R_L = 4\Omega$, $P_O = 1W$ | 0.3 | | |
| | | LM4866MT, $R_L = 8\Omega$, $P_O = 1W$ | 0.3 | | % |
| PSRR | Power Supply Rejection Ratio | $V_{DD} = 5V$, $V_{RIPPLE} = 200mV_{RMS}$, $R_L = 8\Omega$, $C_B = 1.0\mu F$ | 67 | | dB |
| $X_{TALK}$ | Channel Separation | $f = 1kHz$, $C_B = 1.0\mu F$ | 90 | | dB |
| SNR | Signal To Noise Ratio | $V_{DD} = 5V$, $P_O = 1.1W$, $R_L = 8\Omega$ | 98 | | dB |

**Note 3:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

**Note 4:** The maximum power dissipation is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature $T_A$ and must be derated at elevated temperatures. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4866, $T_{JMAX} = 150˚C$. For the $\theta_{JA}$s for different packages, please see the Application Information section or the Absolute Maximum Ratings section.

**Note 5:** Human body model, 100pF discharged through a 1.5kΩ resistor.

**Note 6:** Machine model, 220pF–240pF discharged through all pins.

**Note 7:** The given $\theta_{JA}$ is for an LM4866 packaged in an LQA24A with the exposed–DAP soldered to an exposed 2in$^2$ area of 1oz printed circuit board copper.

**Note 8:** The given $\theta_{JA}$ is for an LM4866 packaged in an MXA20A with the exposed–DAP soldered to an exposed 2in$^2$ area of 1oz printed circuit board copper.

**Note 9:** The given $\theta_{JA}$ is for an LM4866 packaged in an MXA20A with the exposed–DAP soldered to an exposed 1in$^2$ area of 1oz printed circuit board copper.

**Note 10:** The given $\theta_{JA}$ is for an LM4866 packaged in an MXA20A with the exposed–DAP not soldered to prinbted circuit board copper.

**Note 11:** All voltages are measured with respect to the ground (GND) pins unless otherwise specified.

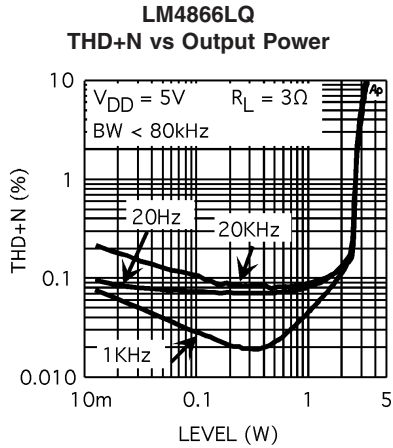**Note 12:** Typicals are measured at 25˚C and represent the parametric norm.

**Note 13:** Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

**Note 14:** The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
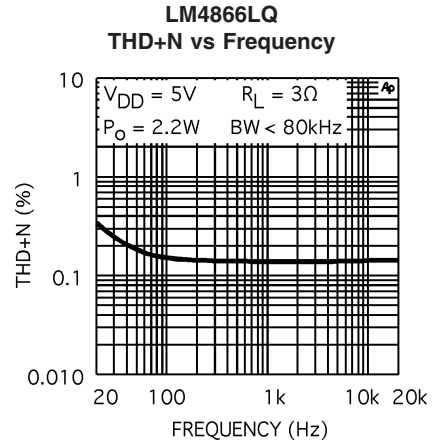
**Note 15:** Output power is measured at the device terminals.

**Note 16:** When driving 3Ω or 4Ω loads and operating on a 5V supply, the LM4866LQ and LM4866MTE must be mounted to a circuit board that has a minimum of 2.5in$^2$ of exposed, uninterrupted copper area connected to the package's exposed DAP.
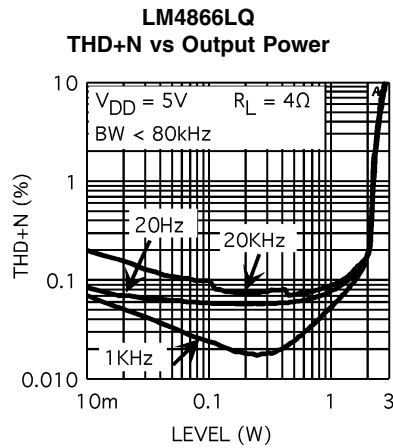
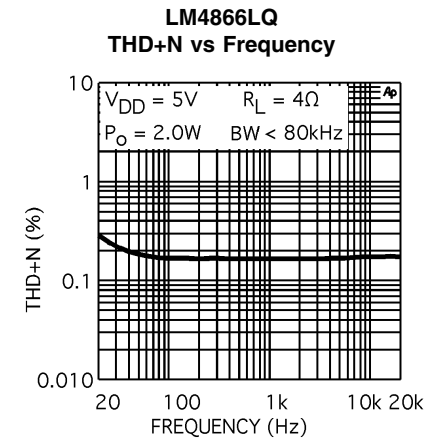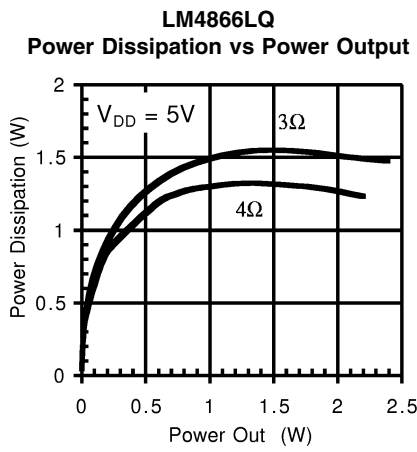# Typical Performance Characteristics
## LQ Specific Characteristics

**LM4866LQ**
**THD+N vs Output Power**



20018666

**LM4866LQ**
**THD+N vs Frequency**



20018668

**LM4866LQ**
**THD+N vs Output Power**



20018665

**LM4866LQ**
**THD+N vs Frequency**



20018667

**LM4866LQ**
**Power Dissipation vs Power Output**



20018664

**LM4866LQ** (Note 17)
**Power Derating Curve**
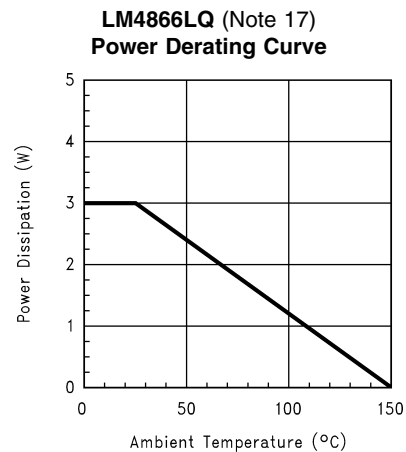


20018695

**Note 17:** This curve shows the LM4866LQ's thermal dissipation ability at different ambient temperatures given this condition:
The LLP package's DAP is soldered to a 2.5in$^2$, 1oz. copper plane.

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# Typical Performance Characteristics
## MTE Specific Characteristics

**LM4866MTE**
**THD+N vs Output Power**



$V_{DD} = 5V$    $R_L = 3\Omega$
BW < 80kHz

20018637

**LM4866MTE**
**THD+N vs Frequency**



$V_{DD} = 5V$    $R_L = 3\Omega$
$P_O = 2.2W$    BW < 80kHz

20018638

**LM4866MTE**
**THD+N vs Output Power**



$V_{DD} = 5V$    $R_L = 4\Omega$
BW < 80kHz

20018639

**LM4866MTE**
**THD+N vs Frequency**



$V_{DD} = 5V$    $R_L = 4\Omega$
$P_O = 2.0W$    BW < 80kHz

20018640

**LM4866MTE**
**Power Dissipation vs Power Output**



$V_{DD} = 5V$    $3\Omega$
$4\Omega$

20018641

**LM4866MTE**(Note 18)
**Power Derating Curve**



With 2.5 in$^2$
Heatsink Plane
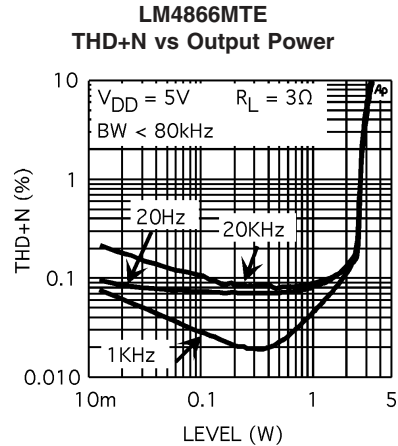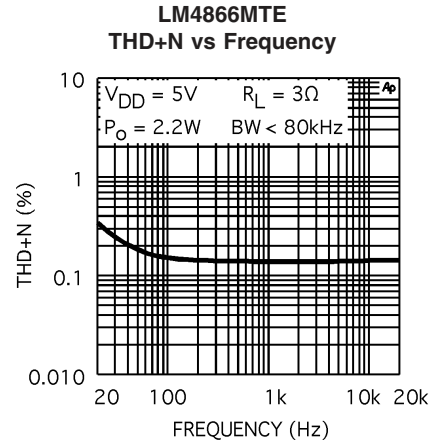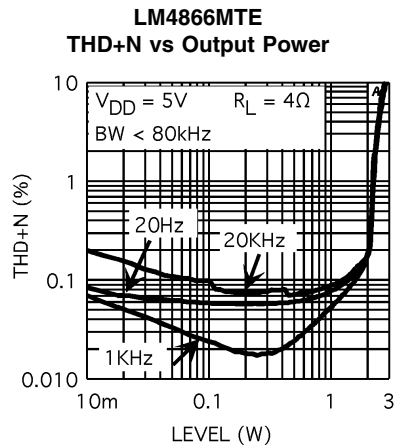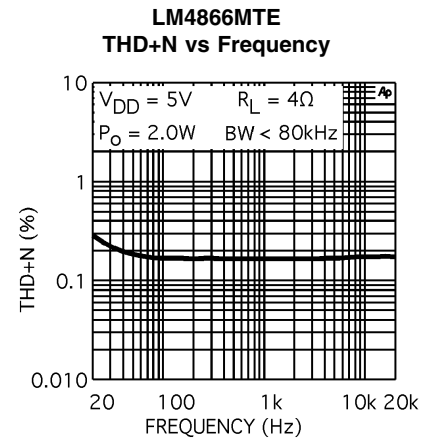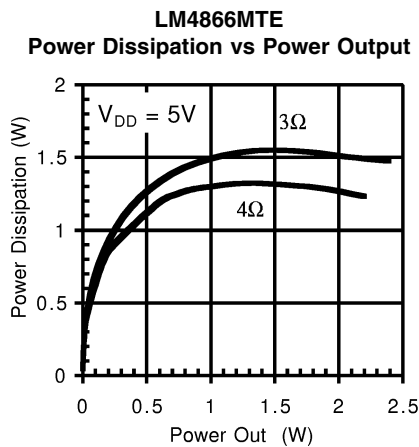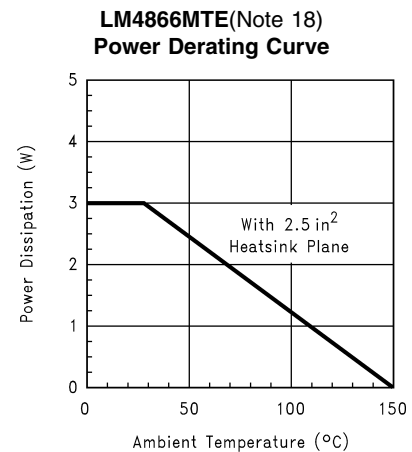
20018642

**Note 18:** This curve shows the LM4866MTE's thermal dissipation ability at different ambient temperatures given these conditions:
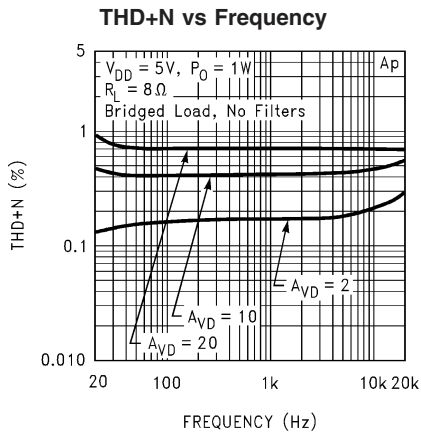
**500LFPM + JEDEC board:** The part is soldered to a 1S2P 20-lead exposed-DAP TSSOP test board with 500 linear feet per minute of forced-air flow across it. **Board information** - copper dimensions: 74x74mm, copper coverage: 100% (buried layer) and 12% (top/bottom layers), 16 vias under the exposed-DAP.

**500LFPM + 2.5in$^2$:** The part is soldered to a 2.5in$^2$, 1 oz. copper plane with 500 linear feet per minute of forced-air flow across it.
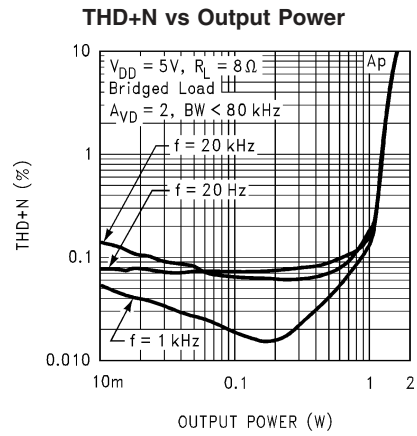
**2.5in$^2$:** The part is soldered to a 2.5in$^2$, 1oz. copper plane.

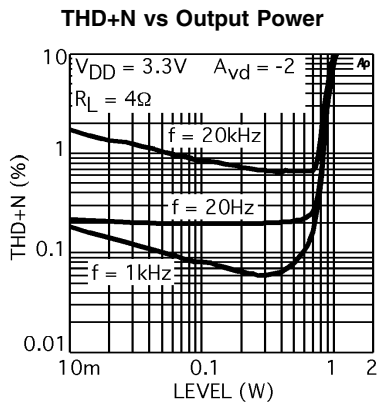**Not Attached:** The part is not soldered down and is not forced-air cooled.
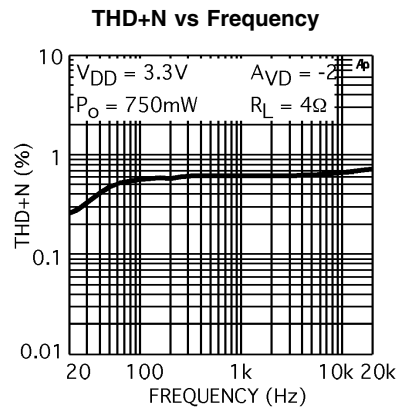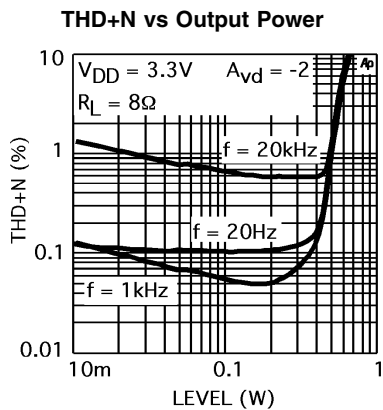
# Typical Performance Characteristics
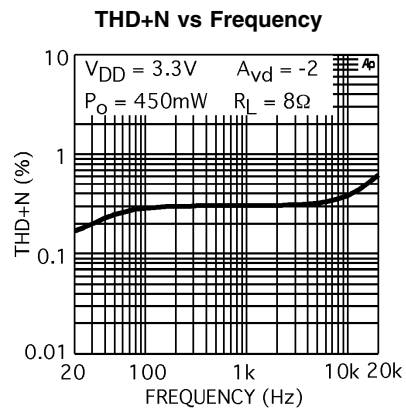
**THD+N vs Frequency**



20018603

**THD+N vs Output Power**



20018606

**THD+N vs Output Power**



20018661

**THD+N vs Frequency**



20018663

**THD+N vs Output Power**



20018660

**THD+N vs Frequency**



20018662

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# Typical Performance Characteristics (Continued)

**Output Power vs
Supply Voltage**



20018609

**Output Power vs
Load Resistance**



20018612

**Power Dissipation vs
Output Power**



20018614

**Dropout Voltage vs
Supply Voltage**



20018615

**Power Derating Curve**



20018616

**Noise Floor**



20018618

# Typical Performance Characteristics (Continued)

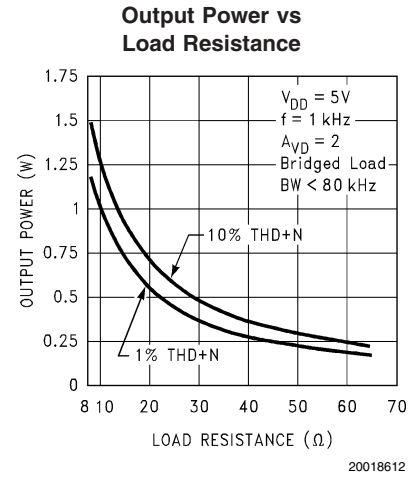**Channel Separation**



20018619

**Power Supply Rejection Ratio**



20018621

**Open Loop Frequency Response**



20018622

**Supply Current vs Supply Voltage**
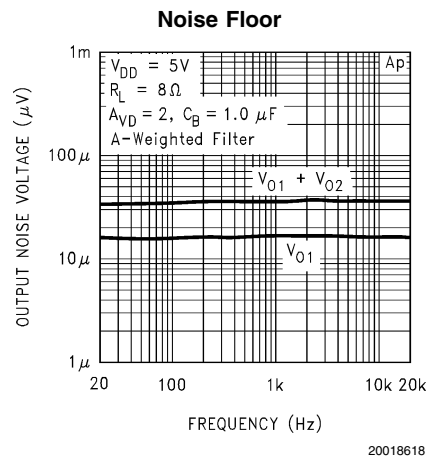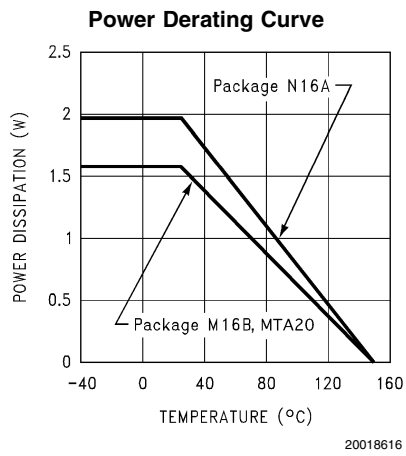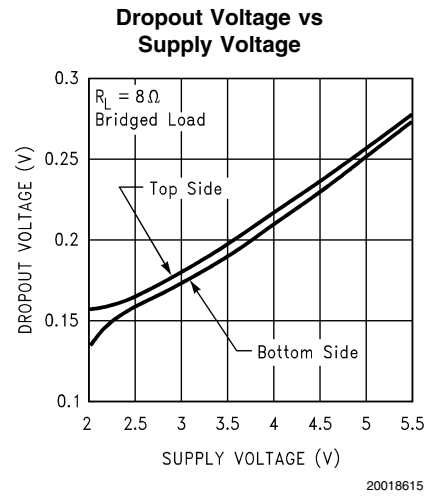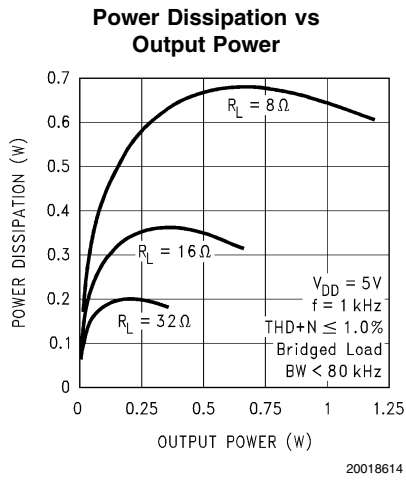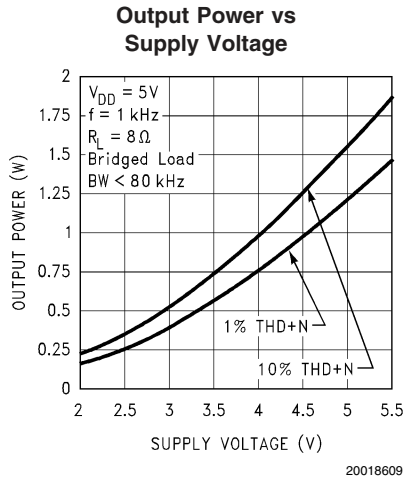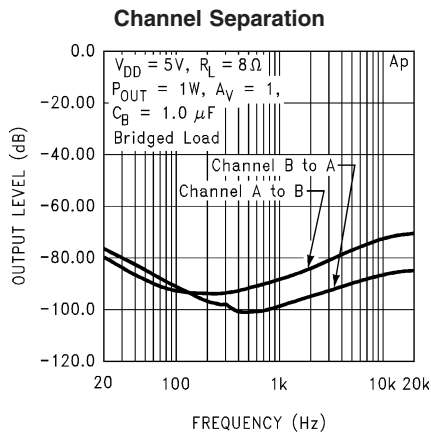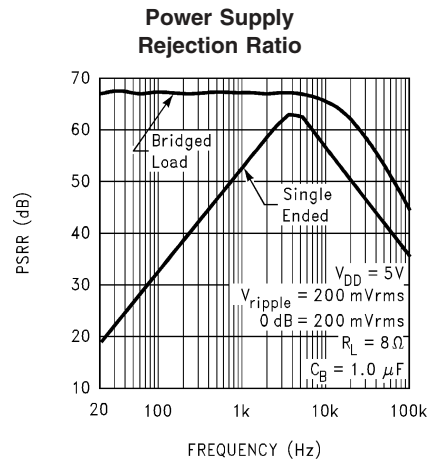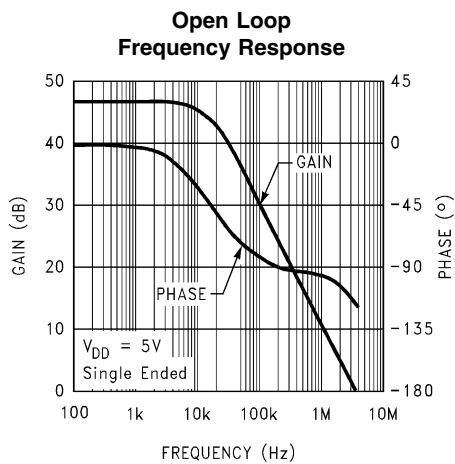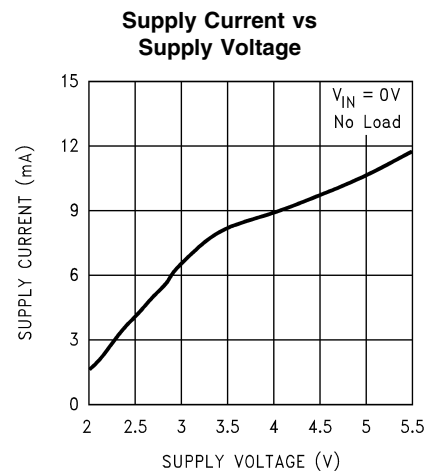


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# External Components Description

(Refer to *Figure 1*.)

| Components | | Functional Description |
|---|---|---|
| 1. | $R_i$ | The Inverting input resistance, along with $R_f$, set the closed-loop gain. $R_i$, along with $C_i$, form a high pass filter with $f_c = 1/(2\pi R_i C_i)$. |
| 2. | $C_i$ | The input coupling capacitor blocks DC voltage at the amplifier's input terminals. $C_i$, along with $R_i$, create a highpass filter with $f_c = 1/(2\pi R_i C_i)$. Refer to the section, **SELECTING PROPER EXTERNAL COMPONENTS**, for an explanation of determining the value of $C_i$. |
| 3. | $R_f$ | The feedback resistance, along with $R_i$, set the closed-loop gain. |
| 4. | $C_s$ | The supply bypass capacitor. Refer to the **POWER SUPPLY BYPASSING** section for information about properly placing, and selecting the value of, this capacitor. |
| 5. | $C_B$ | The capacitor, $C_B$, filters the half-supply voltage present on the BYPASS pin. Refer to the **SELECTING PROPER EXTERNAL COMPONENTS** section for information concerning proper placement and selecting $C_B$'s value. |

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# Application Information

### EXPOSED-DAP PACKAGE (LLP) PCB MOUNTING CONSIDERATIONS

The LM4866's exposed-DAP (die attach paddle) packages (MTE and LQ) provide a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 2.2W at ≤ 1% THD with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4866's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The MTE and LQ packages must have their DAPs soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 32(4x8) (MTE) or 6(3x2) (LQ) vias. The via diameter should be 0.012in - 0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating-through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in$^2$ (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4866 should be 5in$^2$ (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25˚c ambient temperature. Increase the area to compensate for ambient temperatures above 25˚c. In systems using cooling fans, the LM4866MTE can take advantage of forced air cooling. With an air flow rate of 450 linear-feet per minute and a 2.5in$^2$ exposed copper or 5.0in$^2$ inner layer copper plane heatsink, the LM4866MTE can continuously drive a 3Ω load to full power. The LM4866LQ achieves the same output power

level without forced air cooling. In all circumstances and conditions, the junction temperature must be held below 150˚C to prevent activating the LM4866's thermal shutdown protection. The LM4866's power de-rating curve in the **Typical Performance Characteristics** shows the maximum power dissipation versus temperature. Example PCB layouts for the exposed-DAP TSSOP and LLP packages are shown in the **Demonstration Board Layout** section.

Further detailed and specific information concerning PCB layout, fabrication, and mounting an LLP package is available from National Semiconductor's AN-1187.

### PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

# Application Information (Continued)
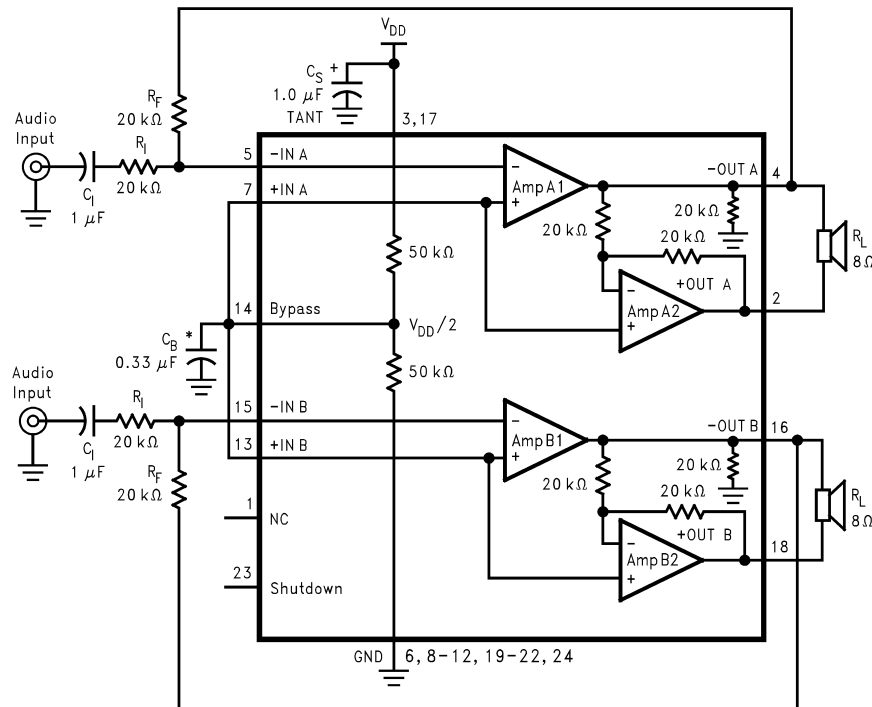


* Refer to the section Proper Selection of External Components, for a detailed discussion of $C_B$ size.

20018601

**FIGURE 1. Typical Audio Amplifier Application Circuit**
**Pin out shown for the LLP package. Refer to the Connection Diagrams for the pinout of the TSSOP package.**

## BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4866 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.) External resistors $R_f$ and $R_i$ set the closed-loop gain of Amp1A, whereas two internal 20kΩ resistors set Amp2A's gain at -1. The LM4866 drives a load, such as a speaker, connected between the two amplifier outputs, -OUTA and +OUTA.

*Figure 1* shows that Amp1A's output serves as Amp2A's input. This results in both amplifiers producing signals identical in magnitude, but 180˚ out of phase. Taking advantage of this phase difference, a load is placed between -OUTA and +OUTA and driven differentially (commonly referred to as 'bridge mode'). This results in a differential gain of

$$A_{VD} = 2 \times (R_f / R_i) \qquad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the

output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the **Audio Power Amplifier Design** section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

## POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \text{ Single-Ended} \qquad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4866 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended ampli-

## Application Information (Continued)

fier. From Equation (3), assuming a 5V power supply and an 4Ω load, the maximum single channel power dissipation is 1.27W or 2.54W for stereo operation.

$$P_{DMAX} = 4 \times (V_{DD})^2 / (2\pi^2 R_L) \text{ Bridge Mode} \qquad (3)$$

The LM4973's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \qquad (4)$$

The LM4866's $T_{JMAX} = 150°C$. In the LQ (LLP) package soldered to a DAP pad that expands to a copper area of 5in$^2$ on a PCB, the LM4866's $\theta_{JA}$ is 20°C/W. In the MTE package soldered to a DAP pad that expands to a copper area of 2in$^2$ on a PCB , the LM4866's $\theta_{JA}$ is 41°C/W. At any given ambient temperature $T_{J\backslash A}$, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting PDMAX for PDMAX' results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4866's maximum junction temperature.

$$T_A = T_{JMAX} - 2 \times P_{DMAX} \theta_{JA} \qquad (5)$$

For a typical application with a 5V power supply and an 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 99°C for the LLP package and 45°C for the MTE package.

$$T_{JMAX} = P_{DMAX} \theta_{JA} + T_A \qquad (6)$$

Equation (6) gives the maximum junction temperature $T_{JMAX}$. If the result violates the LM4866's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce $\theta_{JA}$. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the $\theta_{JA}$ is the sum of $\theta_{JC}$, $\theta_{CS}$, and $\theta_{SA}$. ($\theta_{JC}$ is the junction–to–case thermal impedance, $_{CS}$ is the case–to–sink

thermal impedance, and $\theta_{SA}$ is the sink–to–ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

### POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4866's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation in the output signal. Keep the length of leads and traces that connect capacitors between the LM4866's power supply pin and ground as short as possible. Connecting a 1µF capacitor, $C_B$, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise amplifier's click and pop performance. The selection of bypass capacitor values, especially $C_B$, depends on desired PSRR requirements, click and pop performance (as explained in the section, **Proper Selection of External Components**), system cost, and size constraints.

### MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4866's shutdown function. Activate micro-power shutdown by applying $V_{DD}$ to the SHUTDOWN pin. When active, the LM4866's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically $V_{DD}/2$. The low 0.7µA typical shutdown current is achieved by applying a voltage that is as near as $V_{DD}$ as possible to the SHUTDOWN pin. A voltage thrat is less than $V_{DD}$ may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 10kΩ pull-up resistor between the SHUTDOWN pin and $V_{DD}$. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the SHUTDOWN pin to $V_{DD}$ through the pull-up resistor, activating micro-power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

**TABLE 1. LOGIC LEVEL TRUTH TABLE FOR SHUTDOWN OPERATION**

| SHUTDOWN | OPERATIONAL MODE |
|----------|------------------|
| Low | Full power, stereo BTL amplifiers |
| High | Micro-power Shutdown |

## Application Information (Continued)

### SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4866's performance requires properly selecting external components. Though the LM4866 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4866 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the **Audio Power Amplifier Design** section for more information on selecting the proper gain.

### Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor ($C_i$ in *Figure 1*). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size, $C_i$ has an affect on the LM4866's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, $R_f$. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency.

A shown in *Figure 1*, the input resistor ($R_I$) and the input capacitor, $C_I$ produce a –3dB high pass filter cutoff frequency that is found using Equation (7).

$$f_{-3\,dB} = \frac{1}{2\pi R_{IN} C_1}$$

(7)

As an example when using a speaker with a low frequency limit of 150Hz, $C_I$, using Equation (4), is 0.063µF. The 1.0µF $C_I$ shown in *Figure 1* allows the LM4866 to drive high efficiency, full range speaker whose response extends below 30Hz.

### Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of $C_B$, the capacitor connected to the BYPASS pin. Since $C_B$ determines how fast the LM4866 settles to quiescent operation, its value is critical when minimizing turn–on pops. The slower the LM4866's outputs ramp to their quiescent DC voltage (nominally 1/2 $V_{DD}$), the smaller the turn–on pop. Choosing $C_B$ equal to 1.0µF along with a small value of $C_i$ (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing $C_i$ no larger than necessary for the desired bandwidth helps minimize clicks and pops.

### OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4866 contains circuitry to minimize turn-on and shutdown transients or 'clicks and pop'. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4866's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 $V_{DD}$. As soon as the voltage on the BYPASS pin is stable, the device becomes fully operational. Although the bypass pin current cannot be modified, changing the size of $C_B$ alters the device's turn-on time and the magnitude of 'clicks and pops'. Increasing the value of $C_B$ reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of $C_B$ increases, the turn-on time increases. There is a linear relationship between the size of $C_B$ and the turn-on time. Here are some typical turn-on times for various values of $C_B$:

| $C_B$ | $T_{ON}$ |
|---|---|
| 0.01µF | 20 ms |
| 0.1µF | 200 ms |
| 0.22µF | 440 ms |
| 0.47µF | 940 ms |
| 1.0µF | 2 Sec |

In order eliminate 'clicks and pops', all capacitors must be discharged before turn-on. Rapidly switching $V_{DD}$ may not allow the capacitors to fully discharge, which may cause 'clicks and pops'.

### NO LOAD STABILITY

The LM4866 may exhibit low level oscillation when the load resistance is greater than 10kΩ. This oscillation only occurs as the output signal swings near the supply voltages. Prevent this oscillation by connecting a 5kΩ between the output pins and ground.

# Application Information (Continued)

## AUDIO POWER AMPLIFIER DESIGN

### Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

| | |
|---|---|
| Power Output: | $1W_{RMS}$ |
| Load Impedance: | 8Ω |
| Input Level: | $1V_{RMS}$ |
| Input Impedance: | 20kΩ |
| Bandwidth: | 100Hz–20 kHz ± 0.25 dB |

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the **Typical Performance Characteristics** section. Another way, using Equation (4), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the **Typical Performance Characteristics** curves, must be added to the result obtained by Equation (8). The result in Equation (9).

$$V_{opeak} = \sqrt{(2R_L P_O)}$$

(8)

$$V_{DD} \geq (V_{OUTPEAK} + (V_{OD_{TOP}} + V_{OD_{BOT}}))$$

(9)

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4866 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the **Power Dissipation** section.

After satisfying the LM4866's power dissipation requirements, the minimum differential gain is found using Equation (10).

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms}$$

(10)

Thus, a minimum gain of 2.83 allows the LM4866's to reach full output swing and maintain low noise and THD+N performance. For this example, let $A_{VD}$ = 3.

The amplifier's overall gain is set using the input ($R_i$) and feedback ($R_f$) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (11).

$$R_f/R_i = A_{VD}/2$$

(11)

The value of $R_f$ is 30kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one–fifth the lower bandwidth limit and the high frequency response must extend to at least

five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz$$

(12)

and an

$$F_H = 20kHzx5 = 100kHz$$

(13)

As mentioned in the **External Components** section, $R_i$ and $C_i$ create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation (14).

$$C_i \geq \frac{1}{2\pi R_i f_c}$$

(14)

the result is

$$1/(2\pi * 20kΩ * 20Hz) = 0.398\mu F$$

(15)

Use a 0.39μF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain, $A_{VD}$, determines the upper passband response limit. With $A_{VD}$ = 3 and $f_H$ = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the LM4866's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-lrestricting bandwidth limitations.

## RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figures 2 through 6 show the recommended four-layer PC board layout that is optimized for the 24-pin LQ-packaged LM4866 and associated external components. Figures 7 through 11 show the recommended four-layer PC board layout that is optimized for the 20-pin MTE-packaged LM4866 and associated components. Figures 12 through 14 show the recommended two-layer PC board layout that is optimized for the 20-pin MT-packaged LM4866 and associated components. These circuits are designed for use with an external 5V supply and 3Ω (or greater) speakers for the LQ- and MTE-packaged LM4866 and 4Ω (or greater) speakers for the MT-packaged LM4866.

This circuit board is easy to use. Apply 5V and ground to the board's $V_{DD}$ and GND pads, respectively. Connect speakers between the board's -OUTA and +OUTA and OUTB and +OUTB pads. Apply the stereo input signal to the input pins labeled '-INA' and '-INB.' The stereo input signal's ground references are connected to the respective input channel's 'GND' pin, adjacent to the input pins.
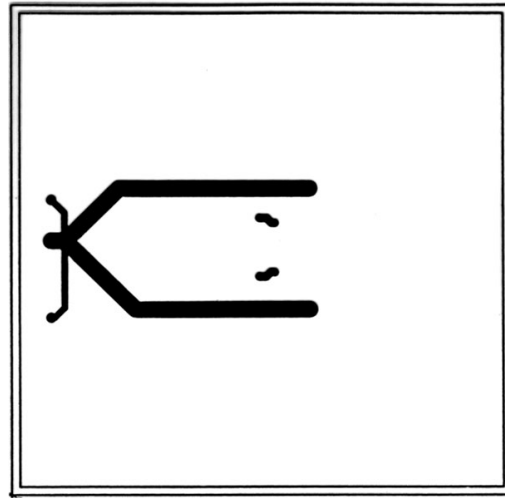
## Application Information (Continued)
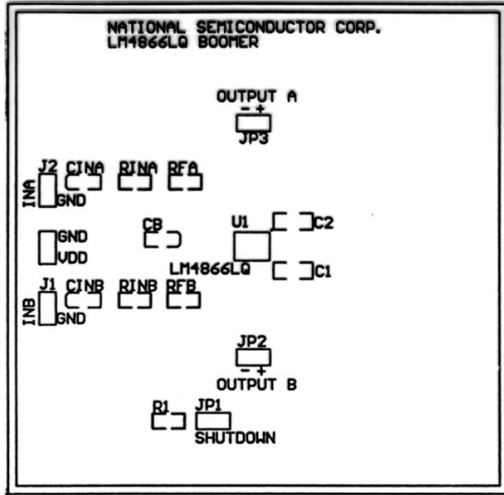


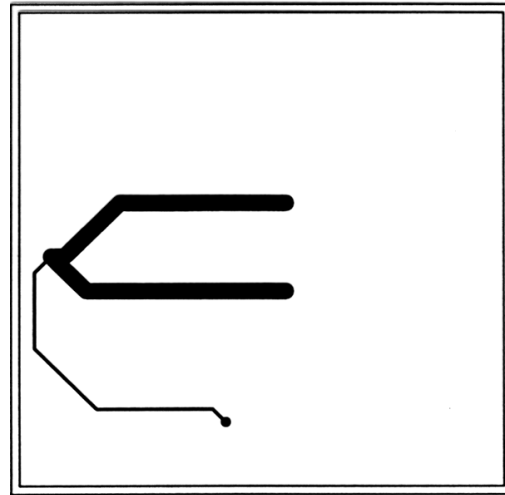FIGURE 2. Recommended LQ PC board layout:
Component-side Silkscreen
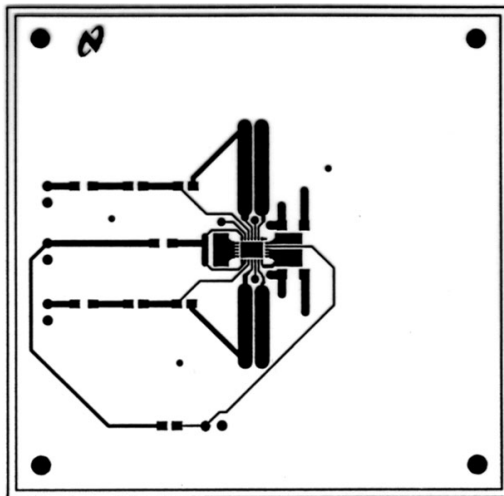


FIGURE 3. Recommended LQ PC board layout:
Component-side layout
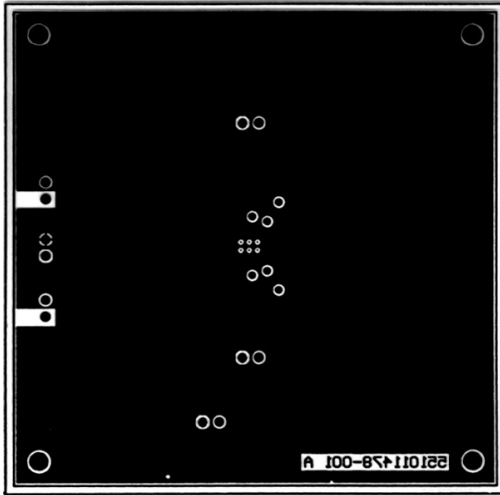


FIGURE 4. Recommended LQ PC board layout:
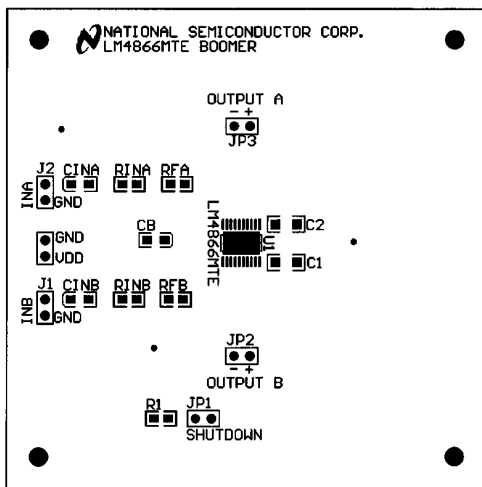upper inner-layer layout



FIGURE 5. Recommended LQ PC board layout:
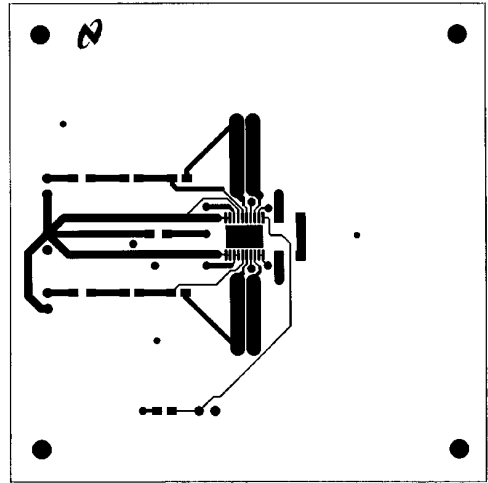lower inner-layer layout

# Application Information (Continued)



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**FIGURE 6. Recommended LQ PC board layout:
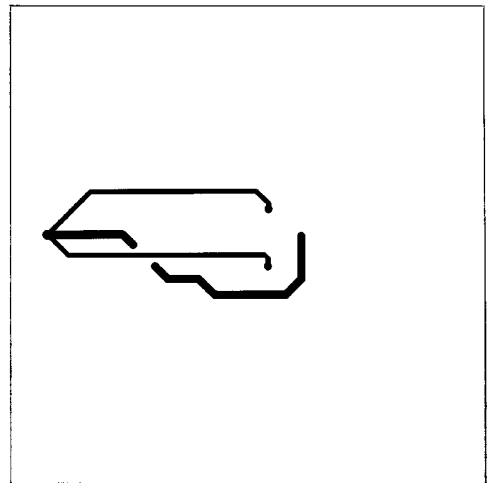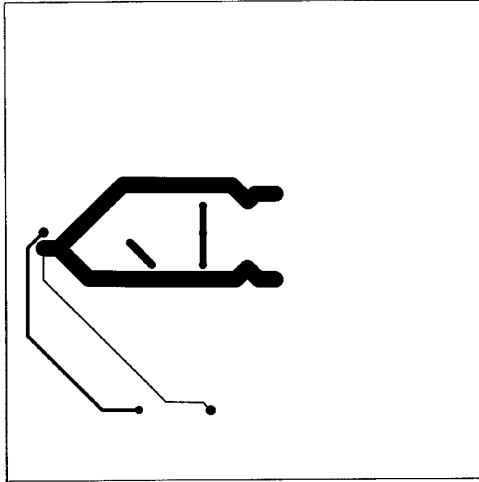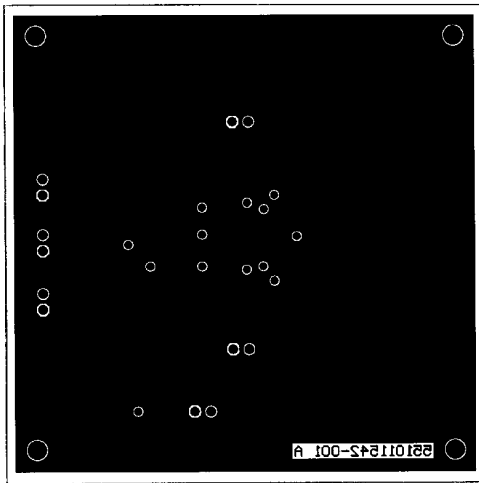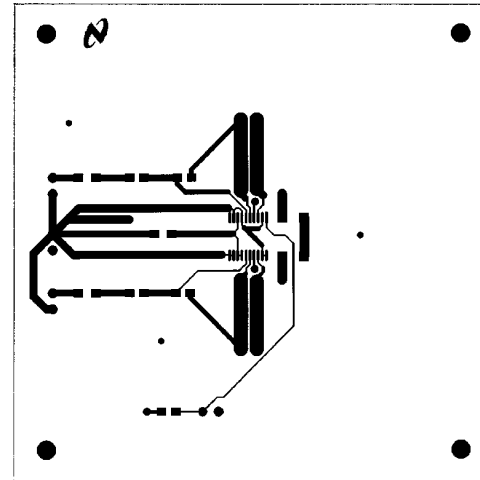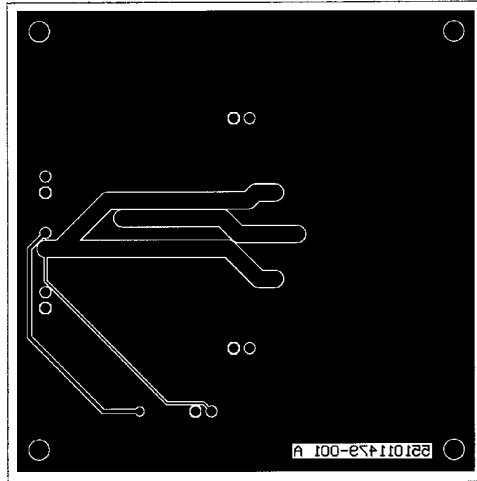bottom-side layout**



20018645

**FIGURE 8. Recommended MTE PC board layout:
component-side layout**



20018644

**FIGURE 7. Recommended MTE board layout:
component-side silkscreen**



20018646

**FIGURE 9. Recommended MTE board layout:
upper inner-layer layout**

# Application Information  (Continued)



20018647

**FIGURE 10. Recommended MTE PC board layout: lower inner-layer layout**



20018648

**FIGURE 11. Recommended MTE board layout: bottom-side layout**
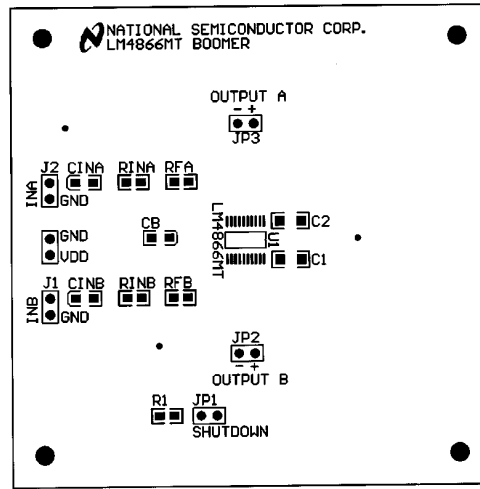


20018649

**FIGURE 12. Recommended MT PC board layout: component-side silkscreen**
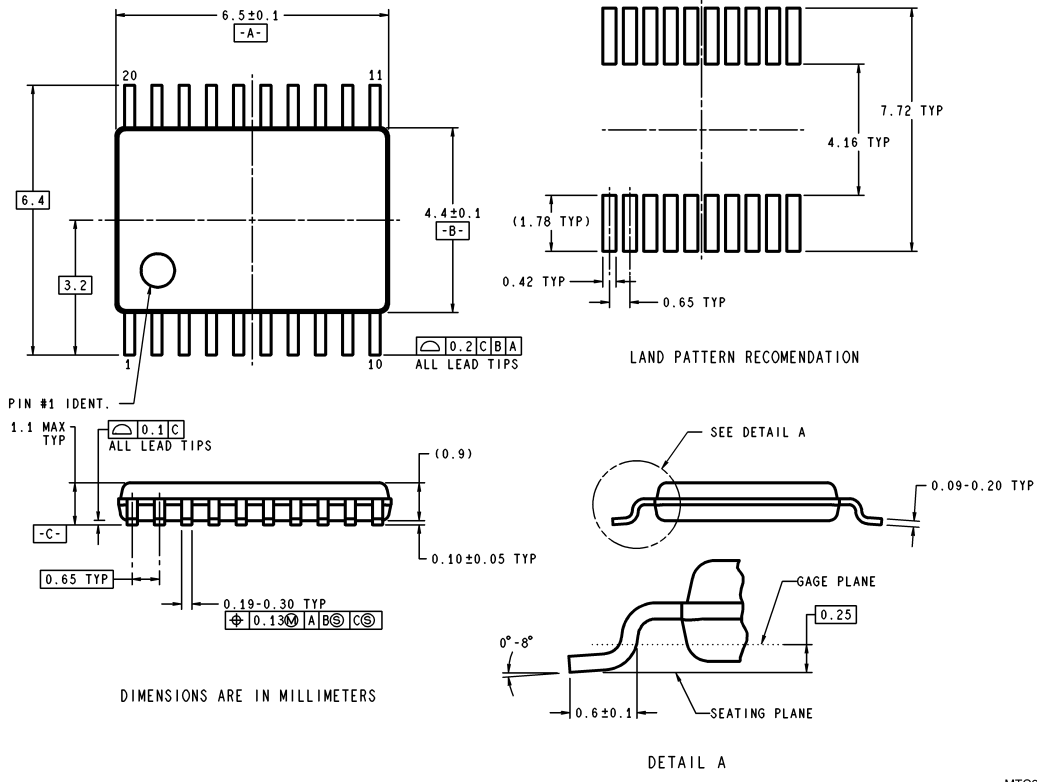


20018651

**FIGURE 13. Recommended MT board layout: component-side layout**

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# Application Information (Continued)



20018650

**FIGURE 14. Recommended MT PC board layout:
bottom-side layout**

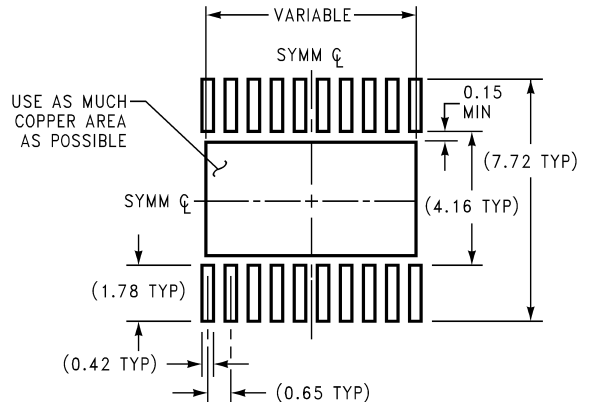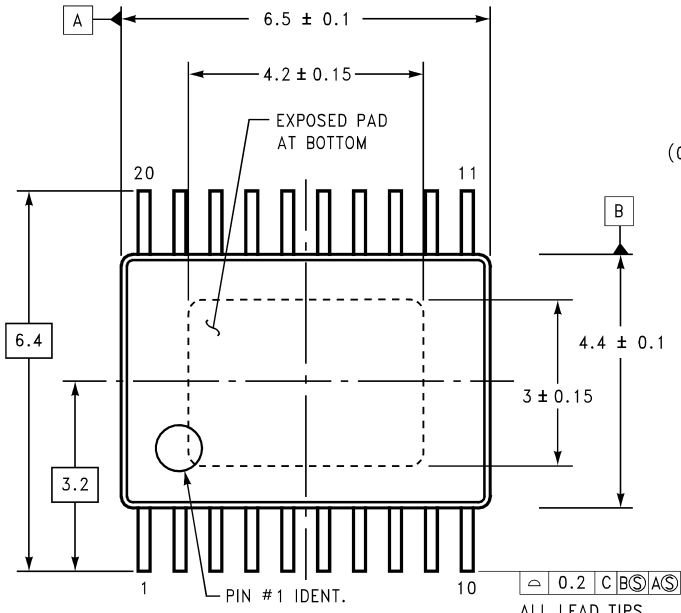# Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMENDATION

DIMENSIONS ARE IN MILLIMETERS

DETAIL A

MTC20 (Rev D)

**20-Lead Molded PKG, TSSOP, JEDEC, 4.4mm BODY WIDTH**
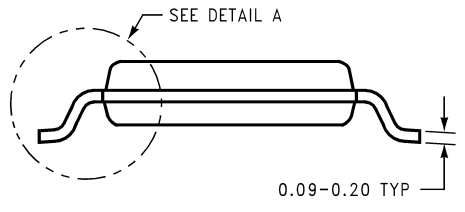**Order Number LM4866MT**
**NS Package Number MTC20**

www.national.com

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

VARIABLE

SYMM ℄

USE AS MUCH
COPPER AREA
AS POSSIBLE

0.15 MIN

(7.72 TYP)

SYMM ℄

(4.16 TYP)

A

6.5 ± 0.1

4.2 ± 0.15

EXPOSED PAD
AT BOTTOM

(1.78 TYP)

(0.42 TYP)

(0.65 TYP)

LAND PATTERN RECOMMENDATION

20                    11

B

6.4

4.4 ± 0.1

3 ± 0.15

(12°) TOP
AND BOTTOM

R0.09 MIN

GAGE PLANE

R0.09 MIN

0.25

3.2

0°–8°

0.6 ± 0.1

(1)

SEATING PLANE

DETAIL A
TYPICAL, SCALE: 40X

1      PIN #1 IDENT.      10

⌒ 0.2 C B(S) A(S)
ALL LEAD TIPS

⌒ 0.1 C
ALL LEAD TIPS

SEE DETAIL A

(0.9)

1.1 MAX TYP

C

0.65 TYP

0.1 ± 0.05 TYP

0.19 – 0.30 TYP

⊕ 0.1(M) C B(S) A(S)

0.09–0.20 TYP
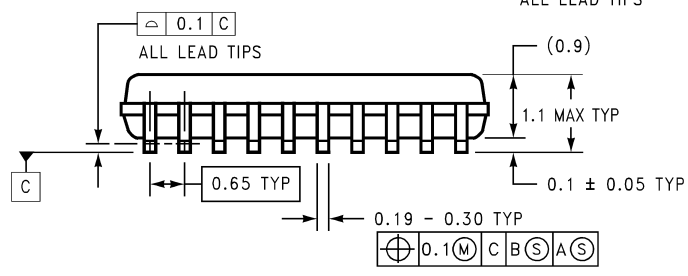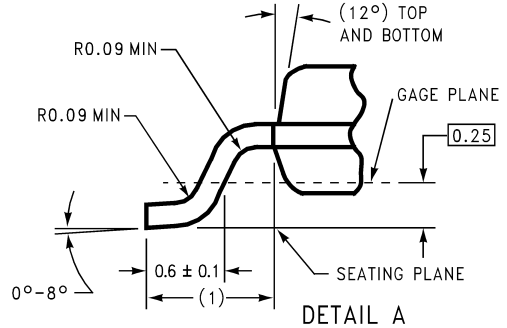
MXA20A (REV A)

**20-Lead Molded TSSOP, Exposed Pad, 6.5x4.4x0.9mm**
**Order Number LM4866MTE**
**NS Package Number MXA20A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

(24X 0.4)
(24X 0.25)
(4)
(2.4)
(3)
(20X 0.5)
(3.4)
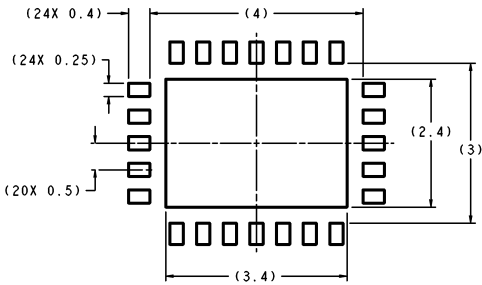
RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS

PIN 1 INDEX AREA

4±0.1

5±0.1

0.8 MAX

(0.2)

PIN 1 ID

3.4±0.1

0.1 MAX ALL AROUND

24

2

20

8

2.4±0.1

12

19

13

24X 0.25±0.05

0.1 M C A Ⓢ B Ⓢ

0.5

3

24X 0.4±0.1
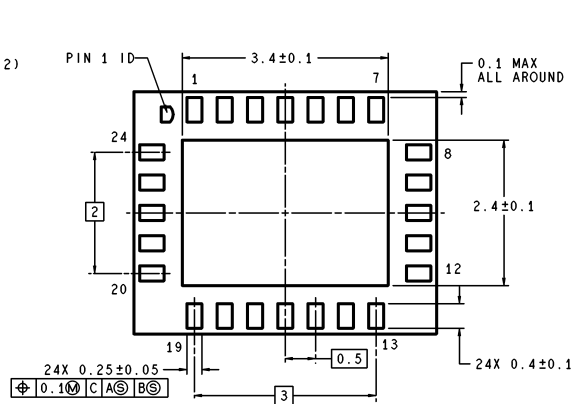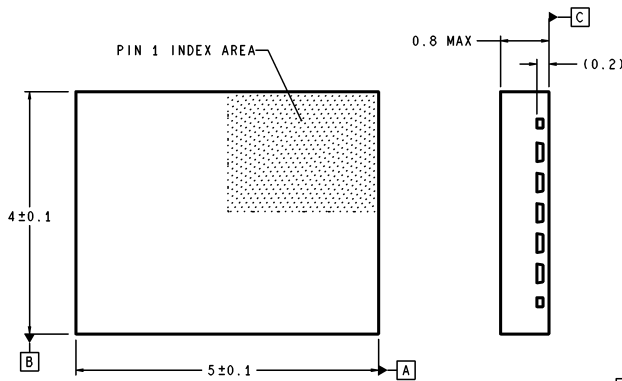
LQA24A (Rev A)

**24-Lead Molded pkg, Leadframe Package LLP**
**Order Number LM4866LQ**
**NS Package Number LQA24A**

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.