DATA SHEET

74ALVC164245

16-bit dual supply translating transceiver (3-State)

Product specification
Supersedes data of 1995 Jul 01
IC24 Data Handbook

1998 Aug 26

Philips Semiconductors

PHILIPS

16-bit dual supply translating transceiver (3-State) 74ALVC164245

FEATURES

- Wide supply voltage range
  - A port: 1.2 to 3.6V
  - B port: 1.2 to 5.5V
- Complies with JEDEC standard no. 8-1A
- Control inputs voltage range from 2.7V to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74ALVC164245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC164245 is a 16-bit (dual-octal) translating transceiver and is designed to interface between a 5V bus and 3V bus in a mixed 3V/5V supply environment. This device can be used as two 8-bit transceivers or one 16-bit transceiver. The direction control inputs (1DIR, 2DIR) determine the direction of the data flow. nDIR (active HIGH) enables data from nA ports to nB ports. nDIR (active LOW) enables data from nB ports to nA ports. The output enable inputs ($1\overline{OE}$, $2\overline{OE}$), when HIGH, disable both nA and nB ports by placing them in a high impedance OFF-state. The nB ports interface with the 5V bus. The nA ports interface with the 3V bus. In suspend mode, when one of the supply voltages is zero, there will be no current flow from the non zero supply towards the zero supply. $V_{CC1} \geq V_{CC2}$ (except in suspend mode).

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nB nB to nA	C_L = 50pF V_{CC1} = 5.0V V_{CC2} = 3.3V	 3.7 3.1	ns
C_I	Input capacitance		5	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance	V_I = GND to V_{CC}[1]	20	pF

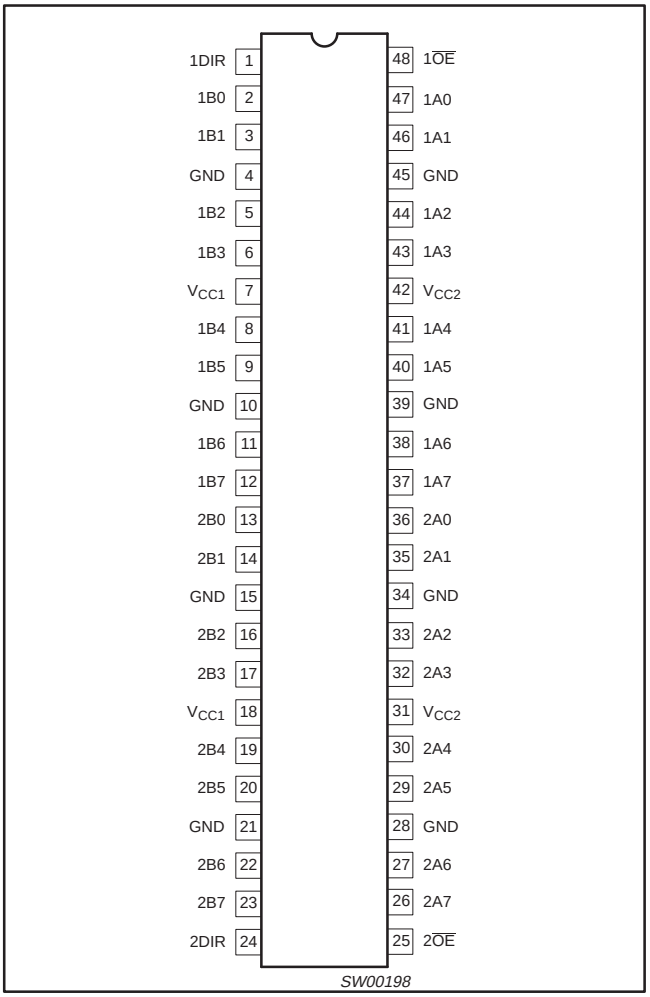
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVC164245 DL	AC164245 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVC164245 DGG	AC164245 DGG	SOT362-1

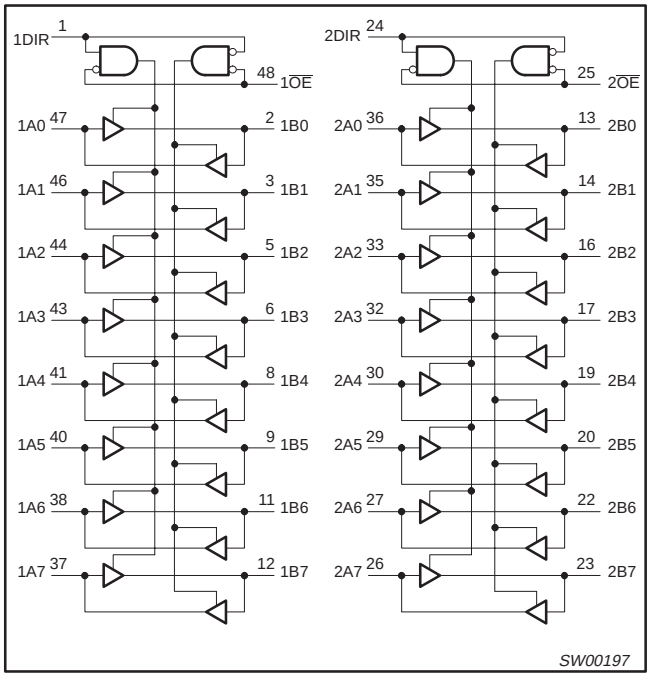
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	Direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	GND
7, 18	V_{CC1}	Positive supply voltage (5V bus)
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	Data inputs/outputs
24	2DIR	Direction control
25	$2\overline{OE}$	Output enable input (active LOW)
26, 27, 29, 30, 32, 33, 35, 36	2A7 to 2A0	Data inputs/outputs
31, 42	V_{CC2}	Positive supply voltage (3V bus)
37, 38, 40, 41, 43, 44, 46, 47	1A7 to 1A0	Data inputs/outputs
48	$1\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

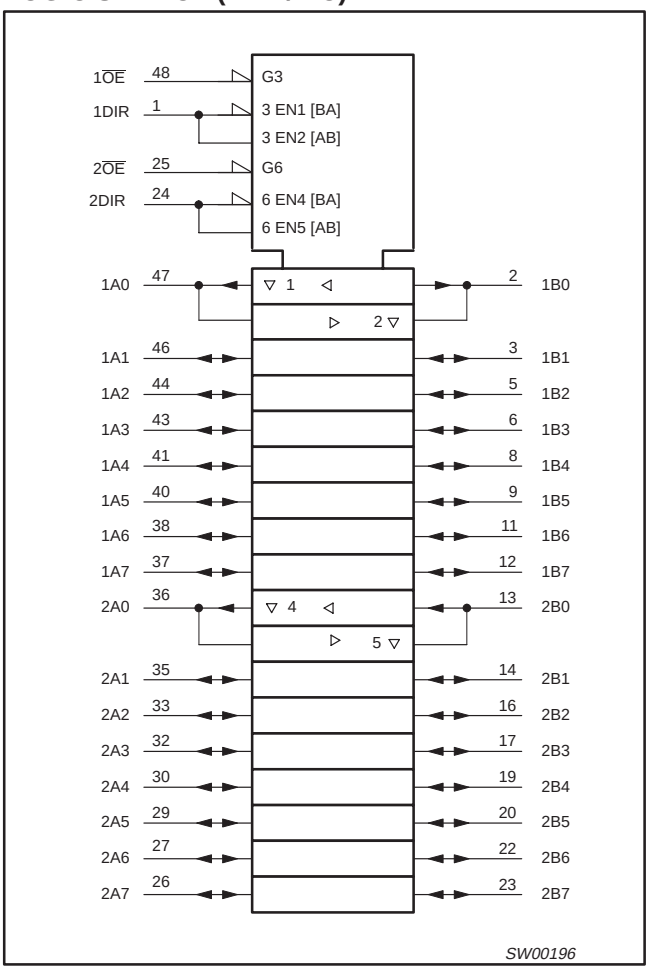


FUNCTION TABLE

INPUTS		OUTPUTS	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC1}	DC supply voltage (B Port)		–0.5 to +6.0	V
V_{CC2}	DC supply voltage (A Port)		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 3	–0.5 to +5.5	V
$V_{I/O}$	DC input voltage range for I/Os		–0.5 to V_{CC} +0.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 3	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–60 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink SO (SSOP) –plastic mini-pack (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC1}	DC supply voltage (for max. speed performance) (B Port)	$V_{CC1} \geq V_{CC2}$	2.7	5.5	V
V_{CC2}	DC supply voltage (for max. speed performance) (A Port)	$V_{CC1} \geq V_{CC2}$	2.7	3.6	V
V_{CC1}	DC supply voltage (for low-voltage applications) (B Port)	$V_{CC1} \geq V_{CC2}$	1.5	5.5	V
V_{CC2}	DC supply voltage (for low-voltage applications) (A Port)	$V_{CC1} \geq V_{CC2}$	1.5	3.6	V
V_I	DC Input voltage range		0	5.5	V
$V_{I/O}$	DC Input voltage range for I/Os	A Port	0	V_{CC2}	V
$V_{I/O}$	DC Output voltage range for I/Os	B Port	0	V_{CC1}	V
V_0	DC Output voltage range	A Port	0	V_{CC2}	V
V_0	DC Output voltage range	B Port	0	V_{CC1}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC2} = 2.7 to 3.0V V_{CC2} = 3.0 to 3.6V V_{CC1} = 3.0 to 4.5V V_{CC1} = 4.5 to 5.5V	0 0 0 0	20 10 20 10	ns/V

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage (B Port)	V_{CC} = 4.5 to 5.5V (Note 2)	2.0			V
	HIGH level Input voltage (A Port)	V_{CC} = 2.7 to 3.6V (Note 2)	2.0			
V_{IL}	LOW level Input voltage (B Port)	V_{CC} = 4.5 to 5.5V (Note 2)			0.8	V
	LOW level Input voltage (A Port)	V_{CC} = 2.7 to 3.6V (Note 2)			0.8	
V_{OH}	HIGH level output voltage (B Port)	V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			
	HIGH level output voltage (A Port)	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0			
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC}		
V_{OL}	LOW level output voltage (B Port)	V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	
	LOW level output voltage (A Port)	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND Control pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins (B Port)	V_{CC} = 5.5V; V_I = V_{CC} or GND		±0.1	±15	µA
	Input current for common I/O pins (A Port)	V_{CC} = 3.6V; V_I = V_{CC} or GND		±0.1	±15	
I_{CC}	Quiescent supply current (B Port)	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0		0.2	40	µA
	Quiescent supply current (A Port)	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.2	40	
ΔI_{CC}	Additional quiescent supply current per input pin (B Port)	V_{CC} = 4.5V to 5.5V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA
	Additional quiescent supply current per control pin (A Port)	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	

NOTES:
1. All typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V and T_{amb} = 25°C.
2. If V_{CC2} <2.7V, the switching levels at all inputs are not TTL compatible.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

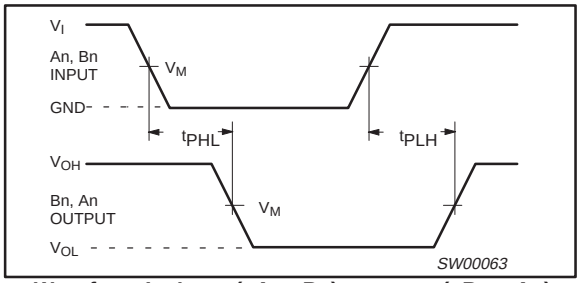
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC1} = 5.0V ±0.5V V_{CC2} = 3.3V ±0.3V		V_{CC1} = 5.0V ±0.5V V_{CC2} = 2.7V		
			MIN	MAX	MIN	MAX	
t_{PHL} t_{PLH}	Propagation delay nAn to nBn	1	1	5.8		5.9	ns
t_{PHL} t_{PLH}	Propagation delay nBn to nAn	1	1.2	5.8		6.7	ns
t_{PZH} t_{PZL}	3-State output enable time n$\overline{OE}$ to nAn	2	1	8.9		9.3	ns
t_{PZH} t_{PZL}	3-State output enable time n$\overline{OE}$ to nBn	2	2.1	9.5		9.2	ns
t_{PHZ} t_{PLZ}	3-State output disable time n$\overline{OE}$ to nAn	2	2	9.1		10.2	ns
t_{PHZ} t_{PLZ}	3-State output disable time n$\overline{OE}$ to nBn	2	2.9	8.6		9	ns

NOTE:

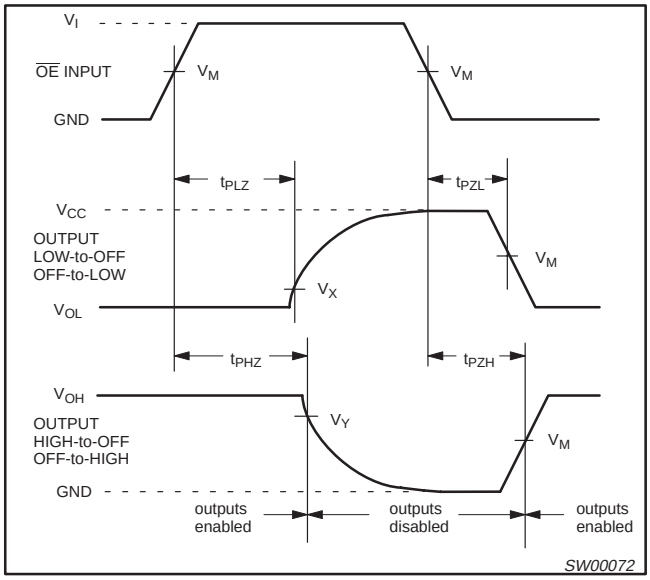
1. All typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V and T_{amb} = 25°C.
2. All typical values are at V_{CC1} = 5.0V, V_{CC2} = 2.7V and T_{amb} = 25°C.

AC WAVEFORMS

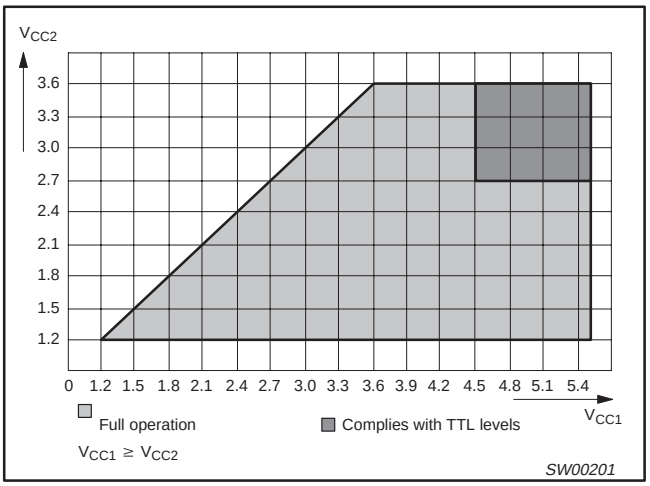
V_M = 1.5V at $V_{CC} \leq$ 3.6V
V_M = 0.5 * V_{CC1} at $V_{CC1} \geq$ 4.5V.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \leq$ 3.6V
$V_X = V_{OL}$ + 0.1 * ($V_{OH} - V_{OL}$) at $V_{CC1} \geq$ 4.5V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \leq$ 3.6V
$V_Y = V_{OH} - 0.1$ * ($V_{OH} - V_{OL}$) at $V_{CC1} \geq$ 4.5V
V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load.



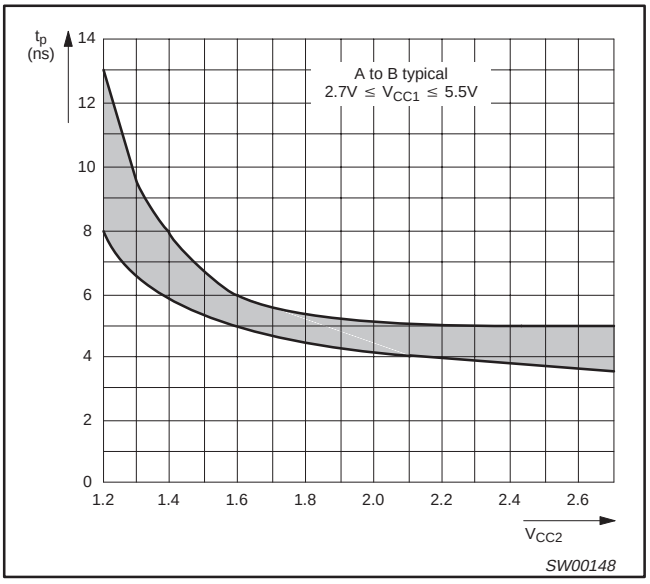
Waveform 1. Input (nAn,nBn) to output (nBn, nAn) propagation delays



Waveform 2. 3-State enable and disable times

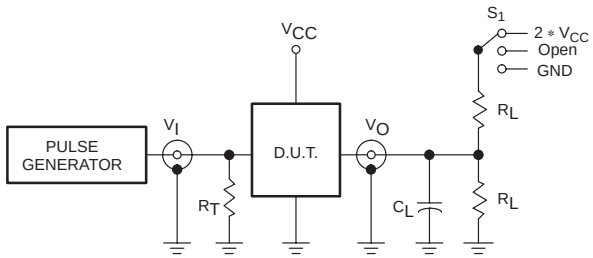


Waveform 3. Supply operating area



Waveform 4. Propagation delay as a function of the supply voltage, V_{CC2}

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 * V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC1}	V_{CC2}	V_I
< 2.7V	< 2.7V	V_{CC}
2.7 – 5.5V	2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor

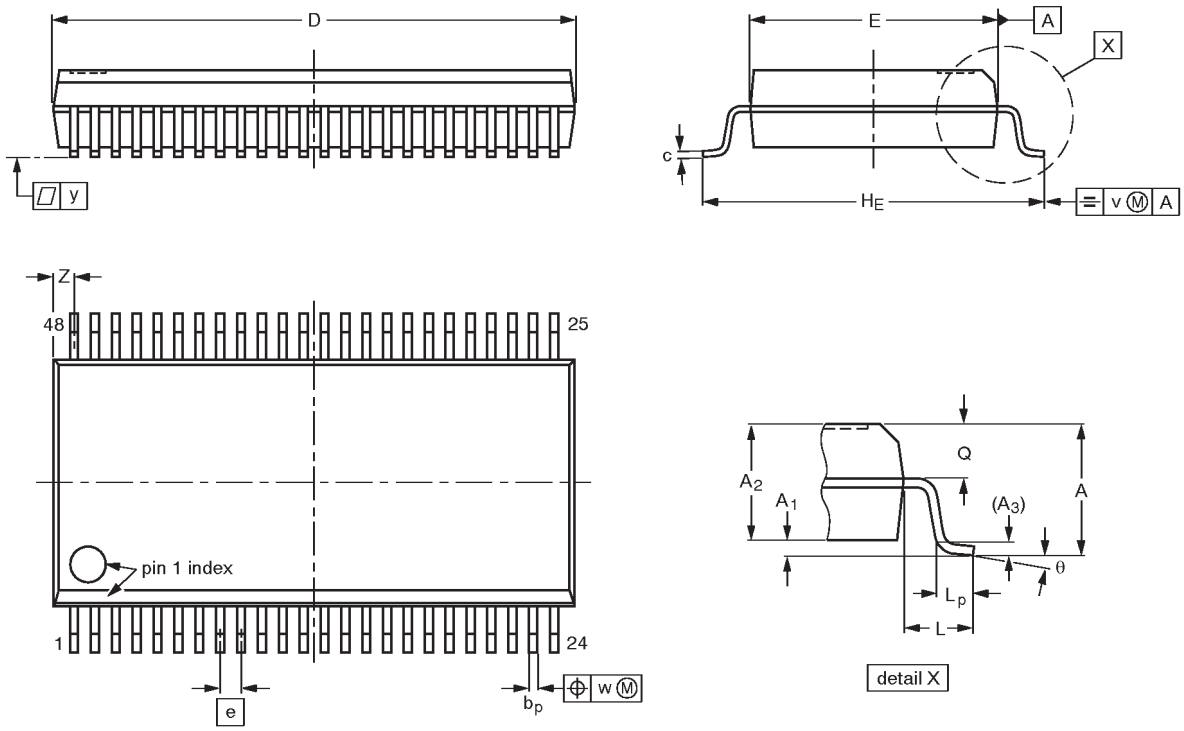
C_L = Load capacitance includes jig and probe capacitance

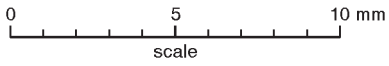
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00330

Waveform 5. Load circuitry for switching times

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**





DIMENSIONS (mm are the original dimensions)

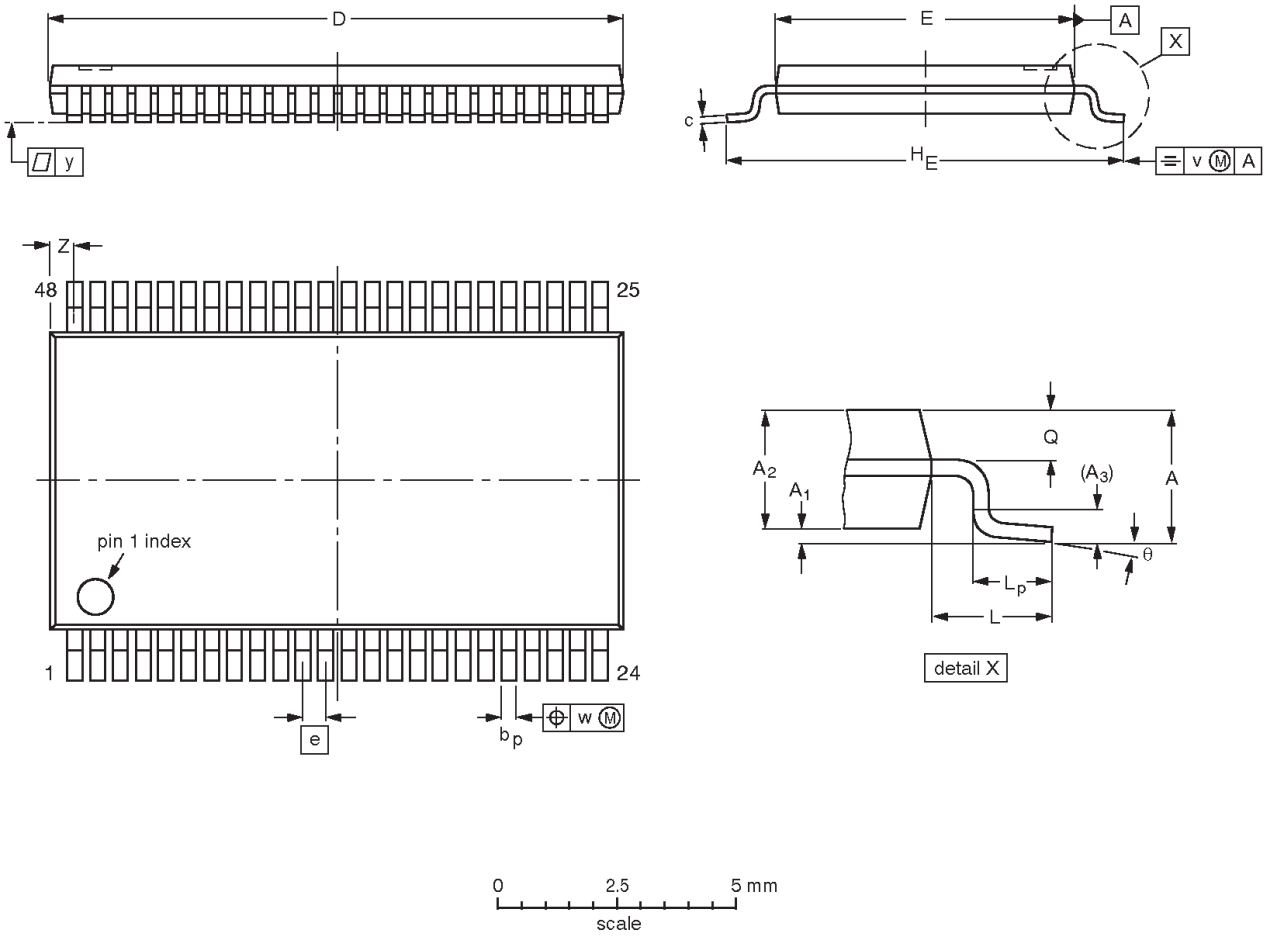
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					~~93-02-03~~ 95-02-10

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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