

## 74ALVC16373

### Low Voltage 16-Bit Transparent Latch with 3.6V Tolerant Inputs and Outputs

#### General Description

The ALVC16373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear to be transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in a high impedance state.

The 74ALVC16373 is designed for low voltage (1.1V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The 74ALVC16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- 1.1V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$  ( $I_n$  to  $O_n$ )
  - 3.5 ns max for 3.0V to 3.6V  $V_{CC}$
  - 3.9 ns max for 2.3V to 2.7V  $V_{CC}$
  - 6.8 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Support live insertion and withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

**Note 1:** To ensure the high-impedance state during power up or power down, OE should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

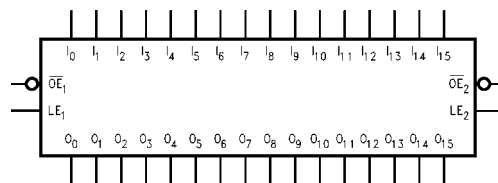
#### Ordering Code:

Order Number	Package Number	Package Description
74ALVC16373GX (Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74ALVC16373MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

**Note 2:** BGA package available in Tape and Reel only.

**Note 3:** Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

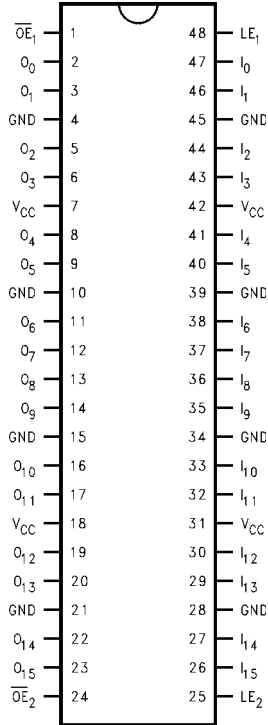
#### Logic Symbol



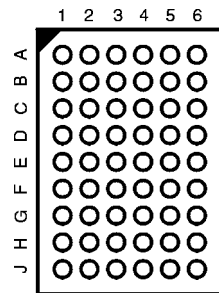
74ALVC16373 Low Voltage 16-Bit Transparent Latch with 3.6V Tolerant Inputs and Outputs

### Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$LE_n$	Latch Enable Input
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs
NC	No Connect

### FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	$O_0$	NC	$\overline{OE}_1$	$LE_1$	NC	$I_0$
<b>B</b>	$O_2$	$O_1$	NC	NC	$I_1$	$I_2$
<b>C</b>	$O_4$	$O_3$	$V_{CC}$	$V_{CC}$	$I_3$	$I_4$
<b>D</b>	$O_6$	$O_5$	GND	GND	$I_5$	$I_6$
<b>E</b>	$O_8$	$O_7$	GND	GND	$I_7$	$I_8$
<b>F</b>	$O_{10}$	$O_9$	GND	GND	$I_9$	$I_{10}$
<b>G</b>	$O_{12}$	$O_{11}$	$V_{CC}$	$V_{CC}$	$I_{11}$	$I_{12}$
<b>H</b>	$O_{14}$	$O_{13}$	NC	NC	$I_{13}$	$I_{14}$
<b>J</b>	$O_{15}$	NC	$\overline{OE}_2$	$LE_2$	NC	$I_{15}$

### Truth Tables

Inputs			Outputs
$LE_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

Inputs			Outputs
$LE_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

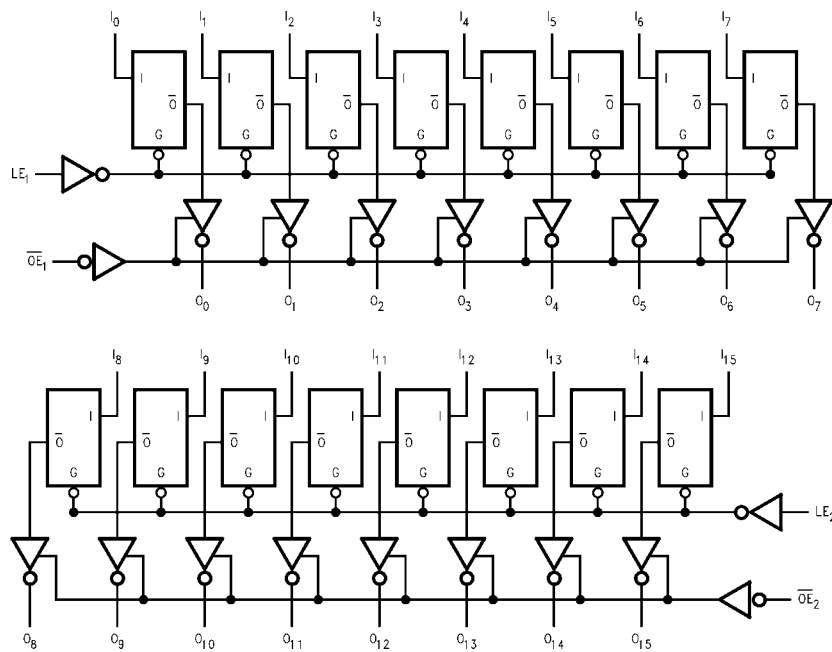
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, inputs may not float)  
 Z = High Impedance  
 $O_0$  = Previous  $O_0$  before HIGH-to-LOW of Latch Enable

## Functional Description

The 74ALVC16373 contains sixteen edge D-type latches with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ( $LE_n$ ) input is HIGH, data on the  $I_n$  enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time

its I input changes. When  $LE_n$  is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition on  $LE_n$ . The 3-STATE outputs are controlled by the Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW the standard outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 4)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to 4.6V
Output Voltage ( $V_O$ ) (Note 5)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ ) $V_O < 0V$	-50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 6)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ ) $V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V

**Note 4:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 5:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 6:** Floating or unused inputs must be held HIGH or LOW.

**DC Electrical Characteristics**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	$0.65 \times V_{CC}$ 1.7 2.0		V
$V_{IL}$	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		$0.35 \times V_{CC}$ 0.7 0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -6 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	1.65 - 3.6 1.65 2.3 2.7 3.0 3.0	$V_{CC} - 0.2$ 1.2 2 1.7 2.2 2.4		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 6 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	1.65 - 3.6 1.65 2.3 2.3 2.7 3		0.2 0.45 0.4 0.7 0.4 0.55	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		$\pm 10$	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	$\mu A$

AC Electrical Characteristics										
Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω								Units
		C <sub>L</sub> = 50 pF				C <sub>L</sub> = 30 pF				
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus to Bus	1.3	3.5	1.5	3.9	1.0	3.4	1.5	6.8	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay LE to Bus	1.3	3.5	1.5	4.4	1.0	3.9	1.5	7.8	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	1.3	4.0	1.5	5.1	1.0	4.6	1.5	9.2	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	1.3	4.0	1.5	4.3	1.0	3.8	1.5	6.8	ns
Capacitance										
Symbol	Parameter		Conditions	T <sub>A</sub> = +25°C		Units				
				V <sub>CC</sub>	Typical					
C <sub>IN</sub>	Input Capacitance		V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	6	pF				
C <sub>OUT</sub>	Output Capacitance		V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	7	pF				
C <sub>PD</sub>	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C <sub>L</sub> = 50 pF	3.3	20	pF				
				2.5	20					

## AC Loading and Waveforms

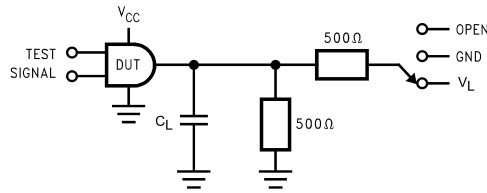


FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_L$
$t_{PZH}$ , $t_{PHZ}$	GND

TABLE 2. Variable Matrix  
(Input Characteristics:  $f = 1\text{MHz}$ ;  $t_r = t_f = 2\text{ns}$ ;  $Z_0 = 50\Omega$ )

Symbol	$V_{CC}$			
	$3.3\text{V} \pm 0.3\text{V}$	2.7V	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
$V_Y$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
$V_L$	6V	6V	$V_{CC} * 2$	$V_{CC} * 2$

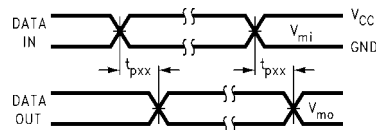


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

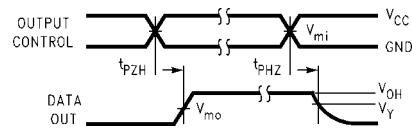


FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

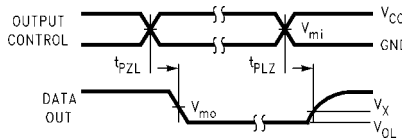


FIGURE 4. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

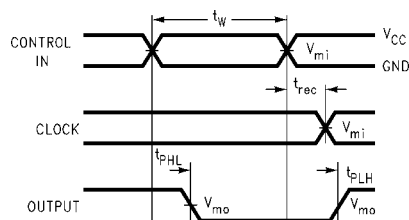


FIGURE 5. Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms

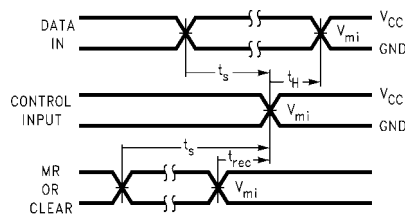
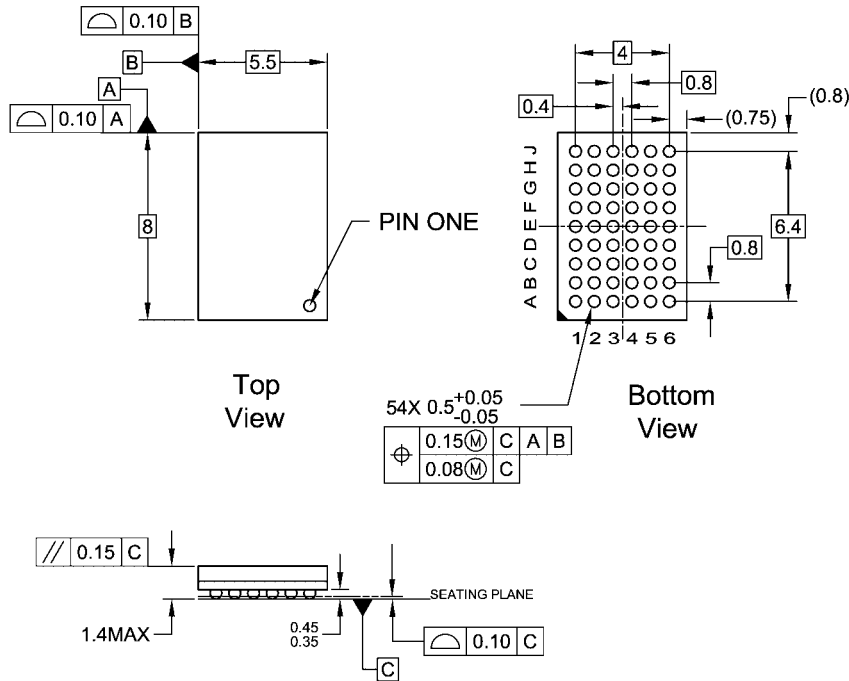


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

**Physical Dimensions** inches (millimeters) unless otherwise noted



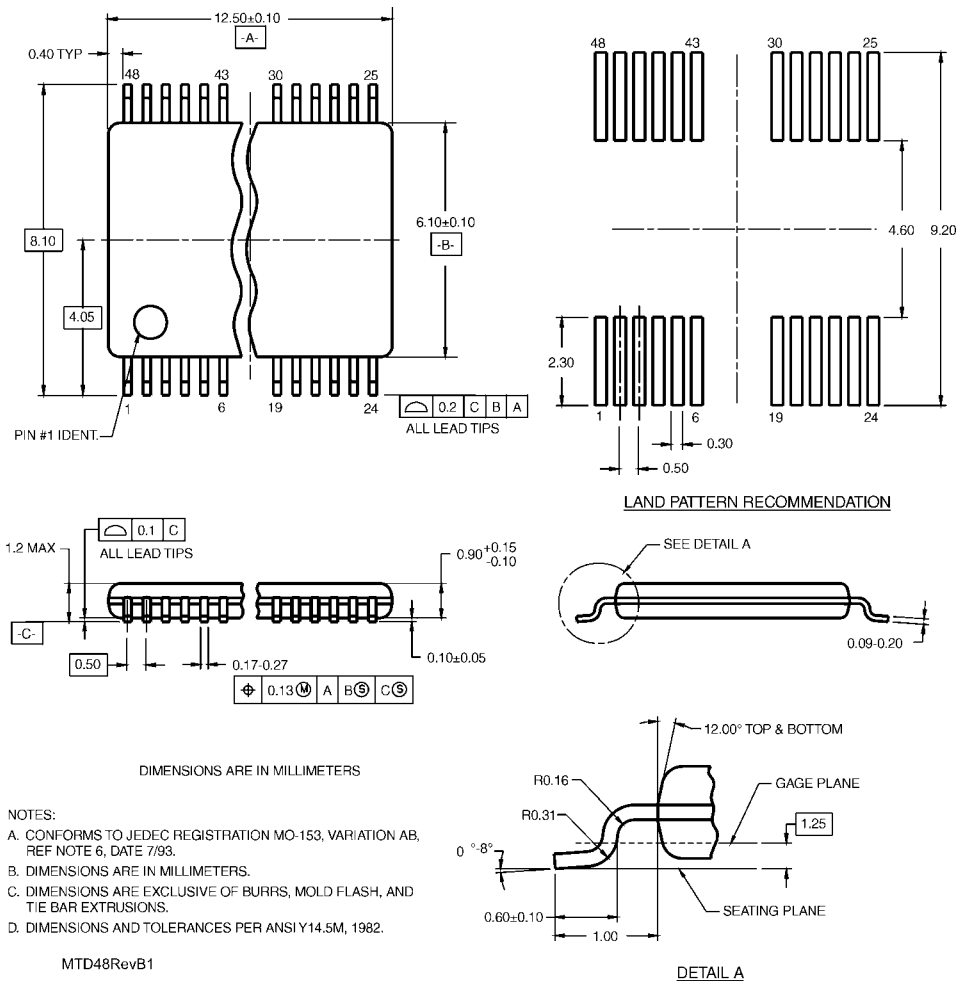
**NOTES:**

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide  
Package Number BGA54A  
(Preliminary)**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)