

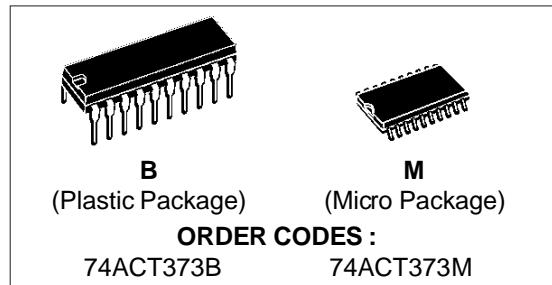
OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT NON INVERTING

- HIGH SPEED: $t_{PD} = 6 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 8 \mu A$ (MAX.) at $T_A = 25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS
 $V_{IH} = 2V$ (MIN), $V_{IL} = 0.8V$ (MAX)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 373
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The ACT373 is an advanced high-speed CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power applications maintaining high speed operation similar to equivalent Bipolar Schottky TTL.

These 8 bit D-Type latch are controlled by a latch enable input (LE) and an output enable input (\overline{OE}).



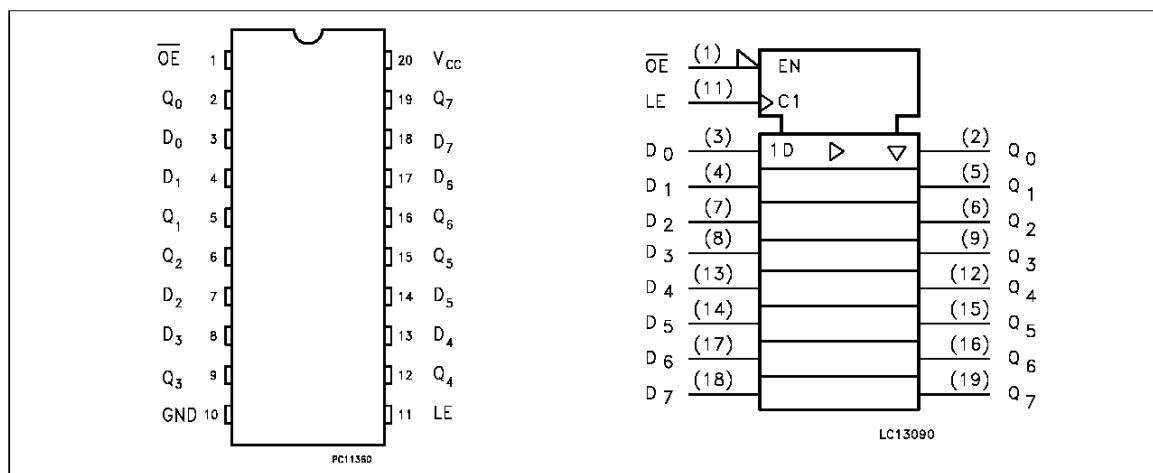
(\overline{OE}).

While the LE inputs is held at a high level, the Q outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the (\overline{OE}) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

This device is designed to interface directly High Speed CMOS systems with TTL and NMOS components.

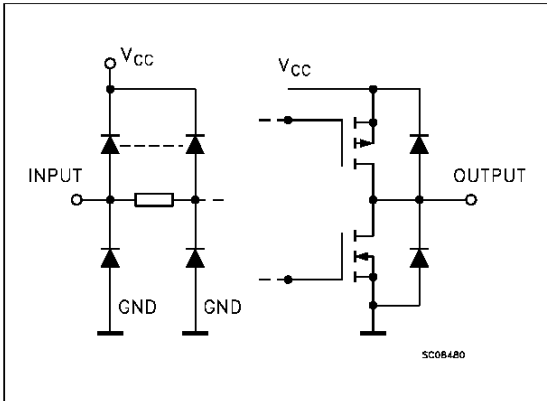
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



74ACT373

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

| PIN No | SYMBOL | NAME AND FUNCTION |
|----------------------------|-----------------|--|
| 1 | \overline{OE} | 3 State Output Enable Input (Active LOW) |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q0 to Q7 | Data Inputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0 to D7 | 3 State Outputs |
| 11 | LE | Latch Enable Input |
| 10 | GND | Ground (0V) |
| 20 | V _{CC} | Positive Supply Voltage |

TRUTH TABLE

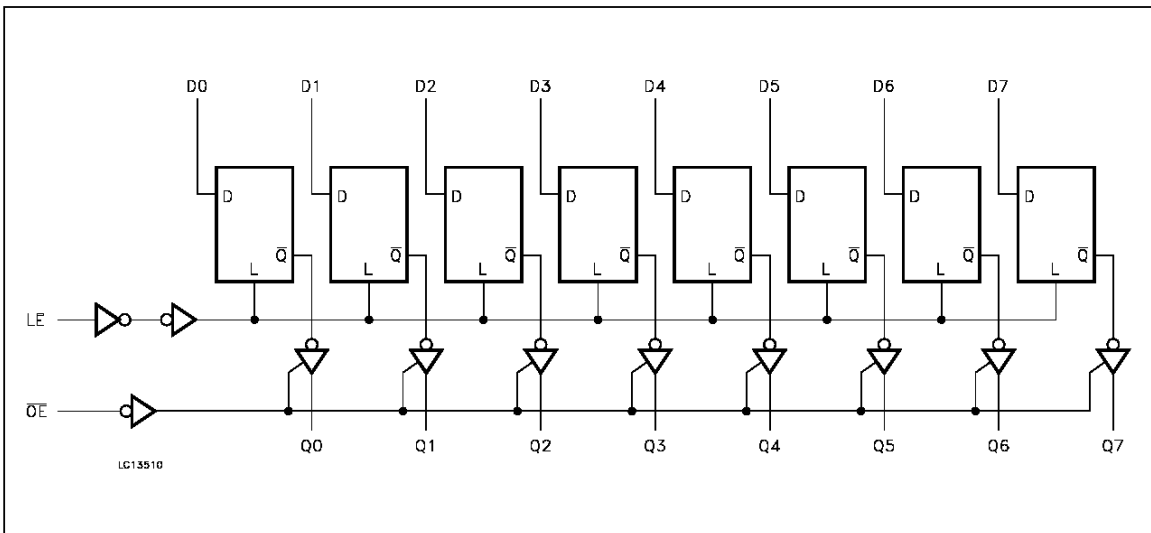
| \overline{OE} | INPUTS | | OUTPUTS |
|-----------------|--------|---|-------------|
| | LE | D | Q |
| H | X | X | Z |
| L | L | X | NO CHANGE * |
| L | H | L | L |
| L | H | H | H |

X: DONT CARE

Z: HIGH IMPEDANCE

*: Q OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

LOGIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-------------------------------------|--------------------------------------|-------------------------------|------|
| V _{CC} | Supply Voltage | -0.5 to +7 | V |
| V _I | DC Input Voltage | -0.5 to V _{CC} + 0.5 | V |
| V _O | DC Output Voltage | -0.5 to V _{CC} + 0.5 | V |
| I _{IK} | DC Input Diode Current | ± 20 | mA |
| I _{OK} | DC Output Diode Current | ± 20 | mA |
| I _O | DC Output Current | ± 50 | mA |
| I _{CC} or I _{GND} | DC V _{CC} or Ground Current | ± 400 | mA |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _L | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|-----------------|---|----------------------|------|
| V _{CC} | Supply Voltage | 4.5 to 5.5 | V |
| V _I | Input Voltage | 0 to V _{CC} | V |
| V _O | Output Voltage | 0 to V _{CC} | V |
| T _{op} | Operating Temperature: | -40 to +85 | °C |
| dt/dv | Input Rise and Fall Time V _{CC} = 4.5 to 5.5V (note 1) | 8 | ns/V |

1) V_{IN} from 0.8 V to 2.0 V

DC SPECIFICATIONS

| Symbol | Parameter | Test Conditions | | Value | | | | | Unit | |
|-------------------|---------------------------------------|-----------------|--|-------------------------|-------------------------|------------------------|--------------|------|------|------|
| | | | | T _A = 25 °C | | | -40 to 85 °C | | | |
| | | | | V _{CC} (V) | Min. | Typ. | Max. | Min. | | Max. |
| V _{IH} | High Level Input Voltage | 4.5 | V _O = 0.1 V or V _{CC} - 0.1 V | 2.0 | 1.5 | | 2.0 | | V | |
| | | 5.5 | | 2.0 | 1.5 | | 2.0 | | | |
| V _{IL} | Low Level Input Voltage | 4.5 | V _O = 0.1 V or V _{CC} - 0.1 V | | 1.5 | 0.8 | | 0.8 | V | |
| | | 5.5 | | | 1.5 | 0.8 | | 0.8 | | |
| V _{OH} | High Level Output Voltage | 4.5 | V _I (*) = V _{IH} or V _{IL} | I _O = -50 μA | 4.4 | 4.49 | | 4.4 | V | |
| | | 5.5 | | | 5.4 | 5.49 | | 5.4 | | |
| | | 4.5 | | | I _O = -24 mA | 3.86 | | | | 3.76 |
| | | 5.5 | | | | 4.86 | | | | 4.76 |
| V _{OL} | Low Level Output Voltage | 4.5 | V _I (*) = V _{IH} or V _{IL} | I _O = 50 μA | | 0.001 | 0.1 | 0.1 | V | |
| | | 5.5 | | | I _O = 50 mA | | 0.001 | 0.1 | | 0.1 |
| | | 4.5 | | | | I _O = 24 mA | | | | 0.36 |
| | | 5.5 | | | | | | | | 0.36 |
| I _I | Input Leakage Current | 5.5 | V _I = V _{CC} or GND | | | | ±0.1 | ±1 | μA | |
| I _{OZ} | 3 State Output Leakage Current | 5.5 | V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND | | | | ±0.5 | ±5 | μA | |
| I _{CCCT} | Max I _{CC} /Input | 5.5 | V _I = V _{CC} -2.1 V | | 0.6 | | | 1.5 | mA | |
| I _{CC} | Quiescent Supply Current | 5.5 | V _I = V _{CC} or GND | | | 8 | | 80 | μA | |
| I _{OLD} | Dynamic Output Current (note 1, 2) | 5.5 | V _{OLD} = 1.65 V max | | | | | 75 | mA | |
| I _{OHD} | | | V _{OHD} = 3.85 V min | | | | | -75 | mA | |

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50 Ω.

(*) All outputs loaded.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 3 \text{ ns}$)

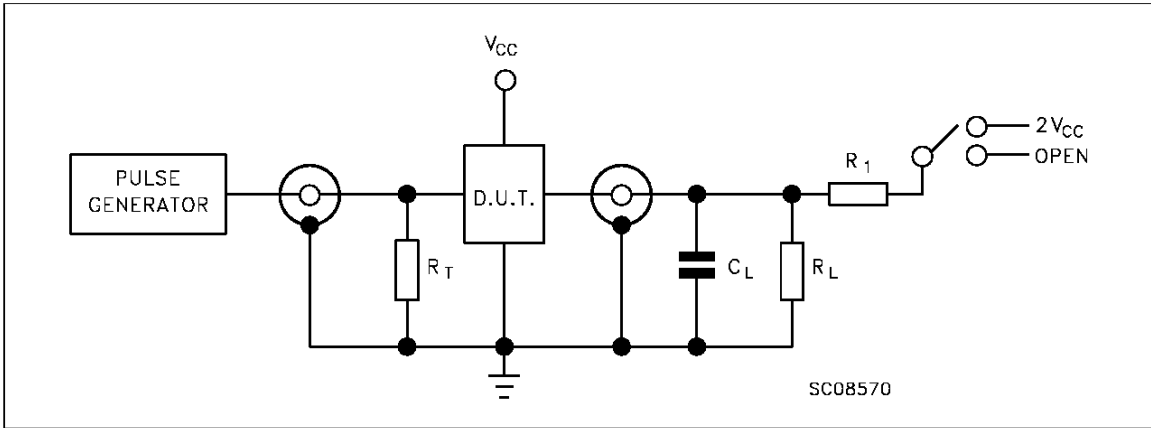
| Symbol | Parameter | Test Condition | | Value | | | | | Unit | |
|------------------------|-----------------------------------|----------------|--|-----------------|-----------------------------------|------|------|---|------|------|
| | | | | V_{CC} (V) | $T_A = 25 \text{ }^\circ\text{C}$ | | | $-40 \text{ to } 85 \text{ }^\circ\text{C}$ | | |
| | | | | | Min. | Typ. | Max. | Min. | | Max. |
| t_{PLH} t_{PHL} | Propagation Delay Time LE to Q | $5.0^{(*)}$ | | | 6.0 | 10.0 | | 11.5 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay Time D to Q | $5.0^{(*)}$ | | | 5.5 | 10.0 | | 11.5 | ns | |
| t_{PZL} t_{PZH} | Output Enable Time | $5.0^{(*)}$ | | | 6.0 | 9.5 | | 10.5 | ns | |
| t_{PLH} t_{PHL} | Output Disable Time | $5.0^{(*)}$ | | | 7.0 | 11.0 | | 12.5 | ns | |
| t_w | CK Pulse Width, HIGH or LOW | $5.0^{(*)}$ | | | 1.0 | 7.0 | | 8.0 | ns | |
| t_s | Setup Time Q to CK HIGH or LOW | $5.0^{(*)}$ | | | 0.5 | 7.0 | | 8.0 | ns | |
| t_h | Hold Time Q to CK HIGH or LOW | $5.0^{(*)}$ | | | 0.5 | 0.0 | | 1.0 | ns | |

(*) Voltage range is $5V \pm 0.5V$ **CAPACITIVE CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | | Value | | | | | Unit | |
|-----------|---|-----------------|--|-----------------|-----------------------------------|------|------|---|------|------|
| | | | | V_{CC} (V) | $T_A = 25 \text{ }^\circ\text{C}$ | | | $-40 \text{ to } 85 \text{ }^\circ\text{C}$ | | |
| | | | | | Min. | Typ. | Max. | Min. | | Max. |
| C_{OUT} | Output Capacitance | 5.0 | | | 10 | | | | pF | |
| C_{IN} | Input Capacitance | 5.0 | | | 5 | | | | pF | |
| C_{PD} | Power Dissipation Capacitance (note 1) | 5.0 | | | 25 | | | | pF | |

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/n$ (per circuit)

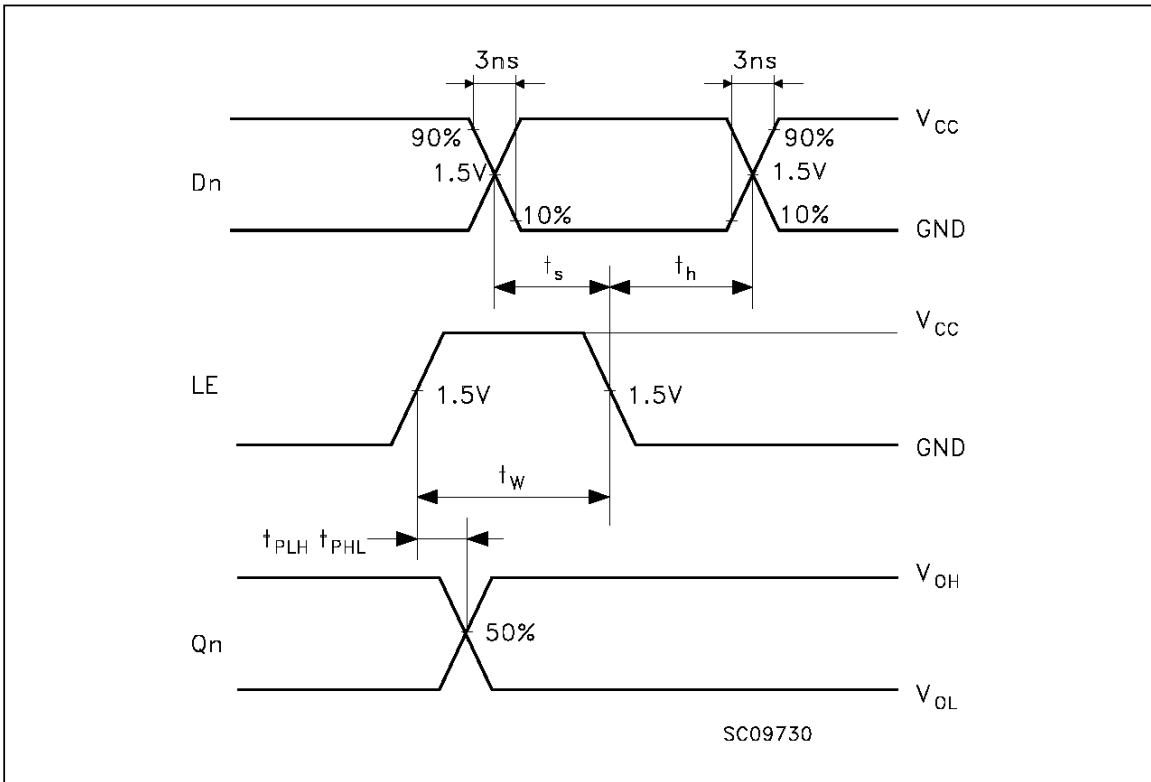
TEST CIRCUIT

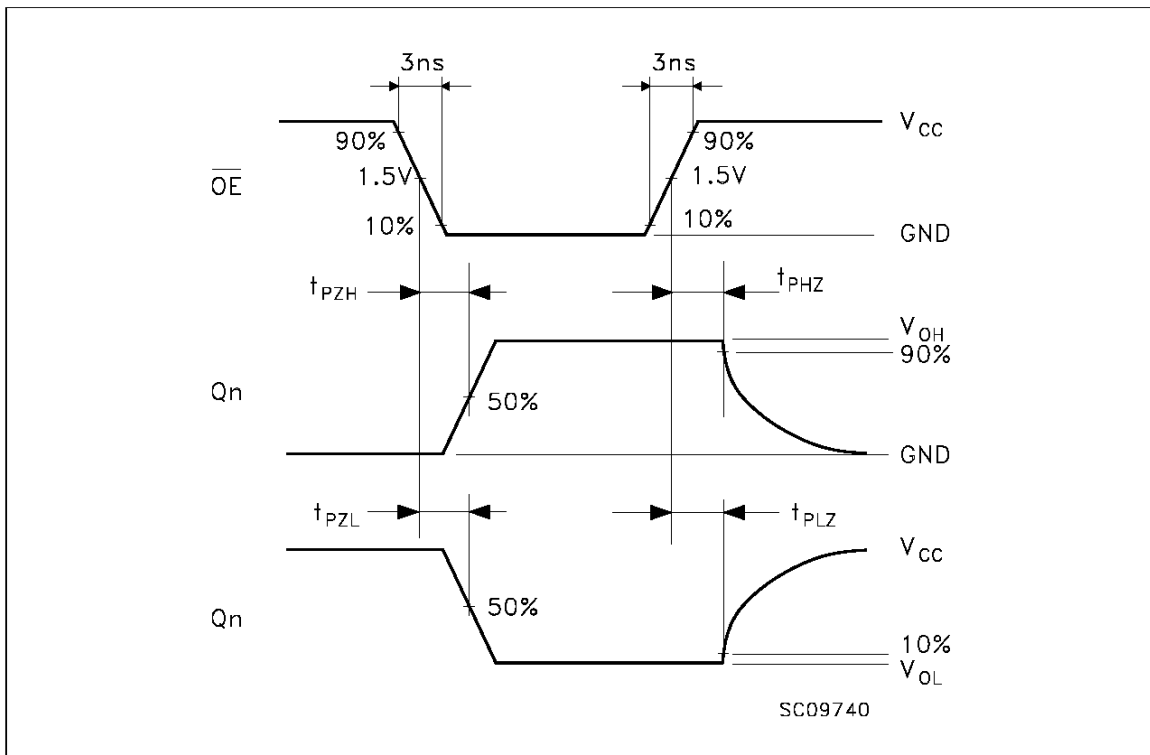
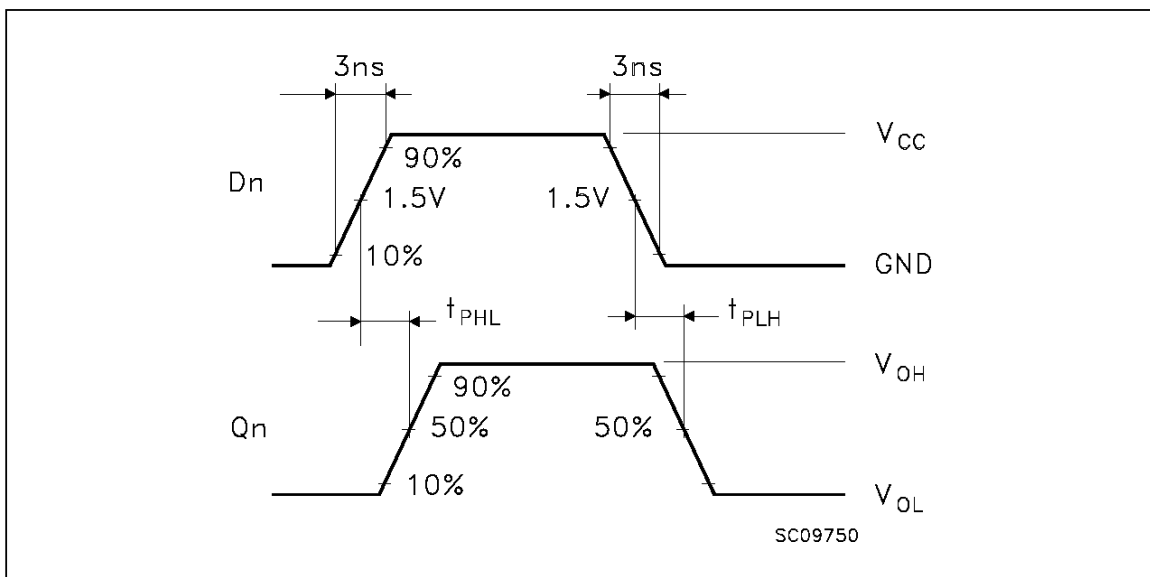


| TEST | SWITCH |
|-----------------------|-----------|
| t_{PLH} , t_{PHL} | Open |
| t_{PZL} , t_{PLZ} | $2V_{CC}$ |
| t_{PZH} , t_{PHZ} | Open |

$C_L = 50$ pF or equivalent (includes jig and probe capacitance)
 $R_L = R_1 = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

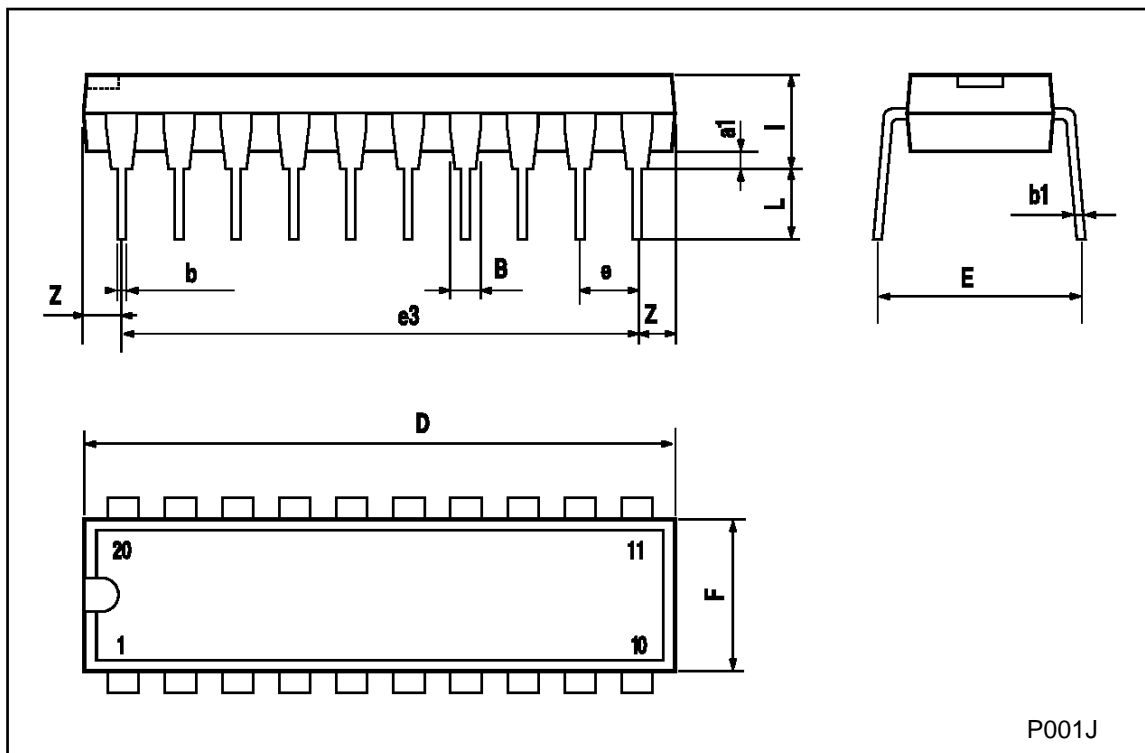
WAVEFORM 1: LE TO Q_n PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, D_n TO LE SETUP AND HOLD TIMES ($f=1$ MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 3: PROPAGATION DELAY TIME** ($f=1\text{MHz}$; 50% duty cycle)

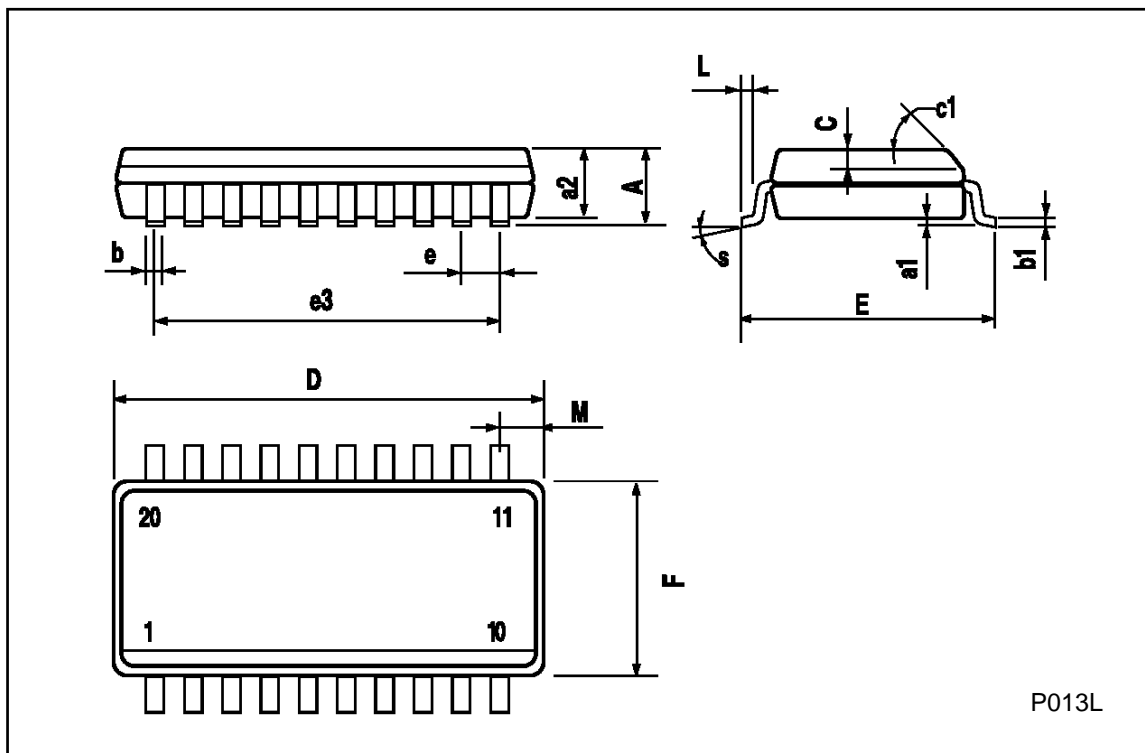
| |
|---|
| Plastic DIP20 (0.25) MECHANICAL DATA |
|---|

| DIM. | mm | | | inch | | |
|------|-------|-------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.254 | | | 0.010 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| b | | 0.45 | | | 0.018 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 25.4 | | | 1.000 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 22.86 | | | 0.900 | |
| F | | | 7.1 | | | 0.280 |
| l | | | 3.93 | | | 0.155 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.34 | | | 0.053 |



SO20 MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|------------|-------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.10 | | 0.20 | 0.004 | | 0.007 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.013 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.50 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 12.60 | | 13.00 | 0.496 | | 0.512 |
| E | 10.00 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 11.43 | | | 0.450 | |
| F | 7.40 | | 7.60 | 0.291 | | 0.299 |
| L | 0.50 | | 1.27 | 0.19 | | 0.050 |
| M | | | 0.75 | | | 0.029 |
| S | 8° (max.) | | | | | |



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