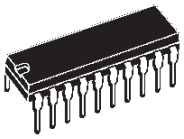
74ACT299

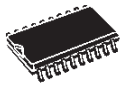
8 BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

PRELIMINARY DATA

- HIGH SPEED:
  f_{MAX} = 170 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION:
  I_{CC} = 8 µA (MAX.) at T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN), V_{IL} = 0.8V (MAX)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24 mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 299
- IMPROVED LATCH-UP IMMUNITY



B
(Plastic Package)



M
(Micro Package)

ORDER CODES :

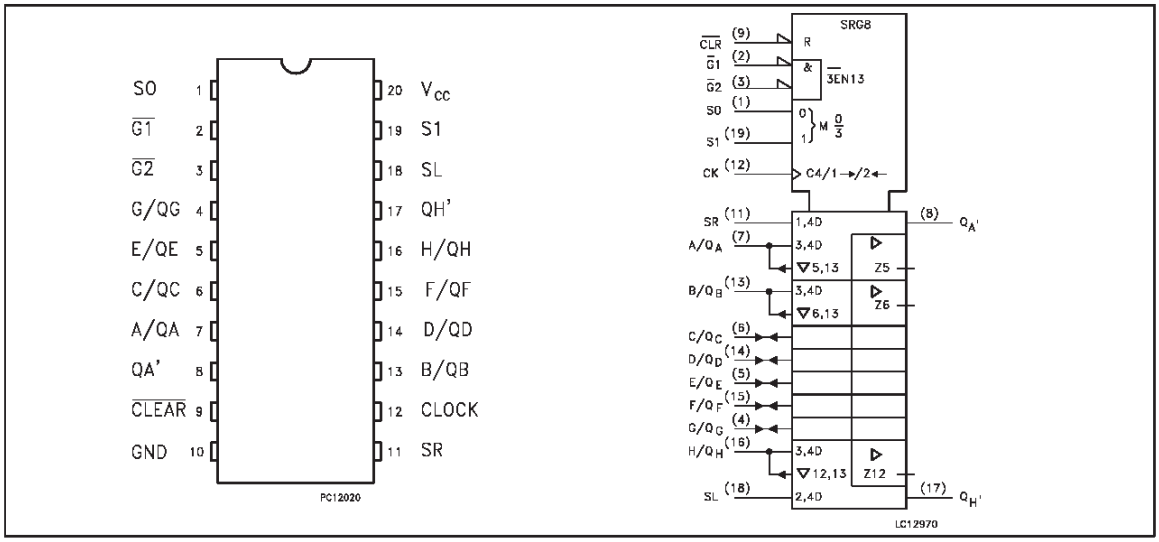
74ACT299B 74ACT299M

DESCRIPTION

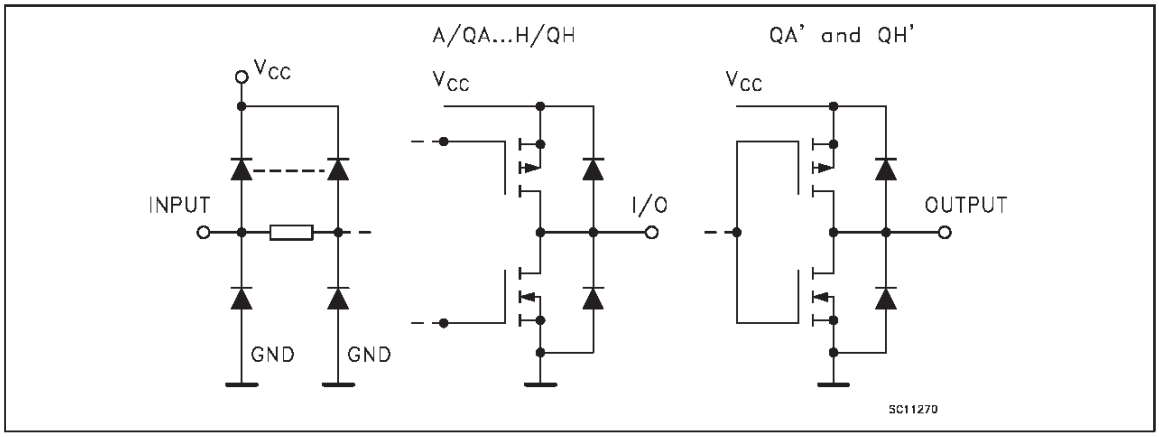
The ACT299 is an high-speed CMOS 8-BIT PIPO SHIFT REGISTERS (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power applications mantaining high speed operation similar to equivalent Bipolar Schottky TTL.

These devices have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1) as shown in the Truth Table.
When one or both enable inputs, ($\overline{G1}$, $\overline{G2}$) are high, the eight input/output terminals are in the high-impedance state ; however sequential operation or clearing of the register is not affected. Clear function is synchronous to clock.
The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

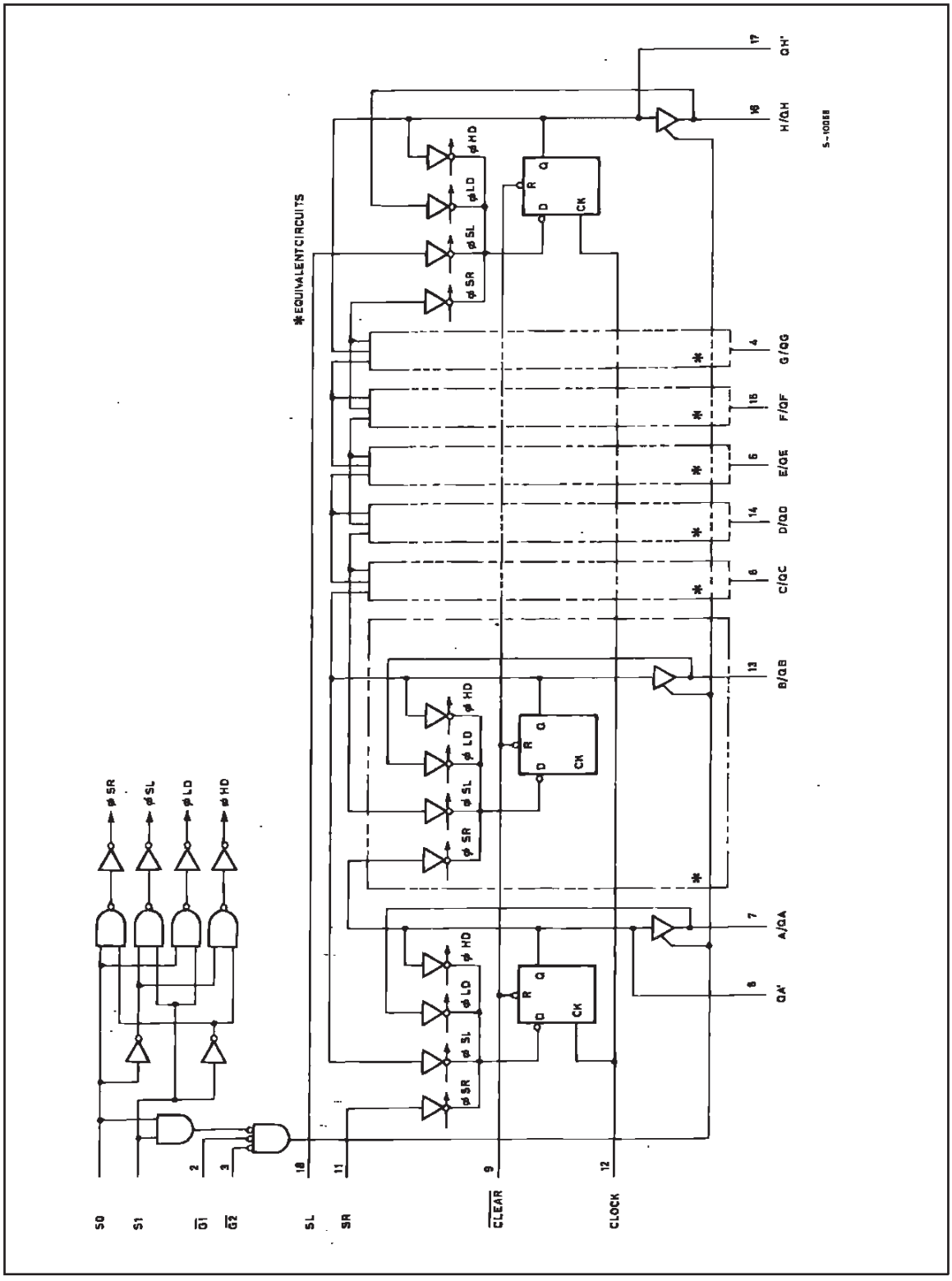
PIN No	SYMBOL	NAME AND FUNCTION
1, 19	S0, S1	Mode Select Inputs
2, 3	$\overline{G1}$, $\overline{G2}$	3 State Output Enable Inputs (Active LOW)
7, 13, 6, 14, 5, 15, 4, 16	A/QA to H/QH	Parallel Data Inputs or 3 State Parallel Outputs (Bus Driver)
8, 17	QA' to QH'	Serial Outputs (Standard Output)
9	$\overline{CLEAR}$	Asynchronous Master Reset Input (Active LOW)
11	SR	Serial Data Shift Right Input
12	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
18	SL	Serial Data Shift Left Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

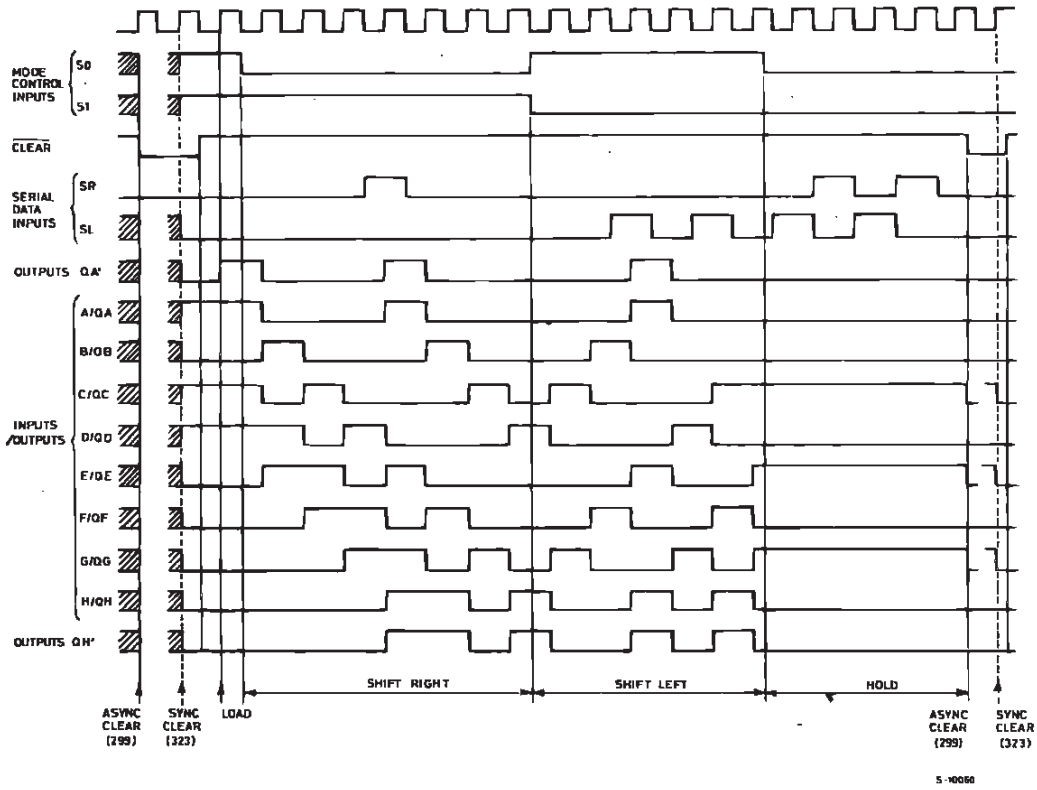
MODE	INPUTS						INPUTS/OUTPUTS				OUTPUTS	
	$\overline{CLEAR}$	FUNCTION SELECTED		OUTPUT CONTROL		CLOCK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G1}$*	$\overline{G2}$*		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	⎍	X	H	H	QGn	H	QGn
	H	L	H	L	L	⎍	X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	⎍	H	X	QBn	H	QBn	H
	H	H	L	L	L	⎍	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	⎍	X	X	a	h	a	h

* When one or both output controls are high, the eight, input/output terminals are the high impedanc e state: howewer sequential operation or clearing of the register is not affected.
Z : HIGH IMPEDANCE
Qn0 : THE LEVEL OF An BEFORE THE INDICATED STEADY STATE INPUT CONDITIONS WERE ESTABLISED.
Qnn : THE LEVEL OF Qn BEFORE THE MOST RECENT ACTIVE TRANSITION INDICATED BY OR
a, h : THE LEVEL OF THE STEADY STATE INPUTS A, H, RESPECTIVELY.
X : DON'T CARE

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature:	-40 to +85	°C
dt/dv	Input Rise and Fall Time V_{CC} = 4.5 to 5.5V (note 1)	8	ns/V

1) V_{IN} from 0.8 V to 2.0 V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5	V_O = 0.1 V or V_{CC} - 0.1 V		2.0	1.5		2.0		V
		5.5			2.0	1.5		2.0		
V_{IL}	Low Level Input Voltage	4.5	V_O = 0.1 V or V_{CC} - 0.1 V			1.5	0.8		0.8	V
		5.5				1.5	0.8		0.8	
V_{OH}	High Level Output Voltage	4.5	V_I(*) = V_{IH} or V_{IL}	I_O=-50 µA	4.4	4.49		4.4		V
		5.5		I_O=-50 µA	5.4	5.49		5.4		
		4.5		I_O=-24 mA	3.86			3.76		
		5.5		I_O=-24 mA	4.86			4.76		
V_{OL}	Low Level Output Voltage	4.5	V_I(*) = V_{IH} or V_{IL}	I_O=50 µA		0.001	0.1		0.1	V
		5.5		I_O=50 mA		0.001	0.1		0.1	
		4.5		I_O=24 mA			0.36		0.44	
		5.5		I_O=24 mA			0.36		0.44	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1	µA
I_{OZ}	3 State Output Leakage Current	5.5	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5	µA
I_{CCT}	Max I_{CC} /Input	5.5	V_I = V_{CC} -2.1 V			0.6			1.5	mA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				8		80	µA
I_{OLD}	Dynamic Output Current (note 1, 2)	5.5	V_{OLD} = 1.65 V max						75	mA
I_{OHD}			V_{OHD} = 3.85 V min						-75	mA

1) Maximum test duration 2ms, one output loaded at time
2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50 Ω.
(*) All outputs loaded.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input $t_r = t_f$ =3 ns)

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CLOCK to Q'_A, Q'_H	5.0(*)			7.2	10.5	1.0	12.0	ns
t_{PLH} t_{PHL}	Propagation Delay Time CLOCK to Q_A - Q_H	5.0(*)			7.4	11.4	1.0	13.0	ns
t_{PHL}	Propagation Delay Time $\overline{CLEAR}$ to Q'_A, Q'_H	5.0(*)			6.0	10.0	1.0	11.5	ns
t_{PHL}	Propagation Delay Time $\overline{CLEAR}$ to Q_A - Q_H	5.0(*)			6.3	10.5	1.0	12.0	ns
t_{PZL} t_{PZH}	Output Enable Time	5.0(*)			7.4	11.4	1.0	13.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time	5.0(*)			7.2	9.6	1.0	11.0	ns
t_w	$\overline{CLEAR}$ pulse Width, LOW	5.0(*)				5.0		5.0	ns
t_w	CLOCK pulse Width	5.0(*)				5.0		5.0	ns
t_s	Setup Time HIGH or LOW (S0 or S1 to CK)	5.0(*)				6.0		6.5	ns
t_h	Hold Time HIGH or LOW (S0 or S1 to CK)	5.0(*)				0.0		0.0	ns
t_s	Setup Time HIGH or LOW (SR or SL to CK)	5.0(*)				3.5		3.5	ns
t_h	Hold Time HIGH or LOW (SR or SL to CK)	5.0(*)				2.0		2.0	ns
t_{REM}	Recovery Time $\overline{CLR}$ to Q	5.0(*)				2.0		2.0	ns
f_{MAX}	Maximum Clock Frequency	5.0(*)		80	120		80		MHz

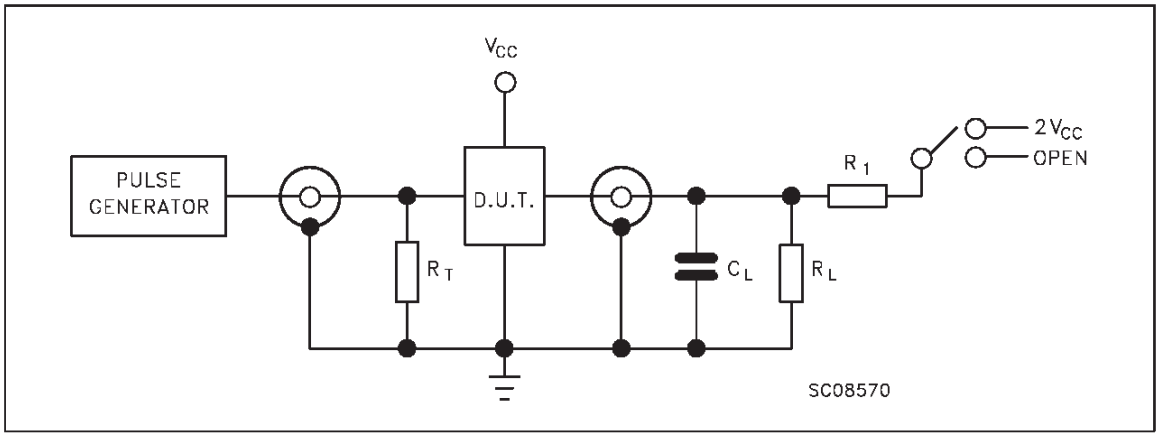
*) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10	pF
$C_{I/O}$	Bus Input Capacitance	5.0			13				
C_{PD}	Power Dissipation Capacitance (note 1)	5.0	f_{IN} = 10 MHz		160				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to

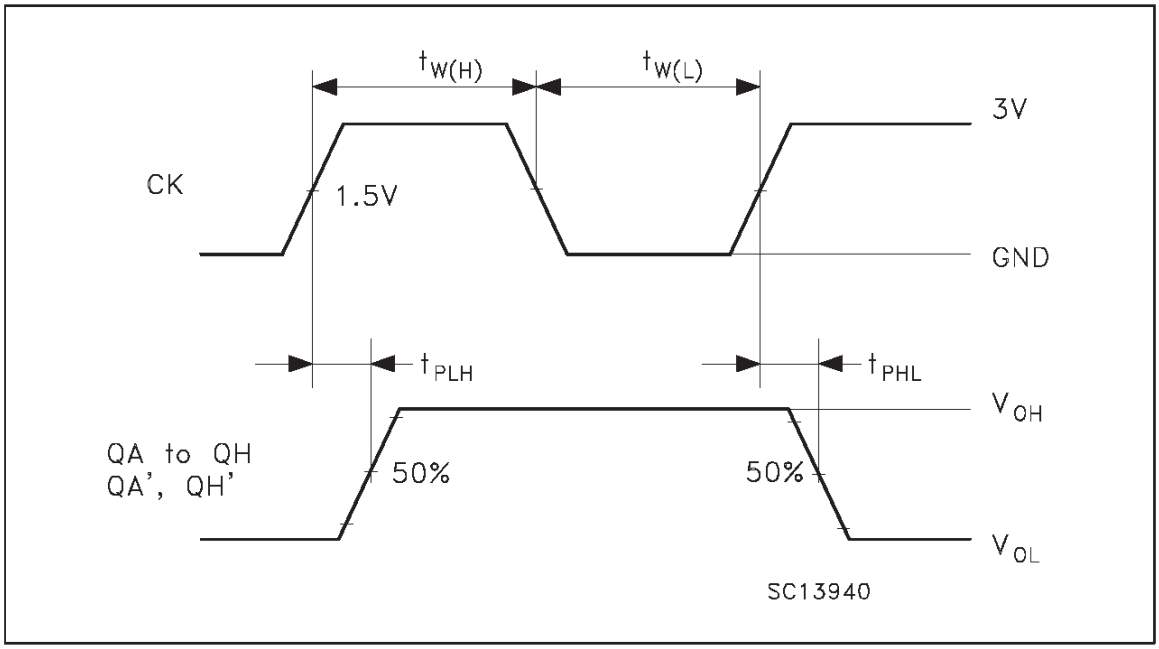
TEST CIRCUIT



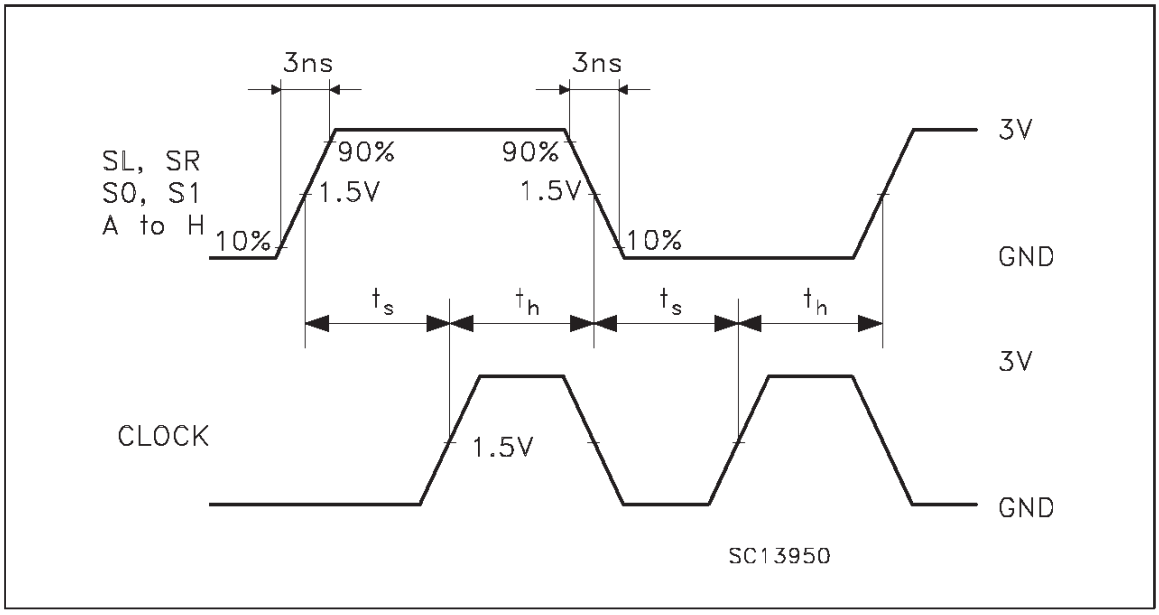
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$2V_{CC}$
t_{PZH}, t_{PHZ}	Open

C_L = 50 pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

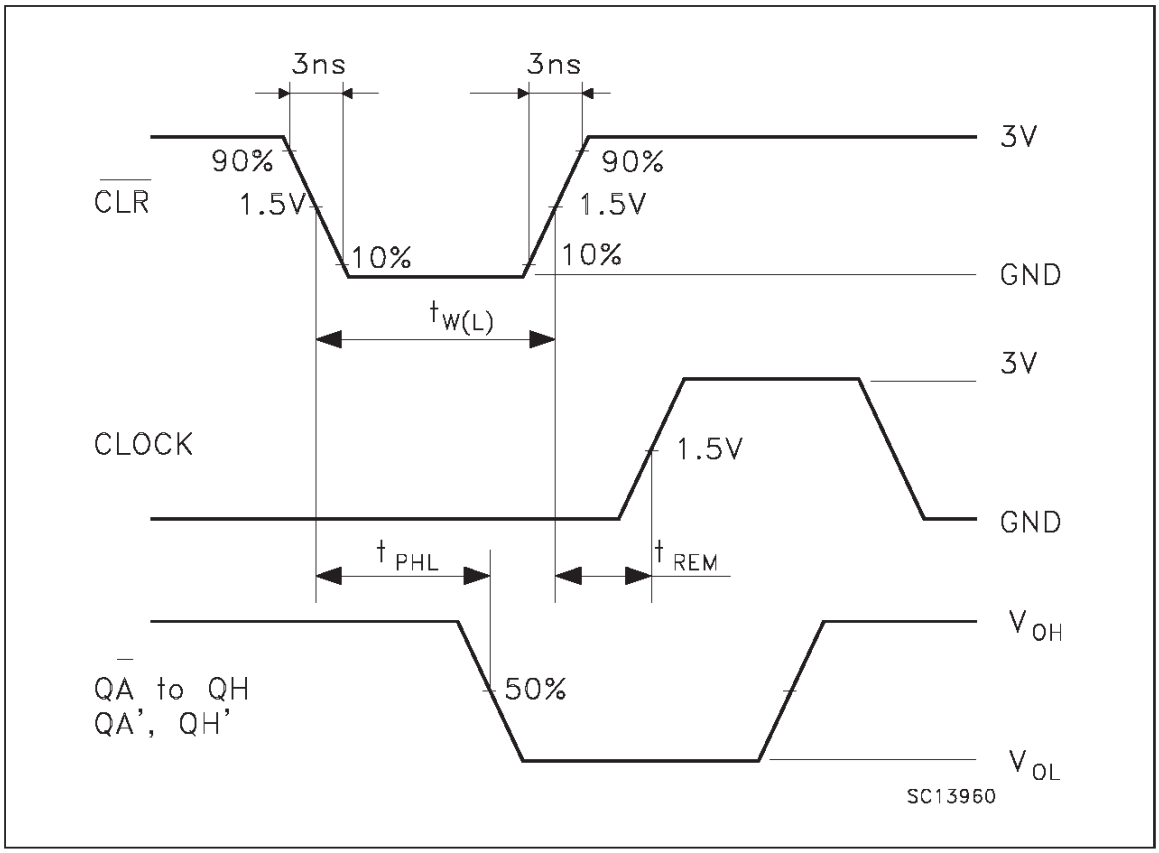
WAVEFORM 1: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



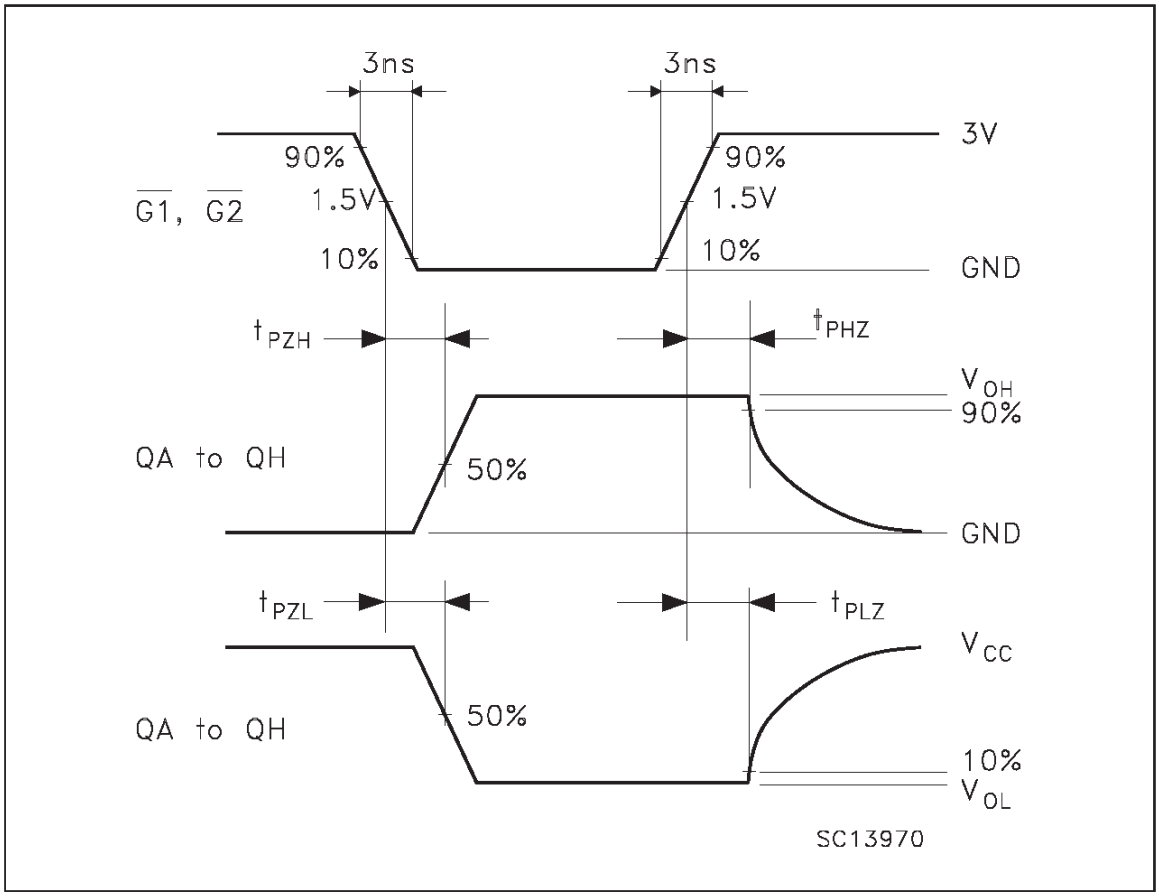
WAVEFORM 2: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



WAVEFORM 3: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)

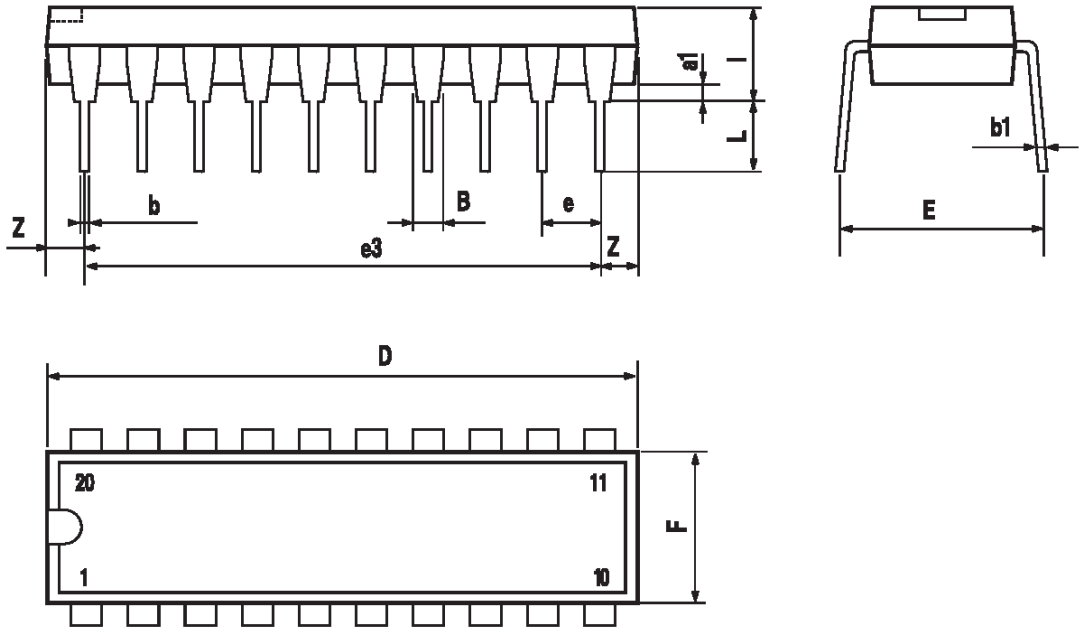


WAVEFORM 4: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



Plastic DIP-20 (0.25) MECHANICAL DATA

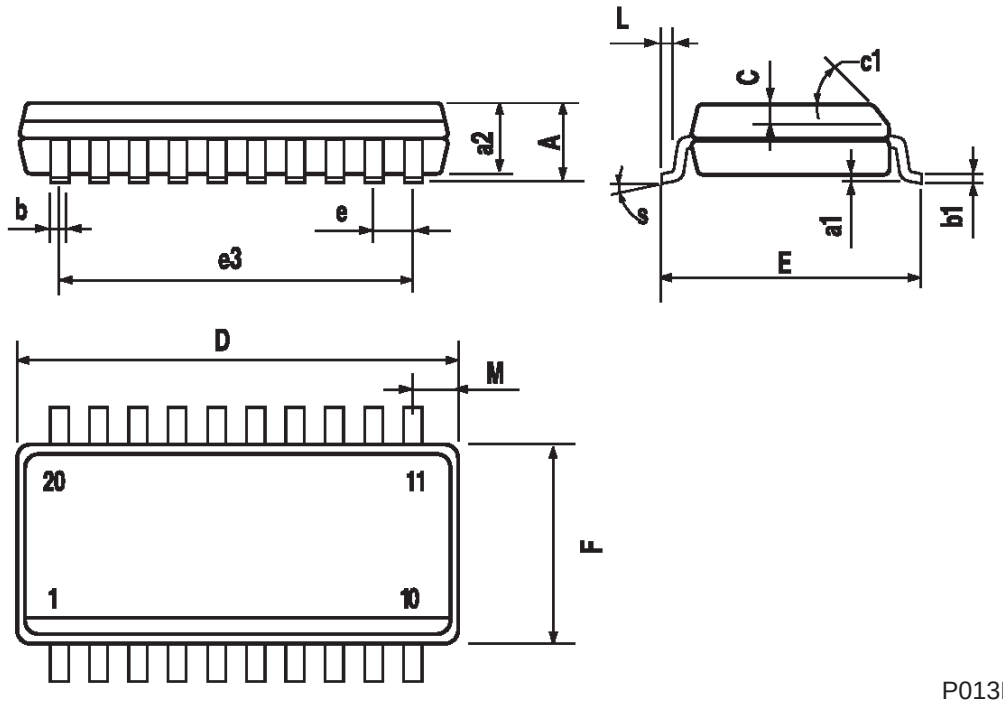
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

SO-20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



P013L