

## 54AC253 • 54ACT253 Dual 4-Input Multiplexer with TRI-STATE® Outputs

### General Description

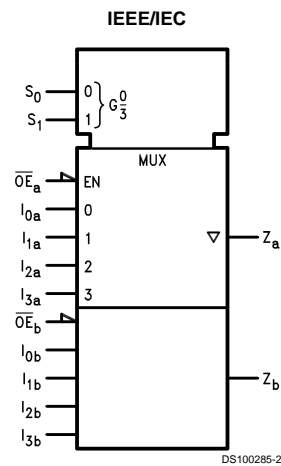
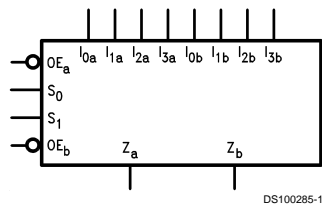
The 'AC/ACT253 is a dual 4-input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ( $\overline{OE}$ ) inputs, allowing the outputs to interface directly with bus oriented systems.

- Multifunction capability
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT253 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC253: 5962-87693
  - 'ACT253: 5962-87761

### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%

### Logic Diagrams

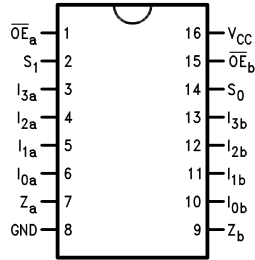


Pin Names	Description
$I_{0a}$ – $I_{3a}$	Side A Data Inputs
$I_{0b}$ – $I_{3b}$	Side B Data Inputs
$S_0$ , $S_1$	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
$Z_a$ , $Z_b$	TRI-STATE Outputs

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FACT® is a registered trademark of Fairchild Semiconductor Corporation.

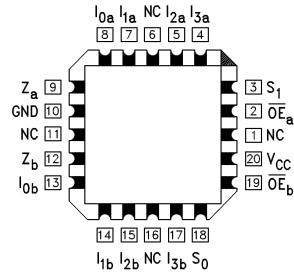
## Connection Diagrams

Pin Assignment  
for DIP and Flatpak



DS100285-3

Pin Assignment  
for LCC



DS100285-4

## Functional Description

The 'AC/ACT253 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs ( $S_0$ ,  $S_1$ ). The 4-input multiplexers have individual Output Enable ( $\overline{OE}_a$ ,  $\overline{OE}_b$ ) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot S_1 \cdot S_0 + I_{1a} \cdot S_1 \cdot S_0 +$$

$$I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 +$$

$$I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

## Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
$S_0$	$S_1$	$I_0$	$I_1$	$I_2$	$I_3$	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs  $S_0$  and  $S_1$  are common to both sections.

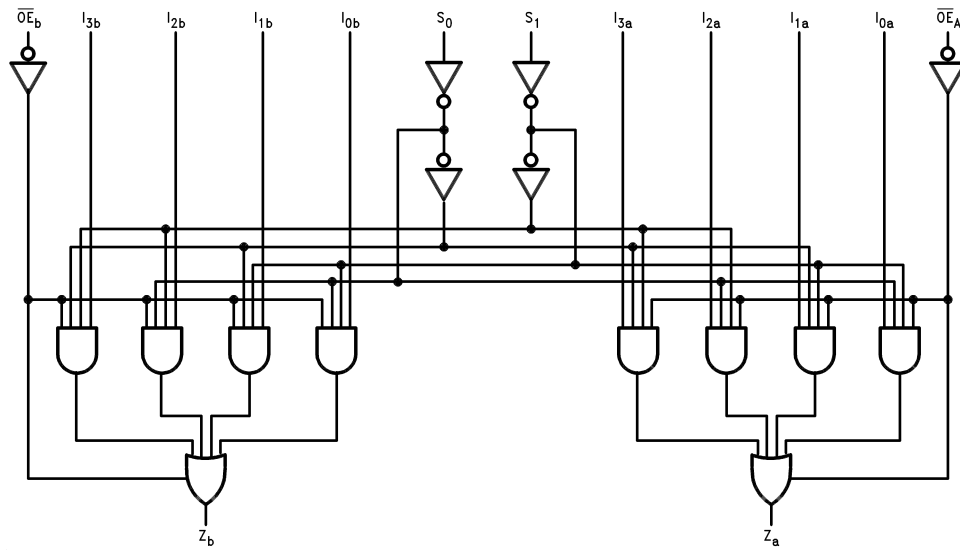
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## Logic Diagram



DS100285-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
CDIP	175°C

### Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

### DC Characteristics for 'AC Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54AC	Units	Conditions	
			$T_A =$			
			-55°C to +125°C			
			Guaranteed Limits			
$V_{IH}$	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	3.15			
		5.5	3.85			
$V_{IL}$	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	1.35			
		5.5	1.65			
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.4			
		5.5	5.4			
			3.0	2.4	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA
			4.5	3.7		
			5.5	4.7		
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.1			
		5.5	0.1			
			3.0	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA
			4.5	0.50		
			5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$	
$I_{OZ}$	Maximum TRI-STATE Current	5.5	$\pm 5.0$	$\mu A$	$V_I (OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}, GND$ $V_O = V_{CC}, GND$	

## DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54AC		Units	Conditions
			T <sub>A</sub> = -55°C to +125°C			
			Guaranteed Limits			
I <sub>OLD</sub>	(Note 3) Minimum Dynamic	5.5	50		mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current	5.5	-50		mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

## DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	54ACT		Units	Conditions	
			T <sub>A</sub> = -55°C to +125°C				
			Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	2.0		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	2.0				
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	0.8		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	0.8				
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.4		V	I <sub>OUT</sub> = -50 μA	
		5.5	5.4				
			4.5	3.70		V	(Note 5) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA
			5.5	4.70			
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.1		V	I <sub>OUT</sub> = 50 μA	
		5.5	0.1				
		4.5	0.50				V
5.5	0.50						
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OZ</sub>	Maximum TRI-STATE Current	5.5	±5.0		μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND	
I <sub>CC</sub> T	Maximum I <sub>CC</sub> /Input	5.5	1.6		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	
I <sub>OLD</sub>	(Note 6) Minimum Dynamic	5.5	50		mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Output Current	5.5	-50		mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Note 5:** All outputs loaded; thresholds on input associated with output under test.

**Note 6:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 7:** I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
t <sub>PLH</sub>	Propagation Delay S <sub>n</sub> to Z <sub>n</sub>	3.3	1.0	18.0	ns	
		5.0	1.0	12.5		
t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to Z <sub>n</sub>	3.3	1.0	18.5	ns	
		5.0	1.0	13.5		
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	3.3	1.0	17.0	ns	
		5.0	1.0	11.5		
t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	3.3	1.0	15.0	ns	
		5.0	1.0	11.5		
t <sub>PZH</sub>	Output Enable Time	3.3	1.0	9.0	ns	
		5.0	1.0	7.0		
t <sub>PZL</sub>	Output Enable Time	3.3	1.0	9.5	ns	
		5.0	1.0	8.0		
t <sub>PHZ</sub>	Output Disable Time	3.3	1.0	10.5	ns	
		5.0	1.0	9.0		
t <sub>PLZ</sub>	Output Disable Time	3.3	1.0	9.5	ns	
		5.0	1.0	8.0		

**Note 8:** Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V

## AC Electrical Characteristics

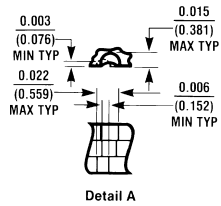
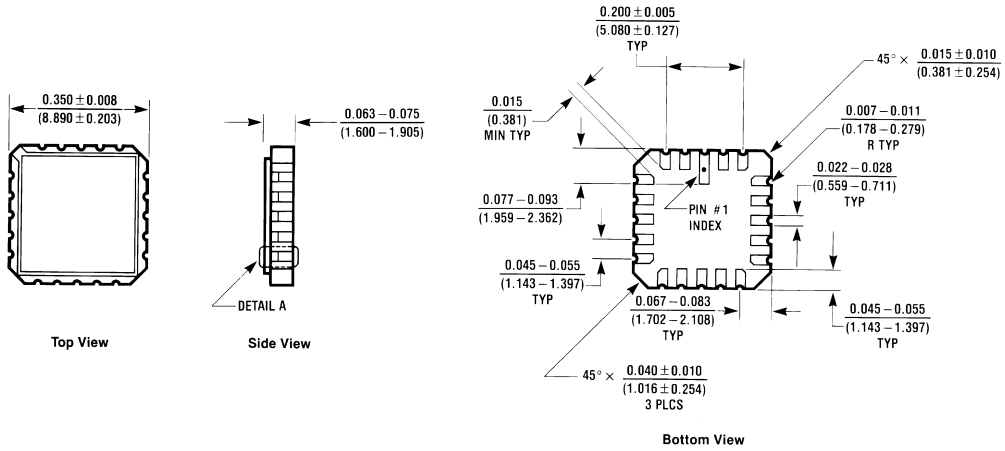
Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
t <sub>PLH</sub>	Propagation Delay S <sub>n</sub> to Z <sub>n</sub>	5.0	1.0	14.5	ns	
t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to Z <sub>n</sub>	5.0	1.0	16.0	ns	
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	5.0	1.0	12.0	ns	
t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	5.0	1.0	13.5	ns	
t <sub>PZH</sub>	Output Enable Time	5.0	1.0	9.5	ns	
t <sub>PZL</sub>	Output Enable Time	5.0	1.0	9.5	ns	
t <sub>PHZ</sub>	Output Disable Time	5.0	1.0	11.0	ns	
t <sub>PLZ</sub>	Output Disable Time	5.0	1.0	9.0	ns	

**Note 9:** Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

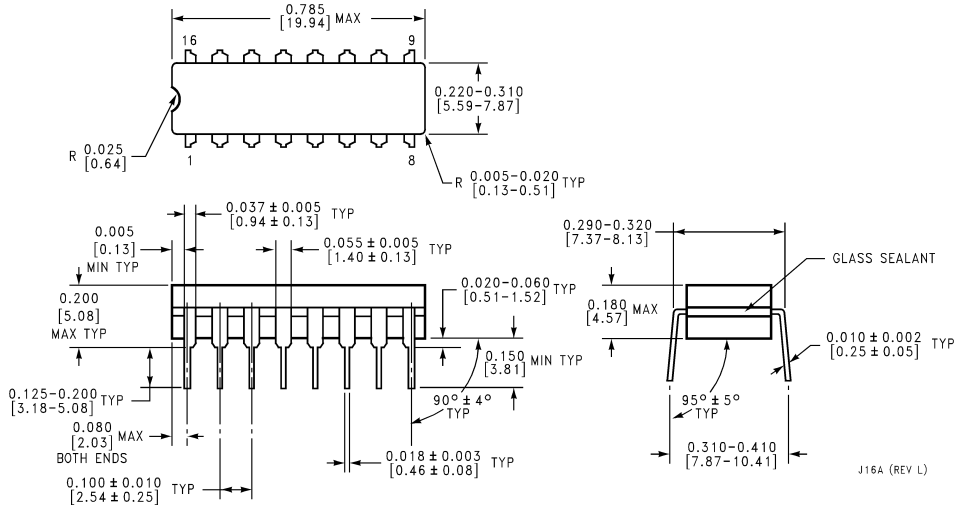
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	50.0	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20 Terminal Ceramic Leadless Chip Carrier (L)**  
 NS Package Number E20A

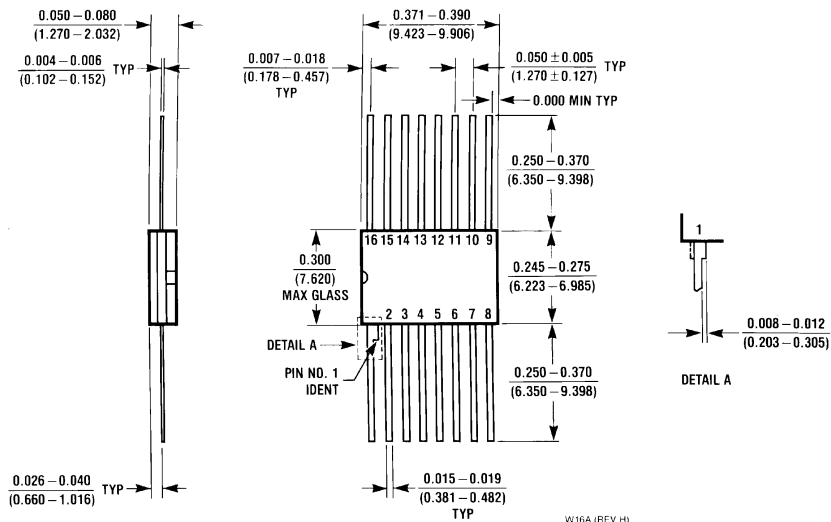
E20A (REV D)



**16 Lead Ceramic Dual-In-Line Package (D)**  
 NS Package Number J16A

J16A (REV L)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16 Lead Ceramic Flatpak (F)  
NS Package Number W16A**

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