NEC

MOS INTEGRATED CIRCUIT

μPD6461, 6462

CMOS LSI CHIP FOR CAMCORDER ON-SCREEN CHARACTER DISPLAY (12 ROWS × 24 COLUMNS)

The μPD6461, 6462 are CMOS LSI chips designed to provide on-screen character display for camcorders. When combined with a microcontroller, the μPD6461, 6462 control the display of the characters displayed in the viewfinder (count, time, date, etc.) and the recording of characters onto video tape (time, date, etc.).

Each character is created using 12 (width) × 18 (height) dots. Kanji characters and graphic symbols can also be displayed by using two or more characters. The μPD6461, 6462 are compatible with color viewfinders and can output character signals to three channels, the RGB channel for the color viewfinder and the V_{C1} and V_{C2} channels for the recording system and monitor terminal.

The μPD6461, 6462 also have a power-on clear function and video RAM batch clear command, enabling the number of operations assigned to the microcontroller to be reduced.

FEATURES

- Maximum number of characters: 12 rows × 24 columns (288 characters)
- Number of character patterns : 256 (μPD6461)/128 (μPD6462) (stored in ROM). Each pattern can be changed by specifying a mask code option.
- Character size : One dot per line or one dot per two lines (field)
- Number of character colors : 8
- Background : No background, minimum background, or overall background can be selected for the entire screen, together with rimming ON/OFF function. Any one of 8 different colors is selectable as the background color and together with the rim color (black or white) selectable per screen.
- Dot matrix : Each character consists of 12 (width) × 18 (height) dots. There is no gap between adjacent characters.
- Blinking : Blinking can be turned on/off for each character. The blinking ratio is 1:1. The blinking frequency can be selected from approx. 1 Hz, 2 Hz, and 0.5 Hz for the entire screen.
- Reversed characters : Specified characters can be displayed in reverse video.
- Character signal output : Character signals can be output to three channels. Output mode (1) (RGB + BLK, V_{C1} + V_{BLK1}, and V_{C2} + V_{BLK2}) or output mode (2) (R + R_{BLK}, B + B_{BLK}, and G + G_{BLK}) can be selected by specifying a mask option. For output mode 1, three output formats are available for the V_{C1} and V_{C2} channels (options A, B, and C).
- Clearing of video RAM : Video RAM batch clear command and power-on clear function
- Interface with a microcontroller : 8-bit serial input supporting variable word length (LSB first or MSB first can be selected by specifying a mask option.)
- Supply voltage : Low-voltage operation possible (supply voltage range: 2.7 to 5.5 V)

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The mark ★ shows major revised points.

ORDERING INFORMATION

Part number	Package
μPD6461GS-xxx	20-pin plastic shrink SOP (300 mil)
μPD6461GT-xxx	24-pin plastic SOP (375 mil)
μPD6462GS-xxx	20-pin plastic shrink SOP (300 mil)

Remarks 1. xxx is a ROM code suffix.

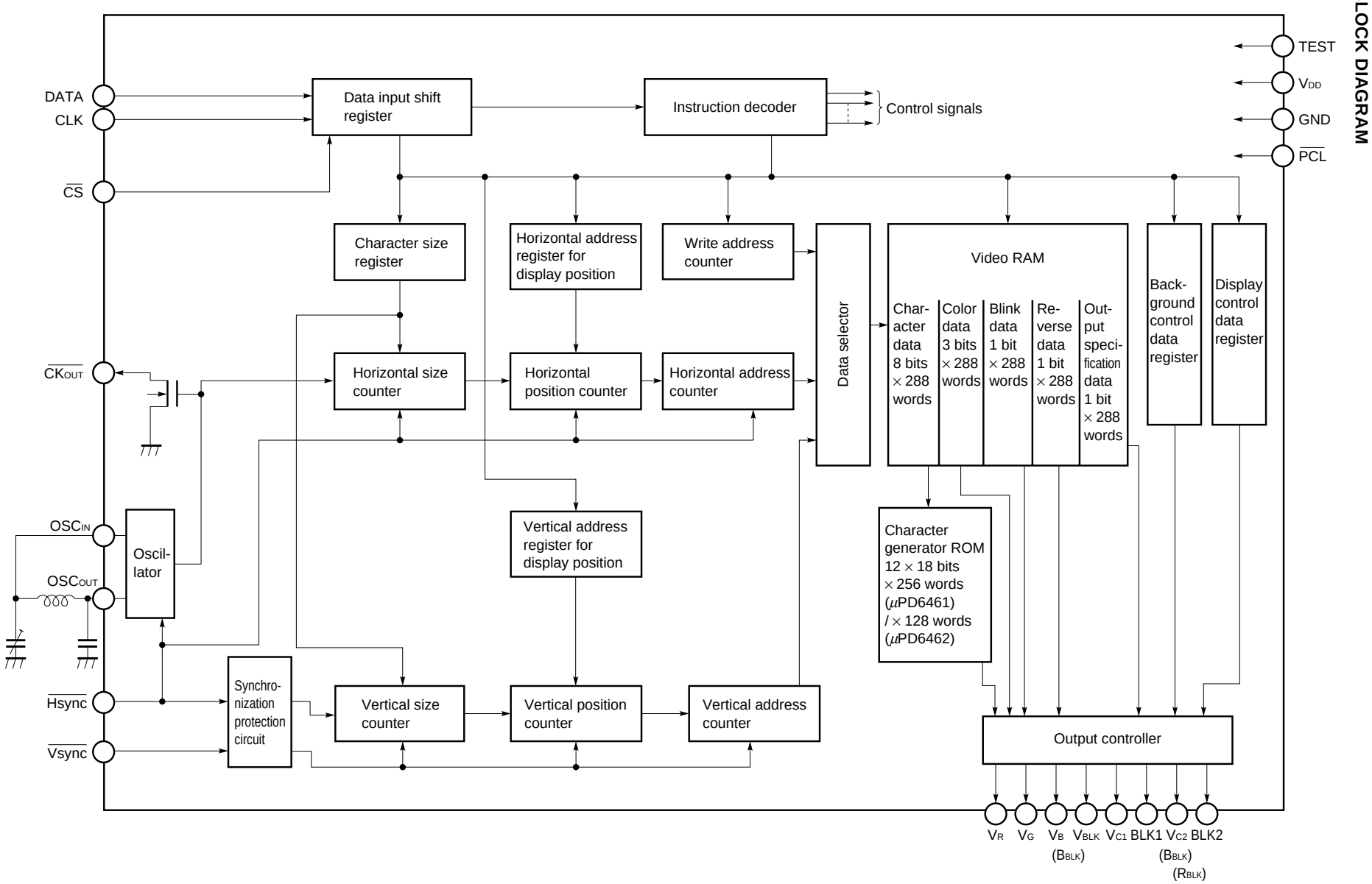
2. NEC's standard models are the μPD6461GS-101/102, μPD6462GS-001. For the details of the character generator ROM, refer to **5. CHARACTER PATTERNS**.

μPD6461GS-101: MSB first/Specified in three-line units/RGB+3BLK/Option B/LC oscillation

μPD6461GS-102: MSB first/Specified in three-line units/RGB+V_{C1}+V_{C2}/Option B/LC oscillation

μPD6462GS-001: MSB first/Specified in three-line units/RGB+V_{C1}+V_{C2}/Option C/LC oscillation

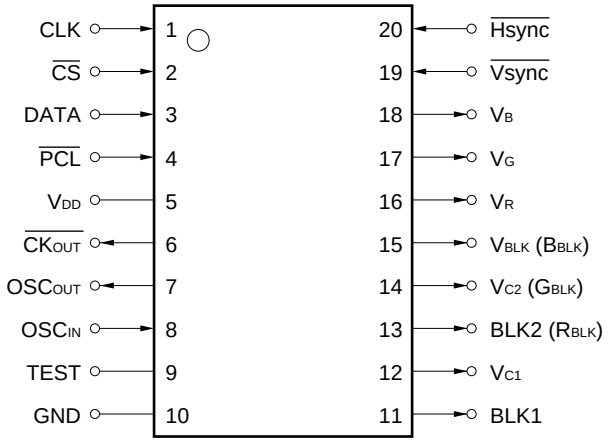
BLOCK DIAGRAM



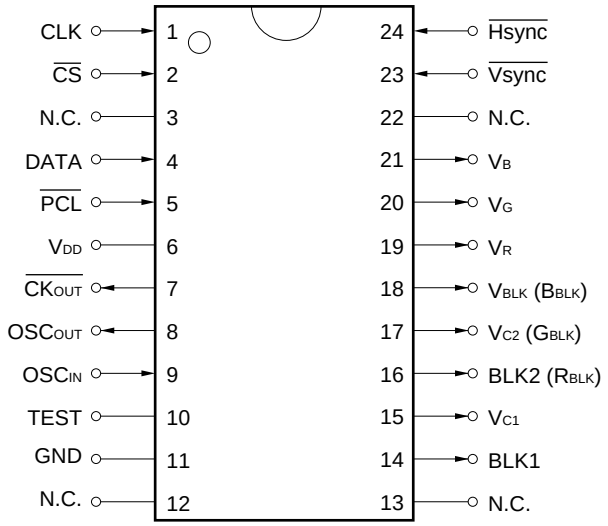
Remark Signals in ( ) are set by a mask option (RGB + RGB compatible blanking).

PIN CONFIGURATION (TOP VIEW)

20-pin plastic shrink SOP (300 mil)
μPD6461GS-xxx
μPD6462GS-xxx



24-pin plastic SOP (375 mil)
μPD6461GT-xxx



Remarks 1. xxx indicates a ROM code suffix.

2. Signals in ( ) are set by a mask option (RGB + RGB compatible blanking).

B_{BLK} : Blanking B
BLK1, BLK2: Blanking Output 1, 2
$\overline{CK_{OUT}}$: Clock Output
CLK : Clock Input
$\overline{CS}$: Chip Select
DATA : Data Input
G_{BLK} : Blanking G
GND : Ground
$\overline{Hsync}$: Horizontal Synchronous Signal Input
N.C. : No Connection
OSC_{IN} : Oscillator Input
OSC_{OUT} : Oscillator Output
$\overline{PCL}$: Power-on Clear
R_{BLK} : Blanking R
TEST : Test
V_B : Character Signal Output
V_{BLK} : Blanking Signal Output for V_R, V_G, V_B
V_{C1}, V_{C2} : Character Signal Output 1, 2
V_{DD} : Power Supply
V_G : Character Signal Output
V_R : Character Signal Output
$\overline{Vsync}$: Vertical Synchronous Signal Input

PIN FUNCTIONS

Pin No.[Note 1]	Symbol[Note 2]	Function[Note 2]	Description
1	CLK	Clock input	Input pin for the data read clock. The data input to the DATA pin is read at rising edges of the clock.
2	$\overline{CS}$	Chip select input	Serial transfer is accepted when this pin is low.
3 (4)	DATA	Serial data input	Input pin for control data. Data is read in synchronization with the clock input to the CLK pin.
4 (5)	$\overline{PCL}$	Power-on clear	Pin used for the power-on clear function. After power-on, set this pin from low to high to initialize the IC.
5 (6)	V_{DD}	Power supply	Power supply pin
6 (7)	$\overline{CK_{OUT}}$	Clock output	N-ch open-drain output pin used to check the oscillation frequency
7 (8) 8 (9)	OSC_{OUT} OSC_{IN}	LC oscillator input/ output OSC_{IN}: External clock input	Input and output pins for the oscillator for generating a dot clock. Connect the oscillation coil and capacitors to these pins. (When an external clock input is selected by specifying a mask option, input an external clock (synchronized with $\overline{Hsync}$) to the OSC_{IN} pin. Leave the OSC_{OUT} pin open.)
9 (10)	TEST	Test pin	Pin used for testing the IC. Usually, connect this pin to ground. The IC cannot enter test mode while this pin is connected to ground.
10 (11)	GND	Ground pin	Connect this pin to the system ground.
11 (14)	BLK1	Blanking signal output 1	Pin used to output the blanking signal for the video signal output from the V_{C1} pin. The blanking signal is high active. (When RGB compatible blanking has been selected by specifying a mask option, this pin outputs the logical OR of R_{BLK}, G_{BLK}, and B_{BLK}.)
12 (15)	V_{C1}	Character signal output 1	Pin used to output a high-active character signal. (When RGB compatible blanking has been selected by specifying a mask option, this pin outputs the logical OR of V_R, V_G, and V_B.)
13 (16)	BLK2 (R_{BLK})	Blanking signal output 2 (blanking R)	Pin used to output the blanking signal for the video signal output from the V_{C2} pin. The blanking signal is high active. (This pin outputs the blanking signal for the video signal output from the V_R pin. The blanking signal is high active.)
14 (17)	V_{C2} (G_{BLK})	Character signal output 2 (blanking G)	Pin used to output a high-active character signal. (This pin outputs the blanking signal for the video signal output from the V_G pin. The blanking signal is high active.)
15 (18)	V_{BLK} (B_{BLK})	Blanking signal output (blanking B)	Pin used to output the blanking signal for the video signals output from the V_R, V_G, and V_B pins. The blanking signal is high active. (This pin outputs the blanking signal for the video signal output from the V_B pin. The blanking signal is high active.)
16 (19) 17 (20) 18 (21)	V_R V_G V_B	Character signal output	Pins used to output high-active character signals.
19 (23)	$\overline{Vsync}$	Vertical synchronizing signal input	Input a low-active vertical synchronizing signal to this pin.
20 (24)	$\overline{Hsync}$	Horizontal synchronizing signal input	Input a low-active horizontal synchronizing signal to this pin.
(3, 12, 13, 22)	N.C.	No connection	Vacant pin

Notes 1. Pin numbers indicated in ( ) are that of the μPD6461GT-xxx.

2. Signals in ( ) are set by a mask option (RGB + RGB compatible blanking).

CONTENTS

1. MASK CODE OPTIONS

1.1 MASK CODE OPTIONS

The μPD6461, μPD6462 provide mask options for selecting the following items:

	Item	Selections		
(1)	Data transfer	LSB first	MSB first	
(2)	Vertical display start position	Specified in three-line units	Specified in nine-line units	
(3)	Pin selection	RGB+V_{C1}+V_{C2}	RGB+3BLK	
(4)	Output distribution format	Option A	Option B	Option C
(5)	Dot clock	LC oscillation	External clock input	

(1) Data transfer

Select the command transfer format.

(2) Vertical display start position

Select the units used for specifying the vertical display start position of the character display area. In three-line units, the vertical display start position can be set more finely than in nine-line units.

(3) Pin selection

Select the pins used to output character signals. In RGB+V_{C1}+V_{C2} mode, character signals are output from the V_R, V_G, V_B, V_{BLK}, V_{C1}, BLK1, V_{C2}, and BLK2 pins. In RGB+3BLK mode, character signals are output from the V_R, V_G, V_B, R_{BLK}, G_{BLK}, B_{BLK}, V_{C1}, and BLK1 pins.

When displaying colored characters in a color viewfinder, select RGB+V_{C1}+V_{C2} mode. When assigning a separate character signal for each color, select RGB+3BLK mode.

(4) Output distribution format

Select the format to be used to distribute character signals to the V_{C1} and V_{C2} channels when RGB+V_{C1}+V_{C2} mode is selected. (When RGB+3BLK mode is selected, select option A as the output distribution format. Options B and C are invalid.)

When an on-screen IC is used in a camcorder, some information is displayed in the viewfinder and recorded onto video tape (such as a date and title). Other information, however, need only be displayed in the viewfinder (battery or focus alarm and tape count). The μPD6461, 6462 can distribute such information to different output channels in units of rows or half rows. You can select option A, option B, and option C as the output distribution format (only when RGB+V_{C1}+V_{C2} mode is selected).

(5) Dot clock

Select the dot clock to be used to display characters. When an external clock input is selected, refer to **EXTERNAL CLOCK INPUT** in **6**. **ELECTRICAL CHARACTERISTICS**.

1.2 HOW TO SELECT MASK OPTIONS

To select mask options, use the option setting command (OC) of the Character Pattern Editor, a tool designed for editing character pattern data.

Activate the Character Pattern Editor, then display the following setting menu:

OC (COMMAND INPUT)
OPTION DATA (0---LSB FAST , 1---MSB FAST) : ..... (1)
OPTION DATA (0---V:9H , 1---V:3H) : ..... (2)
OPTION DATA (0---RGB+3BLK , 1---RGB+V_{C1}+V_{C2}) : ..... (3)
OPTION DATA (0---OUTPUT 20 , 1---OUTPUT 21) : ..... (4)
OPTION DATA (0---OUTPUT 10 , 1---OUTPUT 11) : ..... (5)
OPTION DATA (0---EXT CLK , 1---LC) : ..... (6)
OPTION DATA (0---LC , 1---EXT CLK) : ..... (7)

Actually, the above menu is displayed one line at a time. Once you have selected an option, the next line is displayed.

Select 0 or 1 for lines (1), (2), (3), (6), and (7), according to the setting to be made. For the dot clock, however, make the same settings (different values) for lines (6) and (7). For example, when selecting LC oscillation, select “LC” for both lines (1 for (6) and 0 for (7)). Don’t select external clock input for lines (6) and/or (7).

When selecting the output distribution format, select the values on lines (4) and (5) as follows:

	(4)	(5)
Option A	1(OUTPUT 21)	0(OUTPUT 10)
Option B	0(OUTPUT 20)	0(OUTPUT 10)
Option C	1(OUTPUT 21)	1(OUTPUT 11)

The settings are valid only when RGB+V_{C1}+V_{C2} mode has been selected. Select option A (1, 0) when RGB+3BLK mode has been selected.

The following table lists the correspondence between the command bits and the lines of the setting menu. Specify 0 or 1 for each bit.

D7	D6	D5	D4	D3	D2	D1	D0
0	(1)	(2)	(3)	(4)	(5)	(6)	(7)

Command OD displays the result of the selection, as a hexadecimal number.

Example: When the mask options are selected as follows:

Mask option	Bit	Command
MSB first	D6	1
Specification in three-line units	D5	1
RGB+3BLK	D4	0
Option A (only option A can be specified in RGB+3BLK mode)	D3	1
	D2	0
LC oscillation	D1	1
	D0	0

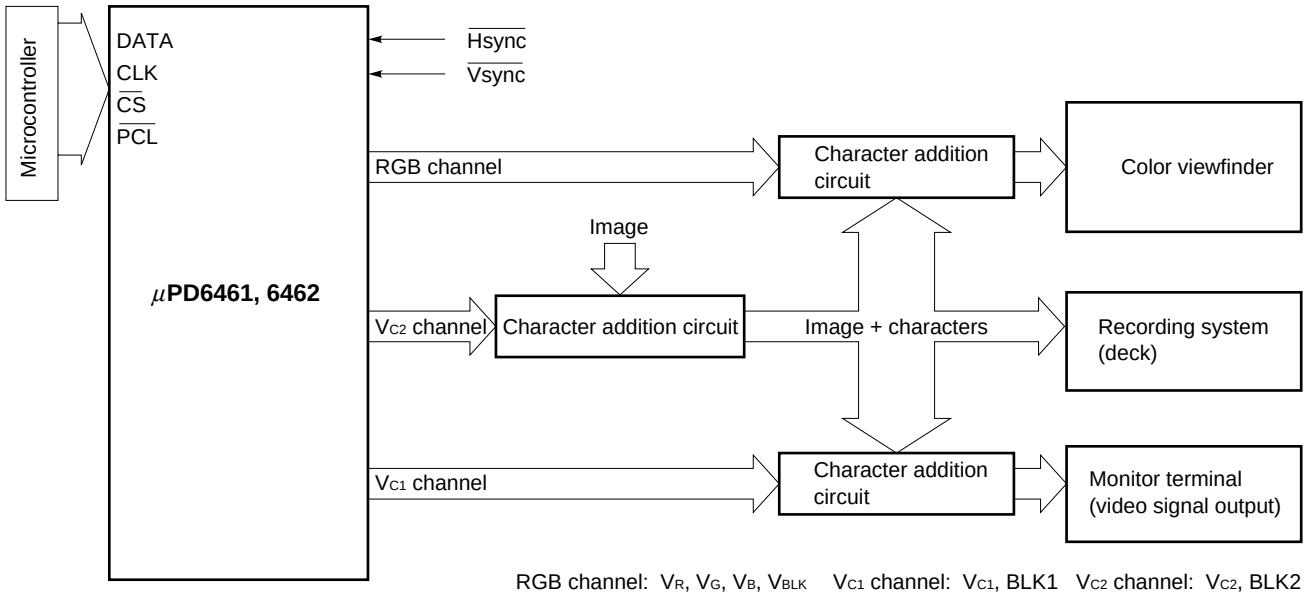
The command bits are set as follows:

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	1	0

→Command OD displays 6AH.

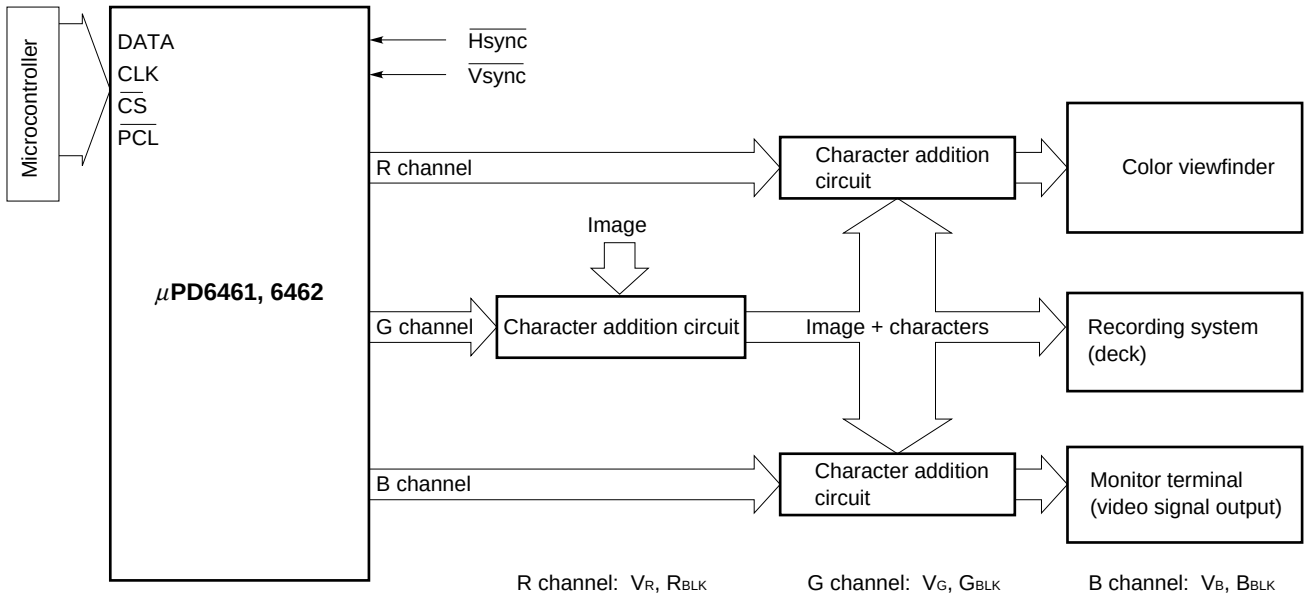
1.3 APPLICATION BLOCK DIAGRAMS

Example of application to a camcorder (1) (in RGB+V_{C1}+V_{C2} mode)
(The V_R, V_G, V_B, V_{BLK}, V_{C1}, BLK1, V_{C2}, and BLK2 pins are used.)



RGB channel: V_R, V_G, V_B, V_{BLK} V_{C1} channel: V_{C1}, BLK1 V_{C2} channel: V_{C2}, BLK2

Example of application to a camcorder (2) (in RGB+3BLK mode for RGB compatible blanking)
(The V_R, V_G, V_B, R_{BLK}, G_{BLK}, and B_{BLK} pins are used.)



R channel: V_R, R_{BLK} G channel: V_G, G_{BLK} B channel: V_B, B_{BLK}

1.4 DISPLAY IN RGB+V_{C1}+V_{C2} MODE

The μPD6461, 6462 provide three options, A, B, and C, for the output distribution format. This section describes how character signals are output when each option is selected. Output is controlled with the output pin control command (refer to **3.8 OUTPUT PIN CONTROL COMMAND** for details).

Output pin control command for MSB-first transfer (Command bits are input starting from the most significant bit (MSB), D15.)

(This command is a 2-byte command. 16 bits must be input for each command, even for continuous input.)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	1	0	0	V_{C2}	V_{C1}	0	0	AR3	AR2	AR1	AR0

Row specification bits				
AR3	AR2	AR1	AR0	Function
0	0	0	0	Specifies row 0.
0	0	0	1	Specifies row 1.
≈	≈	≈	≈	≈
1	0	1	1	Specifies row 11.
Other values are invalid.				

Option A

Output pin control bits		
V_{C2}	V_{C1}	Output from each pin
0	0	V_{C1}: Outputs a specified row. V_{C2}: Fixed to low level.
0	1	V_{C1}: Fixed to low level. V_{C2}: Outputs a specified row.

Option B

Output pin control bits		
V_{C2}	V_{C1}	Output from each pin
0	0	V_{C1}: Outputs all rows. V_{C2}: Fixed to low level.
0	1	V_{C1}: Outputs all rows. V_{C2}: Outputs a specified row.

Option C

Output pin control bits		
V_{C2}	V_{C1}	Output from each pin
0	0	V_{C1}: Outputs columns 0 to 23. V_{C2}: Fixed to low level.
0	1	V_{C1}: Outputs columns 0 to 11. V_{C2}: Outputs columns 12 to 23.
1	0	V_{C1}: Outputs columns 12 to 23. V_{C2}: Outputs columns 0 to 11.
1	1	V_{C1}: Fixed to low level. V_{C2}: Outputs columns 0 to 23.

- Row specification

  You can specify whether the V_{C1} or V_{C2} pin is used to output the character signals for each row (or each 12 columns).

- Output pin control

  The signals output from the V_{C1} and V_{C2} pins depend on whether option A, B, or C is selected (the corresponding blanking signals are output in the same way).

Option A output

Output pin control bits			
V_{C2}	V_{C1}	Output from each pin	
0	0	V_{C1}: Outputs the specified row. V_{C2}: Fixed to low level.	(1)
0	1	V_{C1}: Fixed to low level. V_{C2}: Outputs specified row.	(2)

	Output channel	Character signal	Background signal (if specified)
For case (1) above	V_{C1} channel	Outputs the logical OR of the character signals at the V_R, V_G, and V_B pins (for the specified rows), excluding those characters for which the V_{C2} channel has been specified.	Outputs a background signal for areas other than those for which the V_{C2} channel has been specified.
	V_{C2} channel	Fixed to low level (for the specified rows)	Outputs a background signal for those the areas for which the V_{C2} channel has been specified.
For case (2) above	V_{C1} channel	Fixed to low level (for the specified rows)	Outputs a background signal for areas other than those for which the V_{C2} channel has been specified.
	V_{C2} channel	Outputs those characters for which the V_{C2} channel has been specified (for the specified rows).	Outputs a background signal for those the areas for which the V_{C2} channel has been specified.

Option B output

Output pin control bits			
V_{C2}	V_{C1}	Output from each pin	
0	0	V_{C1}: Outputs all rows. V_{C2}: Fixed to low level.	(1)
0	1	V_{C1}: Outputs all rows. V_{C2}: Outputs a specified row.	(2)

	Output channel	Character signal	Background signal (if specified)
For case (1) above	V_{C1} channel	Outputs the logical OR of the character signals at the V_R, V_G, and V_B pins (for all rows), excluding those characters for which the V_{C2} channel has been specified.	Outputs a background signal for areas other than those for which the V_{C2} channel has been specified.
	V_{C2} channel	Fixed to low level (for the specified rows)	Outputs a background signal for those areas for which the V_{C2} channel has been specified.
For case (2) above	V_{C1} channel	Outputs the logical OR of the character signals at the V_R, V_G, and V_B pins (for all rows), excluding those characters for which the V_{C2} channel has been specified.	Outputs a background signal for areas other than those for which the V_{C2} channel has been specified.
	V_{C2} channel	Outputs the characters for which the V_{C2} channel is specified (for the specified rows).	Outputs a background signal for those areas for which the V_{C2} channel has been specified.

Option C output

Output pin control bits			
V_{C2}	V_{C1}	Output from each pin	
0	0	V_{C1}: Outputs columns 0 to 23. V_{C2}: Fixed to low level.	(1)
0	1	V_{C1}: Outputs columns 0 to 11. V_{C2}: Outputs columns 12 to 23.	(2)
1	0	V_{C1}: Outputs columns 12 to 23. V_{C2}: Outputs columns 0 to 11.	(3)
1	1	V_{C1}: Fixed to low level. V_{C2}: Outputs columns 0 to 23.	(4)

	Output channel	Character signal	Background signal (if specified)
For case (1) above	V_{C1} channel	Outputs the logical OR of the character signals at the V_R, V_G, and V_B pins (for columns 0 to 23 in the specified rows), excluding those characters for which the V_{C2} channel has specified.	Outputs a background signal for areas other than those for which the V_{C2} channel has been specified.
	V_{C2} channel	Fixed to low level (for the specified rows)	Outputs a background signal for those areas for which the V_{C2} channel has been specified.
For case (2) above	V_{C1} channel	Outputs the logical OR of the character signals at the V_R, V_G, and V_B pins (for columns 0 to 11 of the specified rows), excluding those characters for which the V_{C2} channel has been specified.	Outputs a background signal for areas other than those for which the V_{C2} channel has been specified.
	V_{C2} channel	Outputs the characters for which the V_{C2} channel has been specified (for columns 12 to 23 of the specified rows).	Outputs a background signal for those areas for which the V_{C2} channel has been specified.
For case (3) above	V_{C1} channel	Outputs the logical OR of the character signals at the V_R, V_G, and V_B pins (for columns 12 to 23 of the specified rows), excluding those characters for which the V_{C2} channel has been specified.	Outputs a background signal for areas other than those for which the V_{C2} channel has been specified.
	V_{C2} channel	Outputs the characters for which the V_{C2} channel has been specified (for columns 0 to 11 of the specified rows).	Outputs a background signal for those areas for which the V_{C2} channel has been specified.
For case (4) above	V_{C1} channel	Fixed to low level (for the specified rows)	Outputs a background signal for areas other than those for which the V_{C2} channel has been specified.
	V_{C2} channel	Outputs the characters for which the V_{C2} channel has been specified (for columns 0 to 23 in the specified rows).	Outputs a background signal for those areas for which the V_{C2} channel has been specified.

The RGB and V_{C1} channels do not output character signals for characters for which the V_{C2} channel has been specified. Background signals are output separately as listed above.

In addition, the μPD6461, 6462, when set to RGB+V_{C1}+V_{C2} mode, provide the following output control:

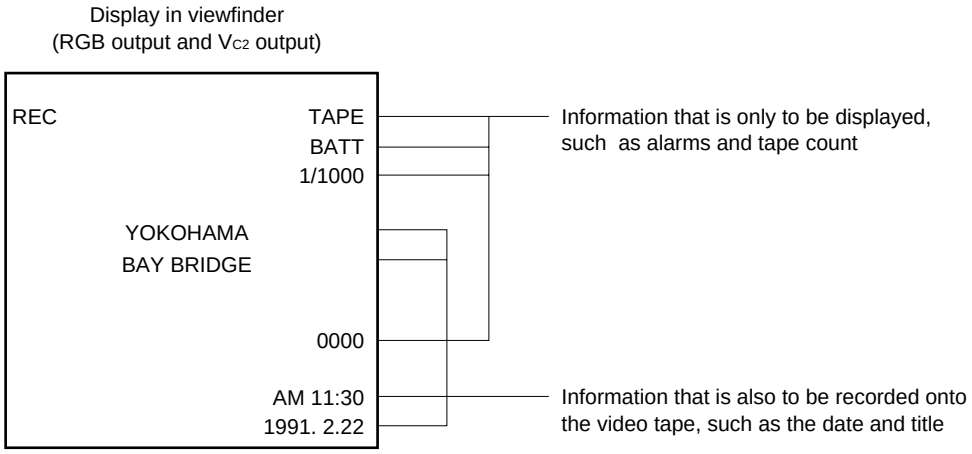
- Independent on/off control of character display for each channel (3-channel independent display on/off command)
- Independent control of the background for each channel (3-channel independent background control command)

1.4.1 Character Signal Output When Option A is Selected

Option A

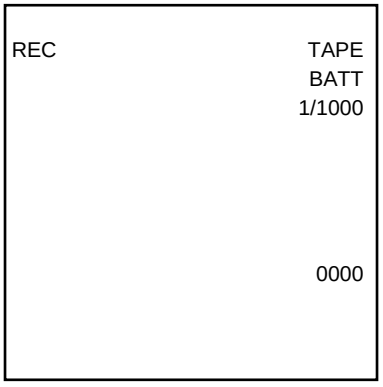
The V_{C1} bit of the output pin control command can be used to specify whether the characters of each row are output to the V_{C1} channel. Each character can be specified to be output to the V_{C2} channel, and the V_{C1} channel outputs only characters for which the V_{C2} channel in the rows for which the V_{C1} bit is set to 1. Characters for which the V_{C2} channel is specified are not output to the RGB or V_{C1} channel.

Display example (when the V_{C2} channel is used for information to be recorded)



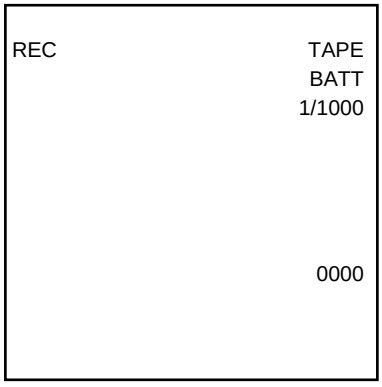
Output example with mask code option A specified

Characters output via RGB channel (colored characters)



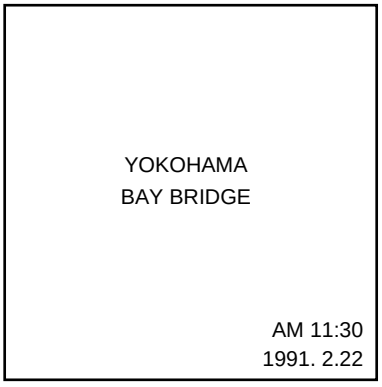
- The RGB channel does not output the characters for which the V_{C2} channel has been specified.

Characters output via V_{C1} channel (specified rows)



- The V_{C1} channel outputs the characters in the rows for which the V_{C1} bit is set to 0, excluding the characters for which the V_{C2} channel is specified.
- Rows for which the V_{C1} bit is set to 1 are not output (the V_{C1} pin is fixed to low level).

Characters output via V_{C2} channel (specified characters of specified rows)



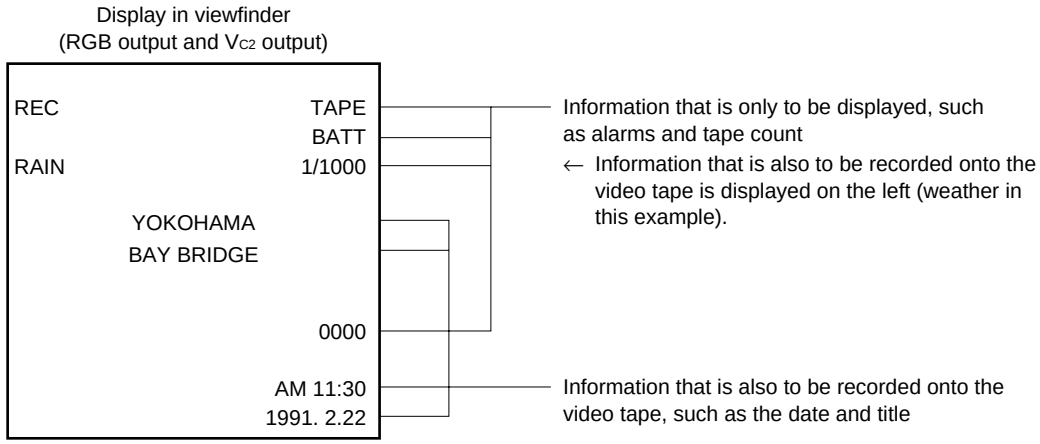
- Rows for which the V_{C1} bit is set to 0 are not output (the V_{C2} pin is fixed to low level).
- The V_{C2} channel outputs only those characters for which the V_{C2} channel has been specified in the rows for which the V_{C1} bit is set to 1.

1.4.2 Character Signal Output When Option B is Selected

Option B

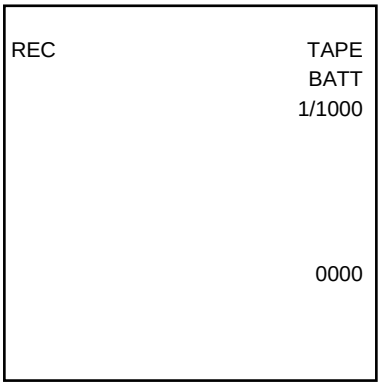
The V_{C1} channel outputs characters of all rows regardless of setting of the V_{C1} and V_{C2} bits. Each character can be specified to be output to the V_{C2} channel, and the V_{C2} channel outputs only characters for which the V_{C2} channel in the rows for which the V_{C1} bit is set to 1. Characters for which the V_{C2} channel is specified are not output to the RGB or V_{C1} channel.

Display example (when the V_{C2} channel is used for information to be recorded)



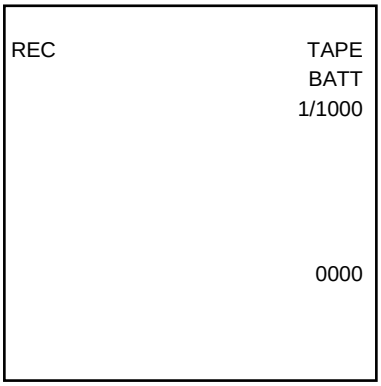
Output example with mask code option B specified

Characters output via RGB channel (colored characters)



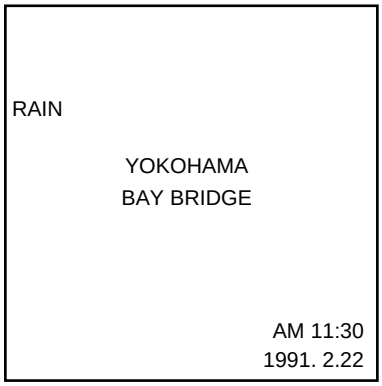
- The RGB channel does not output the characters for which the V_{C2} channel has been specified.

Characters output via V_{C1} channel (all rows)



- The V_{C1} channel outputs the characters of all rows regardless of the setting of the V_{C1} bit, excluding the characters for which the V_{C2} channel is specified.

Characters output via V_{C2} channel (specified characters of specified rows)



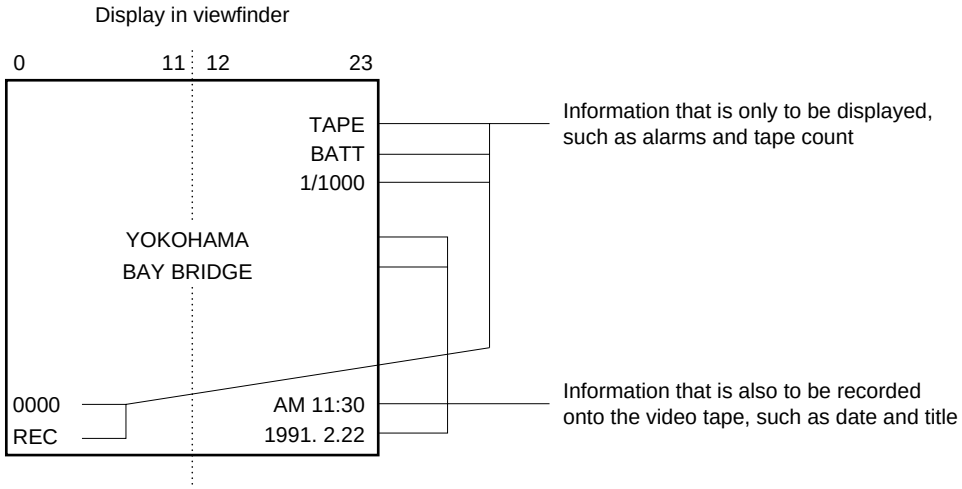
- The V_{C2} channel outputs only those characters for which the V_{C2} channel has been specified in those rows for which the V_{C1} bit has been set to 1.
- The V_{C2} channel outputs no characters in those rows for which the V_{C1} bit has been set to 0.

1.4.3 Character Signal Output When Option C is Selected

Option C

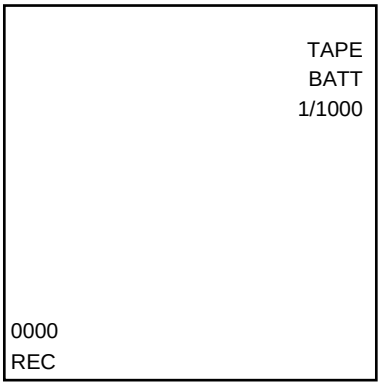
The V_{C1} and V_{C2} bits of the output pin control command can be used to specify whether the characters in columns 0 to 11 of each row and those in columns 12 to 23 are output to the V_{C1} channel or to the V_{C2} channel.

Display example



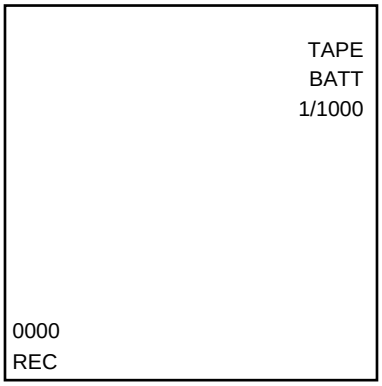
Output example with mask code option C specified

Characters output via RGB channel (colored characters)



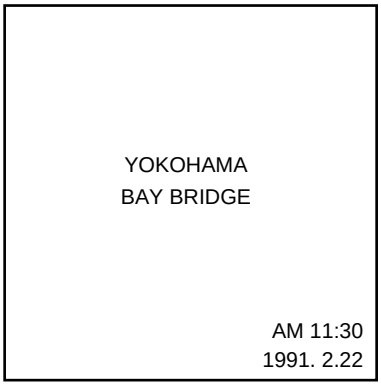
- The RGB channel does not output the characters for which the V_{C2} channel has been specified.

Characters output via V_{C1} channel (specified rows)



- In the case of setting V_{C2} bit to 0, the V_{C1} channel outputs the characters of columns 0 to 23 in specified rows for which the V_{C1} bit is set to 0, or the characters of columns 0 to 11 in specified rows for which the V_{C1} bit is set to 1, excluding the characters for which the V_{C2} channel specified.
- In the case of setting V_{C2} bit to 1, the V_{C1} channel outputs the characters of columns 12 to 23 in specified rows for which the V_{C1} bit is set to 0, and the rows for which the V_{C1} bit is set to 1 are not output (the V_{C1} pin is fixed to low level), excluding the characters for which the V_{C2} channel specified.

Characters output via V_{C2} channel (specified characters)

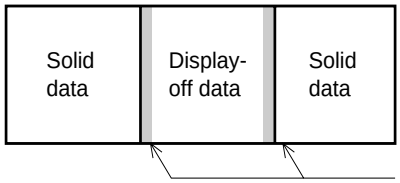


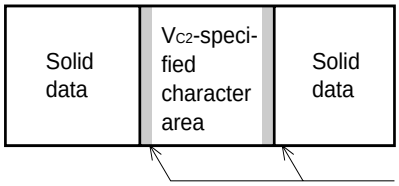
- In the case of setting V_{C1} bit to 0, the V_{C2} channel outputs the characters of columns 0 to 11 in specified rows for which the V_{C2} bit is set to 1, and the rows for which the V_{C2} bit is set to 0 are not output (the V_{C2} pin is fixed to low level).
- In the case of setting V_{C1} bit to 1, the V_{C2} channel outputs the characters of columns 12 to 23 in specified rows for which the V_{C2} bit is set to 0, or the characters of columns 0 to 23 in specified rows for which the V_{C2} bit is set to 1.

1.4.4 Display of V_{C2}-Specified Characters

When the displayed character control command specifies the V_{C2} channel for a character, that character is not output to the RGB or V_{C1} channel (display for the RGB and V_{C1} channels is usually the same as when display-off data is written[Note]). If background display (overall/minimum) is specified for the RGB or V_{C1} channel, no background is displayed for those characters for which the V_{C2} channel has been specified.

Note In some cases, the display will differ slightly from the display-off data.





Solid data: Character for which all 12 × 18 dots are filled

- When display-off data is displayed for the RGB, V_{C1}, or V_{C2} channel

  If a character adjacent to the display-off data is rimmed or has a background, the rim or background encroaches into the area for the display-off data by one dot (minimum size). (The rim encroaches only at the filled dots at the left or right edge of the rimmed character.)

- Display of V_{C2}-specified character area for the RGB or V_{C1} channel

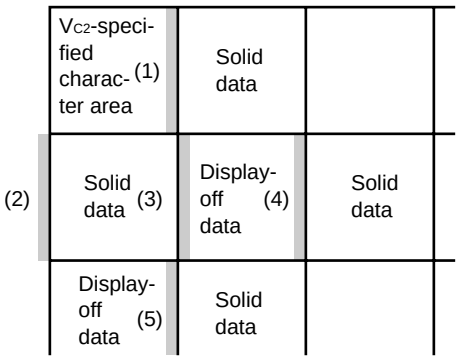
  If a character adjacent to a V_{C2}-specified character is rimmed, the rim encroaches into the area for the V_{C2}-specified character by one dot (minimum size). If the adjacent character has a background, however, the background does not encroach into the V_{C2}-specified character area.

- Display of V_{C2}-specified character area for the V_{C2} channel

  If a rimmed V_{C2}-specified character is adjacent to another V_{C2}-specified character, the rim encroaches into the area for the latter V_{C2}-specified character. The background does not encroach into the adjacent area (The rim encroaches only at the filled dots on the left or right edge of the rimmed character).

- When a V_{C2}-specified character area exists at the right or left edge of the entire display area

  (The figure shows an area at the left edge. The case of an area at the right edge is similar).



Encroachment of rim or background
(with a width of one dot for the minimum character size)

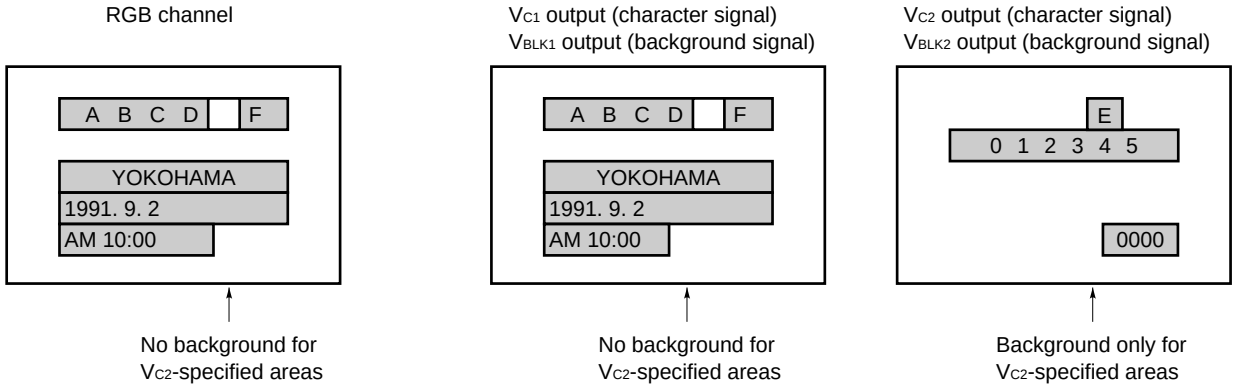
Encroachment of rim	Encroachment of background
(1) – (5)	(2) – (5)

Background does not encroach into the V_{C2}-specified character area.

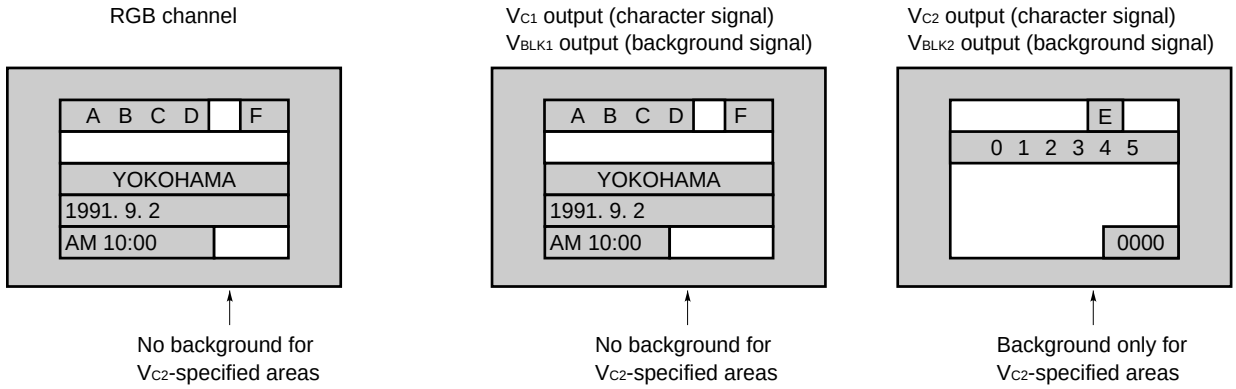
1.5 OUTPUTTING BACKGROUND

The figures below show the screen display when minimum background or overall background is specified for each output channel in RGB+V_{C1}+V_{C2} mode.

(1) Minimum background



(2) Overall background



Remarks 1. The above figures are only examples. Actually, the background can be controlled independently for each output channel (only in RGB+V_{C1}+V_{C2} mode), for example, by applying background (overall/minimum) for the RGB channel but not for the other channels.

2. No background is applied to the V_{C2}-specified areas for the RGB or V_{C1} channel. If a character adjacent to a V_{C2}-specified character is rimmed, the rim encroaches into the area for the V_{C2}-specified character by one dot (minimum size) only at the filled dots at the left or right edge of the area of the rimmed character, in the same way as for display-off data. The background, however, does not encroach into the adjacent area.

2. COMMANDS

2.1 COMMAND FORMAT

Control commands are serially input in 8-bit units with a variable word length. There are three types of commands: 1-byte commands consisting of eight bits including an instruction and data, 2-byte commands consisting of sixteen bits including an instruction and data, and a 2-byte continuous command which can be input in an abbreviated format. Commands are input with the MSB first or LSB first according to the specified mask option.

2.2 COMMANDS AND THEIR BITS

(1) For MSB first

1-byte commands

(MSB)

Function	D7	D6	D5	D4	D3	D2	D1	D0
Video RAM batch clear	0	0	0	0	0	0	0	0
Character display control	0	0	0	1	D0	LC	BL1	BL0
Background/rim color control	0	0	1	0	R	G	B	BFC
3-channel independent display on/off	0	1	1	1	0	DOA	DOB	DOC
Character reverse on/off	0	0	1	1	1	0	0	BCRE

2-byte commands

(MSB)

Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Character display position control	1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0
Write address control	1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0
Output pin control	1	0	0	1	1	1	0	0	V_{C2}	V_{C1}	0	0	AR3	AR2	AR1	AR0
Character size control	1	0	0	1	1	0	0	0	0	S	0	0	AR3	AR2	AR1	AR0
3-channel independent background control	1	0	1	1	0	0	1	BA1	BA0	BFA	BB1	BB0	BFB	BC1	BC0	BFC
Test mode[Note]	1	0	1	1	0	0	0	T8	T7	T6	T5	T4	T3	T2	T1	T0

Note Not to be used

2-byte continuous command

(MSB)

Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Displayed character control	1	1	RV	R	G	B	BL	V_{C2}	C7	C6	C5	C4	C3	C2	C1	C0
									Note							

Note C7 bit is “don’t care” at the μPD6462. However, this data sheet explains the μPD6462 with “0” in the C7 bit.

(2) For LSB first

1-byte commands

(LSB)

Function	D0	D1	D2	D3	D4	D5	D6	D7
Video RAM batch clear	0	0	0	0	0	0	0	0
Character display control	BL0	BL1	LC	DO	1	0	0	0
Background/rim color control	BFC	B	G	R	0	1	0	0
3-channel independent display on/off	DOC	DOB	DOA	0	1	1	1	0
Character reverse on/off	BCRE	0	0	1	1	1	0	0

2-byte commands

(LSB)

Function	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Character display position control	V3	V4	0	0	0	0	0	1	H0	H1	H2	H3	H4	V0	V1	V2
Write address control	AR3	0	0	1	0	0	0	1	AC0	AC1	AC2	AC3	AR4	AR0	AR1	AR2
Output pin control	0	0	1	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	V_{C1}	V_{C2}
Character size control	0	0	0	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	S	0
3-channel independent background control	BA1	1	0	0	1	1	0	1	BFC	BC0	BC1	BFB	BB0	BB1	BFA	BA0
Test mode[Note]	T8	0	0	0	1	1	0	1	T0	T1	T2	T3	T4	T5	T6	T7

Note Not to be used

2-byte continuous command

(LSB)

Function	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Displayed character control	V_{C2}	BL	B	G	R	RV	1	1	C0	C1	C2	C3	C4	C5	C6	C7

Note

Note C7 bit is “don’t care” at the μPD6462. However, this data sheet explains the μPD6462 with “0” in the C7 bit.

2.3 POWER-ON CLEAR FUNCTION

The internal state of the IC is unstable immediately after the power is turned on. It is therefore necessary to keep the $\overline{PCL}$ pin low for the time shown below to allow the system to initialize. This power-on clear places the system in the following state:

- Test mode is not specified.
- All character data in video RAM (12 rows × 24 columns) is cleared (to display-off data (FEH: μPD6461/7EH: μPD6462)) and blinking is turned off.
- The video RAM write address is (row 0, column 0).
- The character size is single (minimum) for all rows.
- The output distribution format is set to the default (the V_{C1} and V_{C2} bits are set to 0).
- Display is turned off and LC oscillation is turned on.

The time required for power-on clear is calculated as follows. No commands must be input during this time.

Time required for power-on clear = t_{PCLL}**Note** + {Time required for clearing video RAM}
= 10(μs) + {10(μs) + 12/f_{OSC}(MHz) × 288}

f_{OSC}(MHz) : LC oscillation frequency or external clock frequency

Note Refer to **POWER-ON CLEAR SPECIFICATIONS** in **6. ELECTRICAL CHARACTERISTICS**.

A dot clock input (to the OSC_{IN} pin) is necessary to clear video RAM. Input a dot clock when an external clock input is selected.

3. COMMAND DETAILS

3.1 VIDEO RAM BATCH CLEAR COMMAND

This command clears the entire video RAM by means of a single operation (the bit configuration is the same as for MSB-first and LSB-first transfer).

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

The video RAM batch clear command places the system in the following state:

- All character data in video RAM (12 rows × 24 columns) is cleared (to display-off data (FEH: μPD6461/7EH: μPD6462)) and blinking is turned off.
- The video RAM write address is (row 0, column 0).
- The character size is single (minimum) for all rows.
- The output distribution format is set to the default (the V_{C1} and V_{C2} bits are set to 0).
- Display is turned off and LC oscillation is turned on.

The time required for clearing video RAM is calculated as follows. No command must be input while the video RAM is being cleared.

Time required to clear video RAM = $10(\mu s) + 12/f_{OSC}(MHz) \times 288$

f_{OSC}(MHz) : LC oscillation frequency or external clock frequency

A dot clock input (to the OSC_{IN} pin) is necessary to clear the video RAM. Input a dot clock when external clock input is selected.

Remark Power-on clear using the $\overline{PCL}$ pin is hardware reset, initializing the IC, including clearing the video RAM and releasing test mode. The video RAM batch clear command, in contrast, performs software reset by initializing the IC without first releasing test mode.

3.2 CHARACTER DISPLAY CONTROL COMMAND

This command turns on/off character display, LC oscillation, and the blinking of characters.

(1) For MSB-first transfer (Command bits are input starting from the MSB (D7).)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	DO	LC	BL1	BL0

Blinking control bits		
BL1	BL0	Function
0	0	Turns off blinking.
0	1	Turns on 2 Hz blinking.
1	0	Turns on 1 Hz blinking.
1	1	Turns on 0.5 Hz blinking.

LC oscillation control bit	
LC	Function
0	Turns off LC oscillator.
1	Turns on LC oscillator.

Character display on/off control bit	
DO	Function
0	Turns off character display.
1	Turns on character display.

(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7
BL0	BL1	LC	DO	1	0	0	0

- Blinking control bits

  These bits are used to turn on or off the blinking of characters for which blinking has been enabled with the displayed character control command. The blinking ratio is 1:1, one of three blinking frequencies being selectable for the entire screen.

- LC oscillation control bit

  This bit is used to turn the oscillator on or off. You can stop the oscillator when no character is being displayed, thus reducing the power consumption.

  While the oscillator is stopped, it is not possible to write to video RAM. Turn on the oscillator before attempting to write to video RAM.

Cautions 1. When using LC oscillation (LC oscillation control bit = 1): When character display is turned on, the oscillation is synchronized with $\overline{\text{Hsync}}$, stopping when $\overline{\text{Hsync}}$ goes low. When character display is turned off, oscillation continues regardless of the state of $\overline{\text{Hsync}}$.

2. When using an external clock (LC oscillation control bit = 1): While the oscillator is turned on, clock pulses are supplied to the IC internal circuit. While the oscillator is turned off, no clock pulses are supplied.

- Character display on/off control bit

  This bit is used to turn character display on or off. Character display is turned on or off upon the detection of a falling edge of $\overline{\text{Hsync}}$.

3.3 BACKGROUND/RIM COLOR CONTROL COMMAND

This command specifies the color of the background or rim when overall background, minimum background, or rimming is specified.

(1) For MSB-first transfer (Command bits are input starting from the MSB (D7).)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	R	G	B	BFC

Rim color specification bit	
BFC	Color
0	Black
1	White

Background color specification bits			
R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7
BFC	B	G	R	0	1	0	0

- Rim color specification bit

  This bit is used to specify the color (white or black) of the rim added to all characters displayed on the screen (only for the RGB channel). When rimming is specified for the V_{C1} or V_{C2} channel, the rim color is always black.

- Background color specification bits

  These bits are used to specify one of eight colors to be used for the background of the entire screen (only for the RGB channel). When background (overall/minimum) is specified for the V_{C1} or V_{C2} channel, the background color is always black.

3.4 3-CHANNEL INDEPENDENT DISPLAY ON/OFF COMMAND

This command turns character display on or off independently for each of the three channels.

(1) For MSB-first transfer (Command bits are input starting from the MSB (D7).)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	DOA	DOB	DOC

When RGB+V_{C1}+V_{C2} mode is selected

Control bits		Function
DOA	0	Turns off display for RGB channel.
	1	Turns on display for RGB channel.
DOB	0	Turns off display for V_{C1} channel.
	1	Turns on display for V_{C1} channel.
DOC	0	Turns off display for V_{C2} channel.
	1	Turns on display for V_{C2} channel.

When RGB+3BLK mode is selected

Control bits		Function
DOA	0	Turns off character display (for all channels).
	1	Turns on character display (for all channels).
DOB	–	Don't care
DOC	–	Don't care

(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7
DOC	DOB	DOA	0	1	1	1	0

3.5 CHARACTER REVERSE ON/OFF COMMAND

This command specifies whether all characters displayed on the screen are reversed.

(1) For MSB-first transfer (Command bits are input starting from the MSB (D7).)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	BCRE

Control bit		Function
BCRE	0	Does not reverse characters.
	1	Reverses characters.

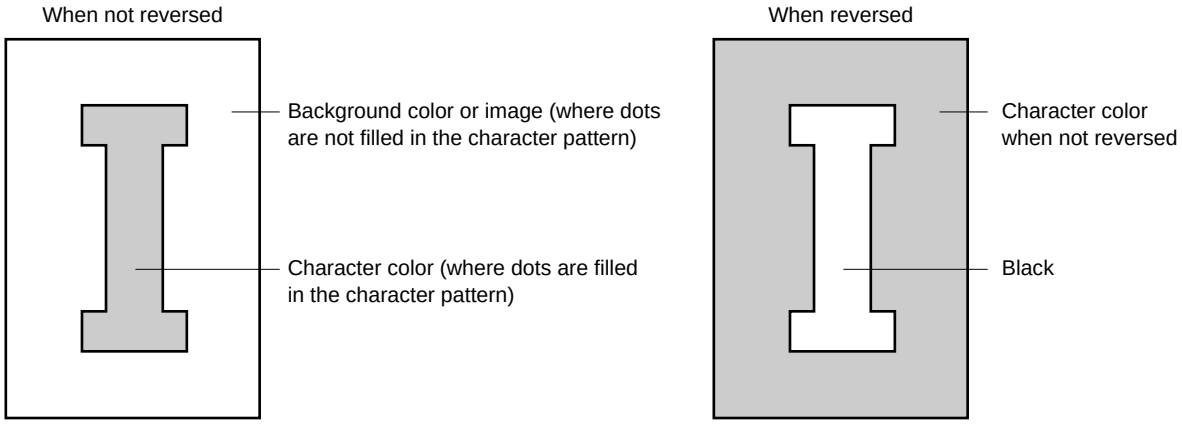
(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7
BCRE	0	0	1	1	1	0	0

Each character is reversed only when reversing of the character is enabled with the displayed character control command.

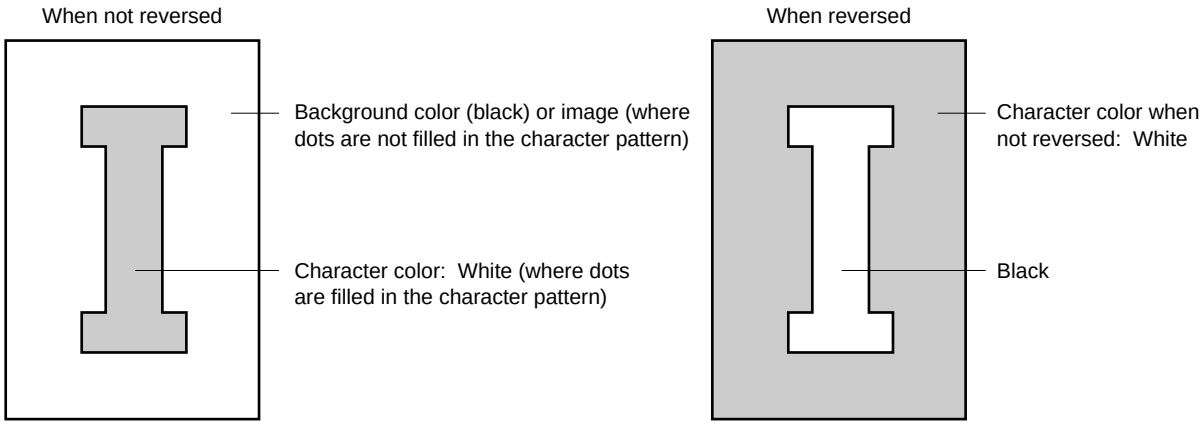
- **Example of reversed character (uppercase letter “I”)**



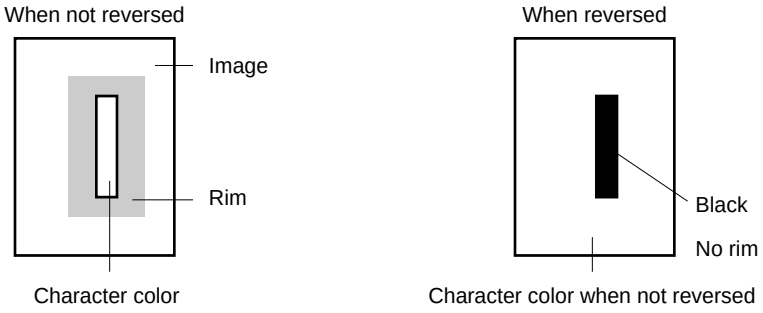
Remark When the character is not reversed, one of eight colors can be selected for the background color for the RGB channel. For the V_{C1} and V_{C2} channels, which can display only white or black, the background is always black (characters are white).

When characters are rseversed for the V_{C1} or V_{C2} channel, the display is as follows:

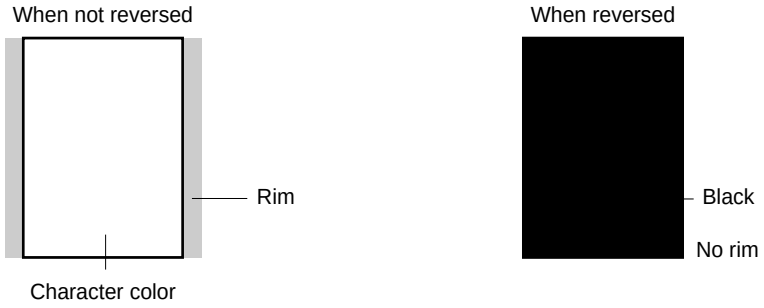
- **Example of reversed character for V_{C1} or V_{C2} channel (uppercase letter “I”)**



- **Rimming of reversed character**
  For an ordinary character



For a solid character (character pattern 18H (μPD6461)/1FH (μPD6462): Refer to 5. CHARACTER PATTERNS)



Display-off data does not change when reversed. When blank data is reversed, it becomes a solid character for which the character color is initially set. The character color can be set only for the RGB channel. It is always white (black when reversed) for the V_{C1} and V_{C2} channels.

3.6 CHARACTER DISPLAY POSITION CONTROL COMMAND

This command specifies the character display start position with one of 32 steps in 12-dot units for the horizontal direction, and one of 32 steps in three-line units for the vertical direction (this command is a 2-byte command, requiring 16 bits for each command even when continuously input).

(1) For MSB-first transfer (Command bits are input starting from the MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0

Control bits for horizontal display start position					
H4	H3	H2	H1	H0	Start position
0	0	0	0	0	$(4 + 12 \times 1)/f_{OSC}$ (MHz) from rising edge of Hsync (μs)
0	0	0	0	1	$(4 + 12 \times 2)/f_{OSC}$ (MHz) from rising edge of Hsync (μs)
≈	≈	≈	≈	≈	≈
1	1	1	1	1	$(4 + 12 \times 32)/f_{OSC}$ (MHz) from rising edge of Hsync (μs)

Remarks f_{OSC}: LC oscillation frequency or external input clock

Control bits for vertical display start position					
V4	V3	V2	V1	V0	Start position
0	0	0	0	0	$3H \times 0 + 1H$ $(9H \times 0 + 1H)$ from rising edge of $\overline{Vsync}$
0	0	0	0	1	$3H \times 1 + 1H$ $(9H \times 1 + 1H)$ from rising edge of $\overline{Vsync}$
≈	≈	≈	≈	≈	≈
1	1	1	1	1	$3H \times 31 + 1H$ $(9H \times 31 + 1H)$ from rising edge of $\overline{Vsync}$

Remarks 1. H: Line

2. ( ) shows when units of nine lines are selected by specifying a mask option.

(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

(LSB) (MSB)

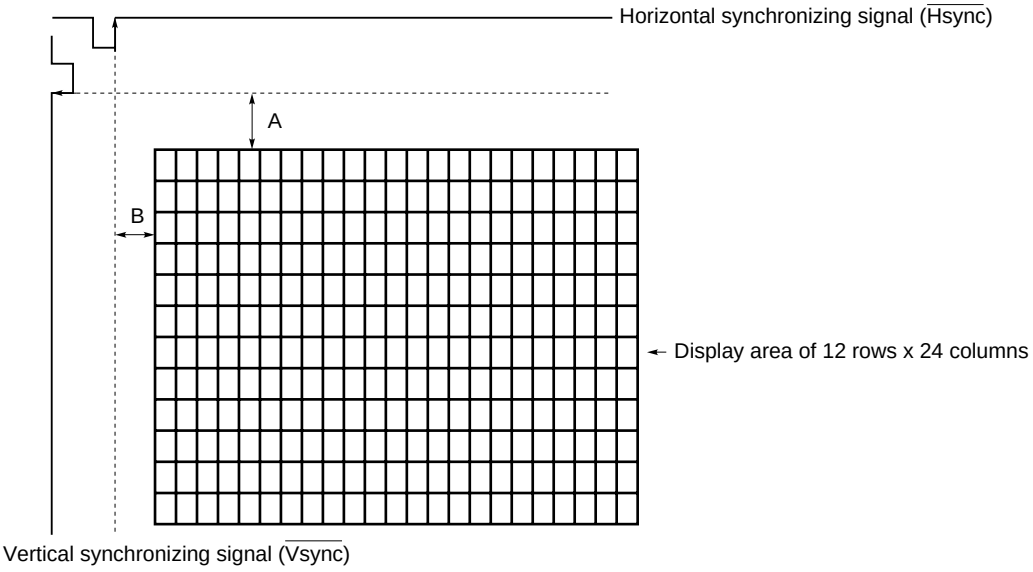
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
V3	V4	0	0	0	0	0	1	H0	H1	H2	H3	H4	V0	V1	V2

- Control bits for the horizontal display start position

  These bits are used to specify the horizontal display start position (timing) as one of 32 steps in units of 12 dots (12/fosc (MHz)). Settable positions are based on the rising edge of the horizontal synchronizing signal input to the $\overline{\text{Hsync}}$ pin. The 32 positions are calculated by adding 12 dots, one to 32 times, to the position equivalent to 16 clock pulses (16/fosc (MHz)) from the rising edge (fosc (MHz): LC oscillation frequency or external input clock frequency).

- Control bits for the vertical display start position

  These bits are used to specify the vertical display start position as one of 32 steps in units of three lines (or 32 steps in units of nine lines when specified with a mask option). The minimum settable position is three lines from a rising edge of the vertical synchronizing signal input to the $\overline{\text{Vsync}}$ pin.



A : $3H \times (2^4V4+2^3V3+2^2V2+2^1V1+2^0V0)+1H$

9H when units of nine lines are selected by specifying a mask option

$$B : \frac{12}{f_{osc}(MHz)} \times (2^4H4+2^3H3+2^2H2+2^1H1+2^0H0+1) + \frac{4}{f_{osc}(MHz)}$$

fosc : LC oscillation frequency or external input clock frequency H : Line

3.7 WRITE ADDRESS CONTROL COMMAND

This command specifies the address at which a character is written in the display area (video RAM) of 12 rows × 24 columns (this command is a 2-byte command, requiring 16 bits for each command, even when continuously input).

(1) For MSB-first transfer (Command bits are input starting from the MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0

Column address specification bits					
AC4	AC3	AC2	AC1	AC0	Column
0	0	0	0	0	Column 0
0	0	0	0	1	Column 1
≈	≈	≈	≈	≈	≈
1	0	1	1	1	Column 23
Any other value is invalid.					

Column address specification bits				
AR3	AR2	AR1	AR0	Row address specification bits
0	0	0	0	Row
0	0	0	1	Row 0
≈	≈	≈	≈	Row 1 ≈
1	0	1	1	Row 11
Any other value is invalid.				

(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
AR3	0	0	1	0	0	0	1	AC0	AC1	AC2	AC3	AR4	AR0	AR1	AR2

- Column write address specification bits

  The display area has 24 columns. These bits are used to specify the column in which a character is to be written.
- Row write address specification bits

  The display area has 12 rows. These bits are used to specify the row in which a character is to be written.

3.8 OUTPUT PIN CONTROL COMMAND

This command distributes character signals to the V_{C1} and V_{C2} channels (this command is a 2-byte command, requiring 16 bits for each command, even when continuously input). The μPD6461, 6462 support a mask option for selecting one of three formats for the output distribution format for the V_{C1} and V_{C2} channels.

(1) For MSB-first transfer (Command bits are input starting from the MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	1	0	0	V_{C2}	V_{C1}	0	0	AR3	AR2	AR1	AR0

Row specification bits				
AR3	AR2	AR1	AR0	Function
0	0	0	0	Specifies row 0.
0	0	0	1	Specifies row 1.
≈	≈	≈	≈	≈
1	0	1	1	Specifies row 11.
Other values are invalid.				

Option A

Output pin control bits		
V_{C2}	V_{C1}	Output from each pin
0	0	V_{C1}: Outputs a specified row. V_{C2}: Fixed to low level.
0	1	V_{C1}: Fixed to low level. V_{C2}: Outputs a specified row.

Option B

Output pin control bits		
V_{C2}	V_{C1}	Output from each pin
0	0	V_{C1}: Outputs all rows. V_{C2}: Fixed to low level.
0	1	V_{C1}: Outputs all rows. V_{C2}: Outputs a specified row.

Option C

Output pin control bits		
V_{C2}	V_{C1}	Output from each pin
0	0	V_{C1}: Outputs columns 0 to 23. V_{C2}: Fixed to low level.
0	1	V_{C1}: Outputs columns 0 to 11. V_{C2}: Outputs columns 12 to 23.
1	0	V_{C1}: Outputs columns 12 to 23. V_{C2}: Outputs columns 0 to 11.
1	1	V_{C1}: Fixed to low level. V_{C2}: Outputs columns 0 to 23.

(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	1	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	V_{C1}	V_{C2}

- Row specification bits

  Output distribution to the V_{C1} and V_{C2} pins is specified for each row (or for 12 columns). These bits are used to specify the row.

- Output pin control bits

  These bits are used to distribute character output signals to the V_{C1} and V_{C2} pins depending on whether option A, B, or C has been selected by specifying a mask option (the corresponding blanking signals are output likewise).

3.9 CHARACTER SIZE CONTROL COMMAND

This command specifies the character size (height and width at one time) for each row (this command is a 2-byte command, requiring 16 bits for each command, even when continuously input).

(1) For MSB-first transfer (Command bits are input starting from the MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0	0	S	0	0	AR3	AR2	AR1	AR0

Row specification bits				
AR3	AR2	AR1	AR0	Row
0	0	0	0	Row 0
0	0	0	1	Row 1
≈	≈	≈	≈	≈
1	0	1	1	Row 11
Any other value is invalid.				

Character size specification bit	
S	Size
0	Height: One dot per line. Width: One dot per 1t (minimum dot).
1	Height: One dot per two lines. Width: One dot per 2t.

$$1t\ (\mu s) = \frac{1}{f_{osc}(MHz)}$$

(f_{osc} : LC oscillation frequency

(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	0	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	S	0

- Row specification bits

  The character size is specified for each row. These bits are used to specify the row.
- Character size specification bit

  This bit is used to select either of two supported sizes.

3.10 3-CHANNEL INDEPENDENT BACKGROUND CONTROL COMMAND

This command specifies the background for each of the three output channels (this command is a 2-byte command, requiring 16 bits for each command, even when continuously input).

(1) For MSB-first transfer (Command bits are input starting from the MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	1	BA1	BA0	BFA	BB1	BB0	BFB	BC1	BC0	BFC

V_{C2} output

Background control bits for V_{C2} channel		
BC1	BC0	Background
0	0	No background
0	1	Minimum background
1	0	Not to be set
1	1	Overall background

Rimming control bit for V_{C2} channel	
BFC	Function
0	Does not rim characters.
1	Rims characters.

V_{C1} output

Background control bits for V_{C1} channel		
BB1	BB0	Background
0	0	No background
0	1	Minimum background
1	0	Not to be set
1	1	Overall background

Rimming control bit for V_{C1} channel	
BFB	Function
0	Does not rim characters.
1	Rims characters.

RGB output

Background control bits for RGB channel		
BA1	BA0	Background
0	0	No background
0	1	Minimum background
1	0	Not to be set
1	1	Overall background

Rimming control bit for RGB channel	
BFA	Function
0	Does not rim characters.
1	Rims characters.

(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

(LSB) (MSB)

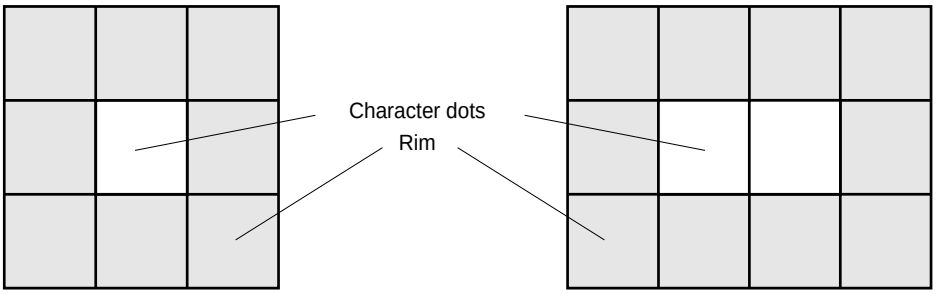
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
BA1	1	0	0	1	1	0	1	BFC	BC0	BC1	BFB	BB0	BB1	BFA	BA0

- Rimming control bit

  This bit is used to specify whether all characters displayed on the screen are rimmed.

Rimming: Whenever there is a dot at the right or left edge of the display area for a character, rimming of the dot will encroach into the adjacent character display area. For dots at the top or bottom edge, however, no rim is added either above the top edge or below the bottom edge, that is, rimming does not encroach into the character display area above or below. Other dots are rimmed as shown below.

Example



The width of a rim is always 1t (minimum dot) regardless of the character size.

- Background control bits

  These bits are used to select no background, minimum background, or overall background as the background type. The background color is specified with the background/rim color control command.

  No background: Outputs only character data.
  Minimum background: Adds a background of an area that is wider than the character display area by a minimum of one dot at each side.
  Overall background: Adds a background over the entire screen.

- Background and rimming in RGB+V_{C1}+V_{C2} mode

  Characters for which the V_{C2} channel is specified with the displayed character control command are not output to the RGB or V_{C1} channel. When background (minimum/overall) is specified for the RGB or V_{C1} channel, no background is added to the areas for the V_{C2}-specified characters. By contrast for the V_{C2} channel, a background is added only to those areas for V_{C2}-specified characters. (Refer to **1.4 DISPLAY IN RGB+V_{C1}+V_{C2} MODE** and **1.4.4 Display of V_{C2}-Specified Characters** for details of the display of V_{C2}-specified character areas for the RGB or V_{C1} channel.)

  When RGB+3BLK (RGB compatible blanking) mode is selected, only the background control bits for the RGB channel are valid. Those for the V_{C1} and V_{C2} channels are invalid (In RGB+3BLK mode, no pin outputs a signal for the V_{C2} channel. The V_{C1} pin is used to output the logical OR of the R, G, and B outputs.).

3.11 TEST MODE COMMAND

This command is used only to test the IC. Usually, do not input this command. The system cannot enter test mode while the TEST pin (pin 9) is connected to ground.

(1) For MSB-first transfer (Command bits are input starting from the MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	T8	T7	T6	T5	T4	T3	T2	T1	T0

(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

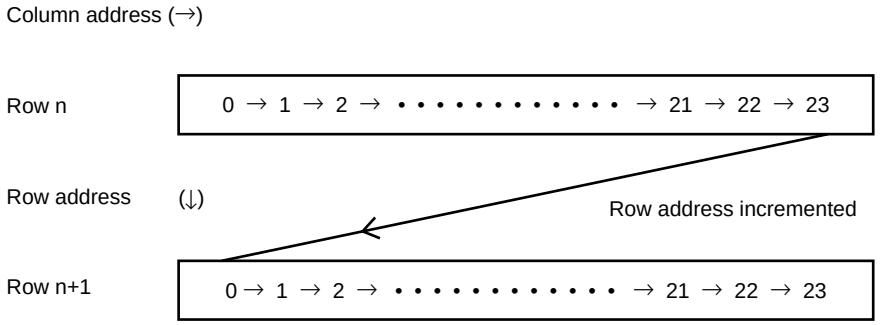
(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
T8	0	0	0	1	1	0	1	T0	T1	T2	T3	T4	T5	T6	T7

3.12 DISPLAYED CHARACTER CONTROL COMMAND

This command specifies the attributes of each character, including the character pattern, color, and whether it is blinked. When inputting this command, ensure that LC oscillator is turned on (if the LC oscillator is turned off, it is not possible to write to video RAM).

This command is a 2-byte continuous command. When continuously writing characters with the same attributes (except for a pattern), you need input only the eight low-order bits (D0 to D7) of the command for the second and subsequent characters. In this case, the write column address is automatically incremented (After a character has been written into column 23, the next character is automatically written into left-most column 0 of the next row. When a character is written into column 23 of row 11, the next character is automatically written into column 0 of row 0.).



(1) For MSB-first transfer (Command bits are input starting from the MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	RV	R	G	B	BL	V_{C2}	C7[Note]	C6	C5	C4	C3	C2	C1	C0

Character pattern specification bits								
C7[Note]	C6	C5	C4	C3	C2	C1	C0	Function
0	0	0	0	0	0	0	0	Outputs pattern at address 00H.
0	0	0	0	0	0	0	1	Outputs pattern at address 01H.
≈	≈	≈	≈	≈	≈	≈	≈	≈
1	1	1	1	1	1	1	0	FEH (μPD6461)/7EH (μPD6462) (display-off data).
1	1	1	1	1	1	1	1	FFH (μPD6461)/7FH (μPD6462) (Indicates the end of second-byte continuous input.)

V_{C2} channel specification bit	
V_{C2}	Function
0	Does not specify output to V_{C2} channel.
1	Specifies output to V_{C2} channel.

Blinking control bit	
BL	Function
0	Disables blinking.
1	Enables blinking.

Character color specification bits			
R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Reversing control bit	
RV	Function
0	Disables reversing.
1	Enables reversing.

Note C7 bit is “don’t care” at the μPD6462. However, this data sheet explains the μPD6462 with “0” in the C7 bit.

(2) For LSB-first transfer (Command bits are input starting from the LSB (D0). The function of each bit is the same as that for MSB-first transfer.)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
V_{C2}	BL	B	G	R	RV	1	1	C0	C1	C2	C3	C4	C5	C6	C7

- Character pattern specification bits

  These bits are used to specify the address of the character pattern to be used. Address FEH (μPD6461)/7EH (μPD6462) indicates display-off data and address FFH (μPD6461)/7FH (μPD6462) indicates the end code for second-byte continuous input. The design of each character pattern can be modified by specifying a mask code option (except for addresses FEH and FFH (μPD6461)/7EH and 7FH (μPD6462)).

- V_{C2} channel specification bit

  This bit is used to specify whether each character is output to the V_{C2} channel. Characters for which the V_{C2} channel is specified are not output to the RGB or V_{C1} channel (This bit is invalid in RGB+3BLK mode).

- Blinking control bit

  This bit is used to enable or disable blinking for each character. Blinking of characters is turned on/off for the entire screen with the character display control command (refer to **3.2 CHARACTER DISPLAY CONTROL COMMAND**).

- Character color specification bits

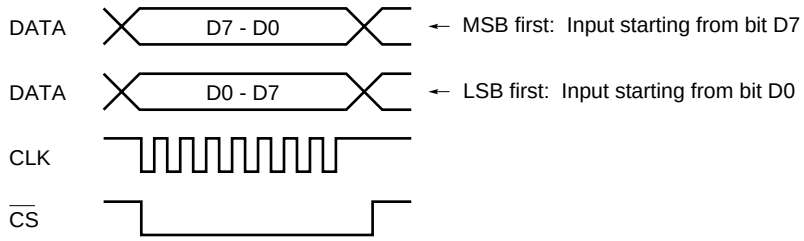
  These bits are used to specify the color of each character (These bits are valid only for the RGB channel. Only a single color can be used for the V_{C1} and V_{C2} channels).

- Reversing control bit

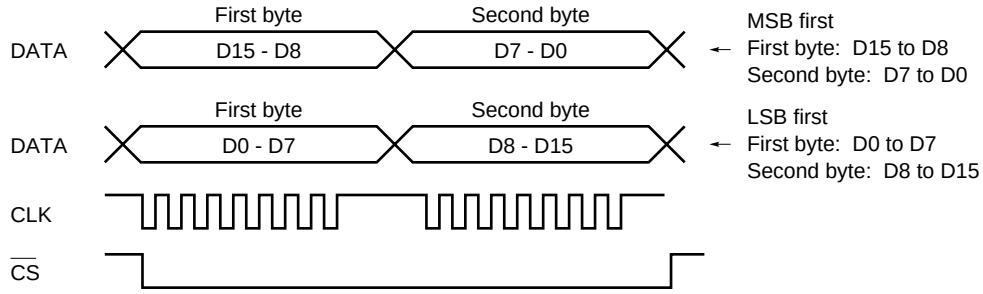
  This bit is used to enable or disable reversing for each character. The characters of the entire screen are reversed with the character reverse on/off command (refer to **3.5 CHARACTER REVERSE ON/OFF COMMAND**).

4. COMMAND TRANSFER

4.1 1-BYTE COMMANDS

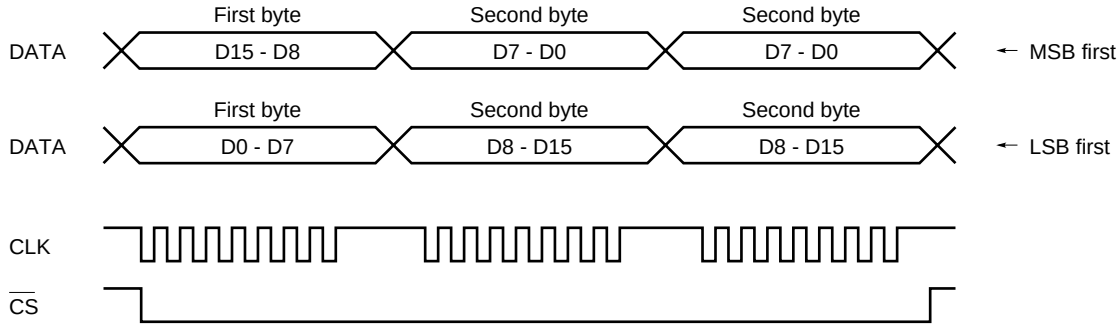


4.2 2-BYTE COMMANDS



When inputting a 2-byte command, keep the $\overline{CS}$ signal low between the first and second bytes of the command.

4.3 2-BYTE CONTINUOUS COMMAND



The 2-byte continuous command is used to write characters to video RAM. When continuously writing characters for which the specifications for the color, blinking, reversing, and V_{C2} channel are the same, transfer the first byte of the first command then continuously transfer only the second bytes (character pattern addresses) of the commands.

When changing any part of the first byte, end continuous input (by setting the $\overline{CS}$ signal to high or transferring the end code for second-byte continuous input) then transfer the newly modified first byte.

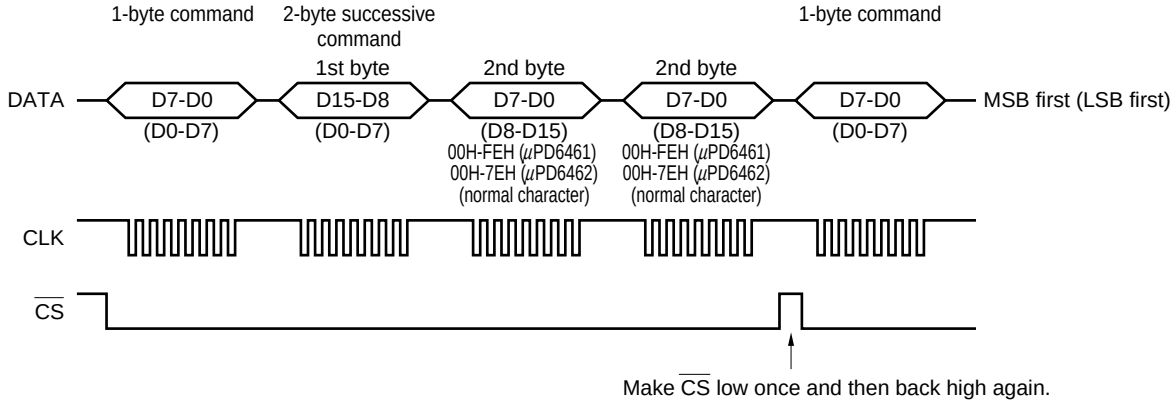
4.4 CONTINUOUS INPUT OF COMMAND

Transfer each of the 1-byte, 2-byte, and 2-byte successive commands from a microcontroller to the μPD6461, 6462 as follows.

To transfer a 1-byte or 2-byte command, or a 2-byte successive command with blinking data changed after a 2-byte successive command has been transferred, either make $\overline{CS}$ high once, or transfer 2-byte successive command end code (FFH: μPD6461/7FH: μPD6462) at the end of the 2-byte successive command. In the latter case, it is not necessary to make $\overline{CS}$ high.

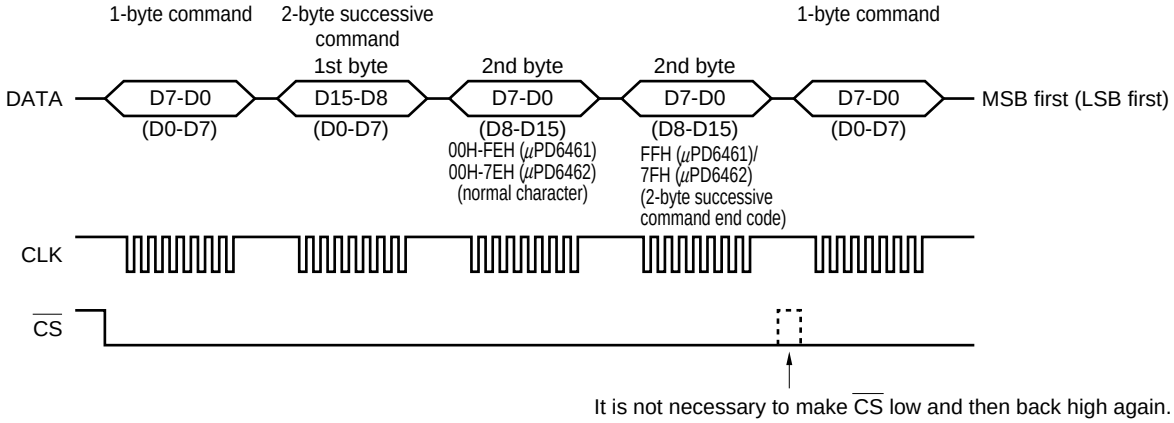
4.4.1 When End Code is Not Used

Example 1-byte command → 2-byte successive command → 1-byte command



4.4.2 When End Code is Used

Example 1-byte command → 2-byte successive command → 1-byte command



Remark By using the 2-byte successive command end code, the $\overline{CS}$ pin may remain low. However, it is recommended to make $\overline{CS}$ pin high to improve the noise immunity.

5. CHARACTER PATTERNS

The μPD6461, 6462 can display 256 (μPD6461)/128 (μPD6462) character patterns, including alphanumerics, Kanji characters, and symbols, which are stored in the character generator ROM. Each pattern in the character generator ROM can be modified by specifying a mask code option. However, the display-off data at character address FEH (μPD6461)/7EH (μPD6462) and end code for second-byte continuous input at FFH (μPD6461)/7FH (μPD6462) cannot be modified. No character pattern can be stored at these addresses.

When none of the 12 × 18 dots are filled for a character pattern at addresses 00H to FDH (μPD6461)/00H to 7DH (μPD6462), the character pattern is called blank data. Character address FEH (μPD6461)/7EH (μPD6462) contains display-off data. Blank data and display-off data are represented in the same way (with no dots filled) in character patterns shown on the following pages, but they are different as follows:

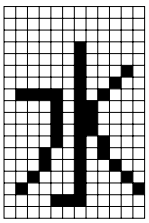
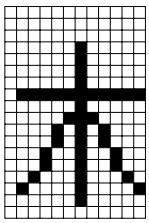
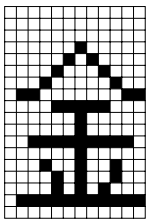
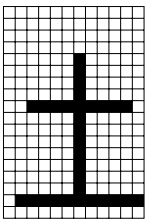
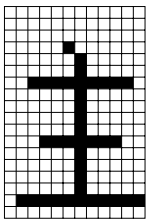
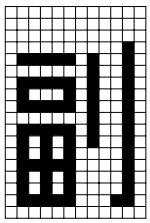
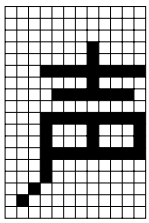
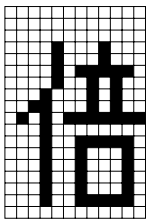
Table 5-1 The Differences between Blank Data and Display-off Data

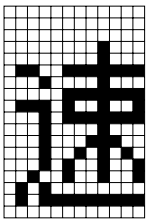
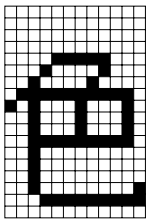
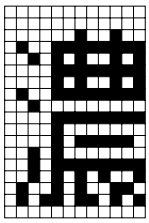
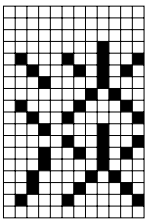
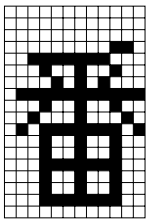
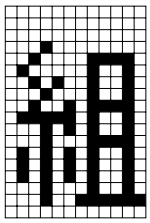
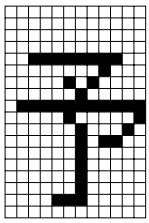
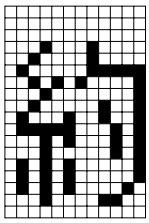
Character data	Display of character area in each background mode		
	No background	Minimum background	Overall background
Blank data	Displays image.	Displays background.	Displays background.
Display-off data	Displays image.	Displays image only (without background).	Displays image only (without background).

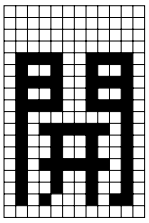
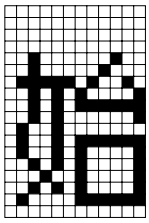
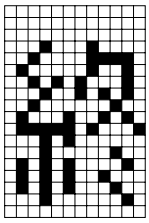
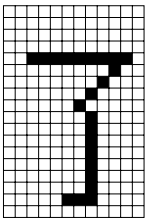
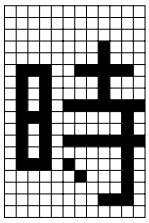
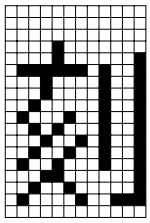
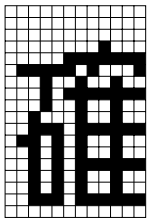
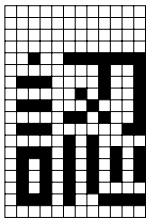
You cannot specify display-off data for addresses other than FEH (μPD6461)/7EH (μPD6462) when using a mask code option. Blank data, however, can be specified at any address from 00H to FDH (μPD6461)/00H to 7DH (μPD6462) (address FFH (μPD6461)/7FH (μPD6462) cannot be used because it contains the end code for second-byte continuous input).

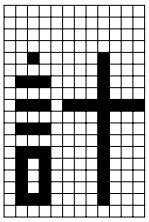
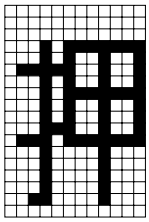
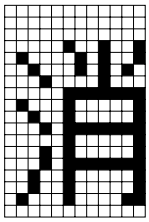
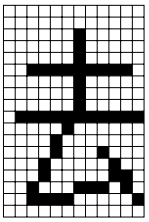
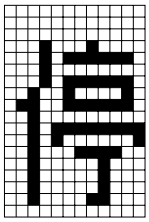
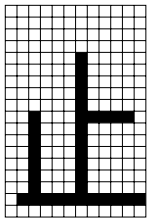
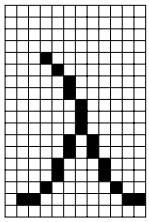
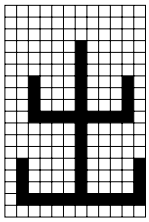
The character patterns of the μPD6461GS-101/102, μPD6462GS-001 (NEC's standard model) are shown on the following pages.

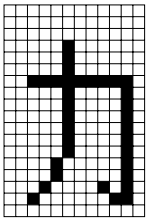
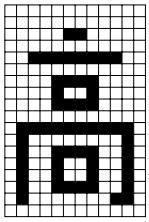
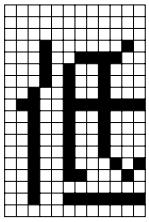
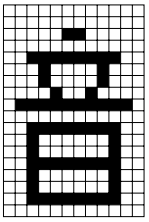
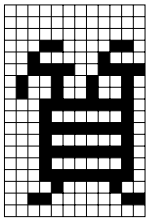
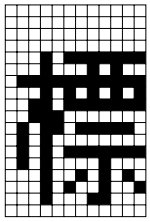
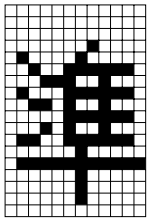
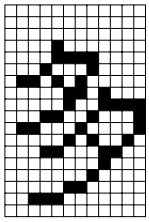
μPD6461GS-101/102 Character Patterns

30H	31H	32H	33H	34H	35H	36H	37H
							

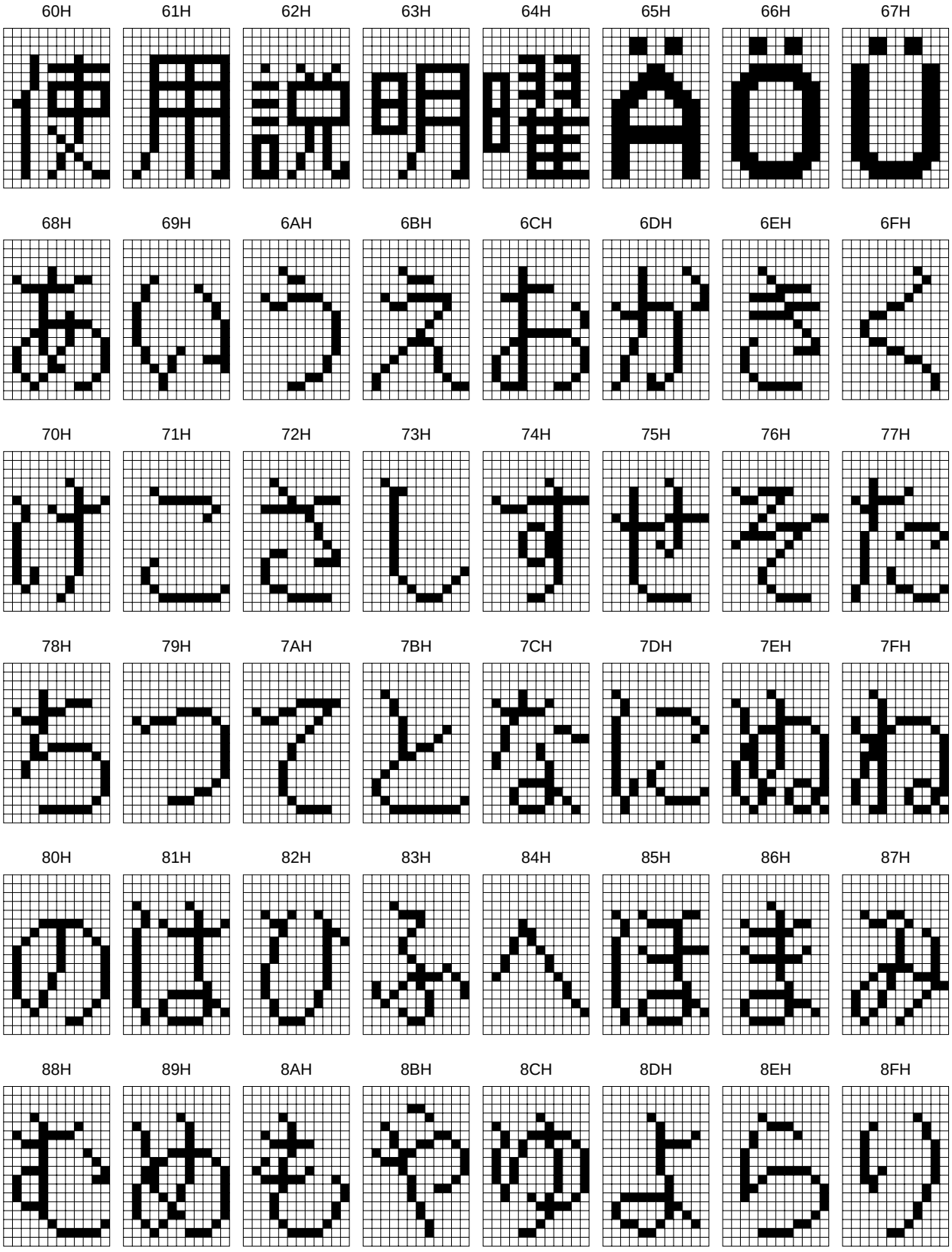
38H	39H	3AH	3BH	3CH	3DH	3EH	3FH
							

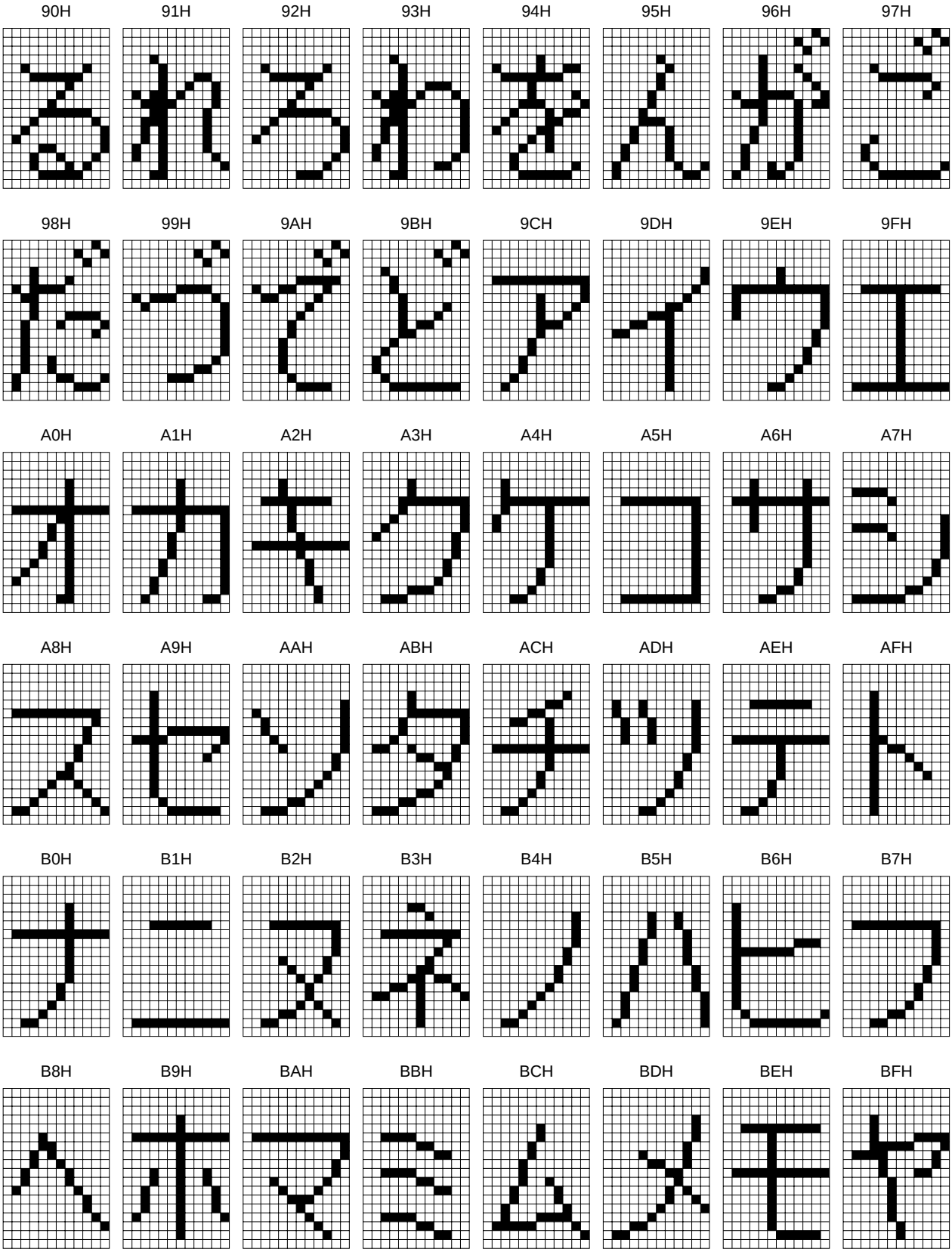
40H	41H	42H	43H	44H	45H	46H	47H
							

48H	49H	4AH	4BH	4CH	4DH	4EH	4FH
							

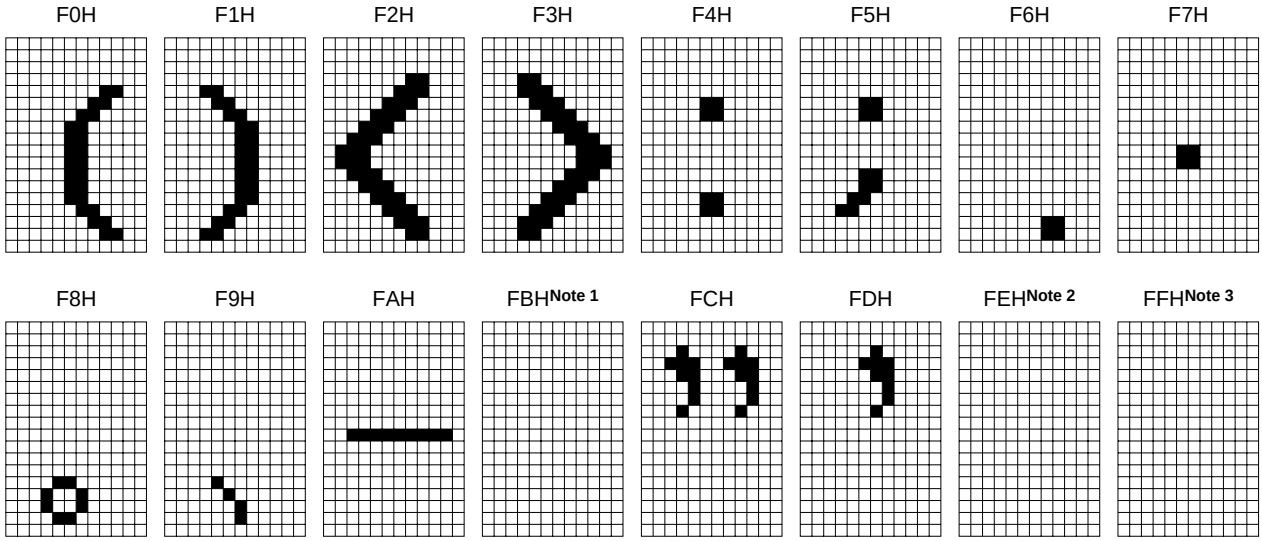
50H	51H	52H	53H	54H	55H	56H	57H
							

58H	59H	5AH	5BH	5CH	5DH	5EH	5FH


60H
61H
62H
63H
64H
65H
66H
67H
68H
69H
6AH
6BH
6CH
6DH
6EH
6FH
70H
71H
72H
73H
74H
75H
76H
77H
78H
79H
7AH
7BH
7CH
7DH
7EH
7FH
80H
81H
82H
83H
84H
85H
86H
87H
88H
89H
8AH
8BH
8CH
8DH
8EH
8FH


90H
91H
92H
93H
94H
95H
96H
97H
98H
99H
9AH
9BH
9CH
9DH
9EH
9FH
A0H
A1H
A2H
A3H
A4H
A5H
A6H
A7H
A8H
A9H
AAH
ABH
ACH
ADH
AEH
AFH
B0H
B1H
B2H
B3H
B4H
B5H
B6H
B7H
B8H
B9H
BAH
BBH
BCH
BDH
BEH
BFH


C0H
C1H
C2H
C3H
C4H
C5H
C6H
C7H
C8H
C9H
CAH
CBH
CCH
CDH
CEH
CFH
D0H
D1H
D2H
D3H
D4H
D5H
D6H
D7H
D8H
D9H
DAH
DBH
DCH
DDH
DEH
DFH
E0H
E1H
E2H
E3H
E4H
E5H
E6H
E7H
E8H
E9H
EAH
EBH
ECH
EDH
EEH
EFH
SP
LP
EP
AM
PM
CH



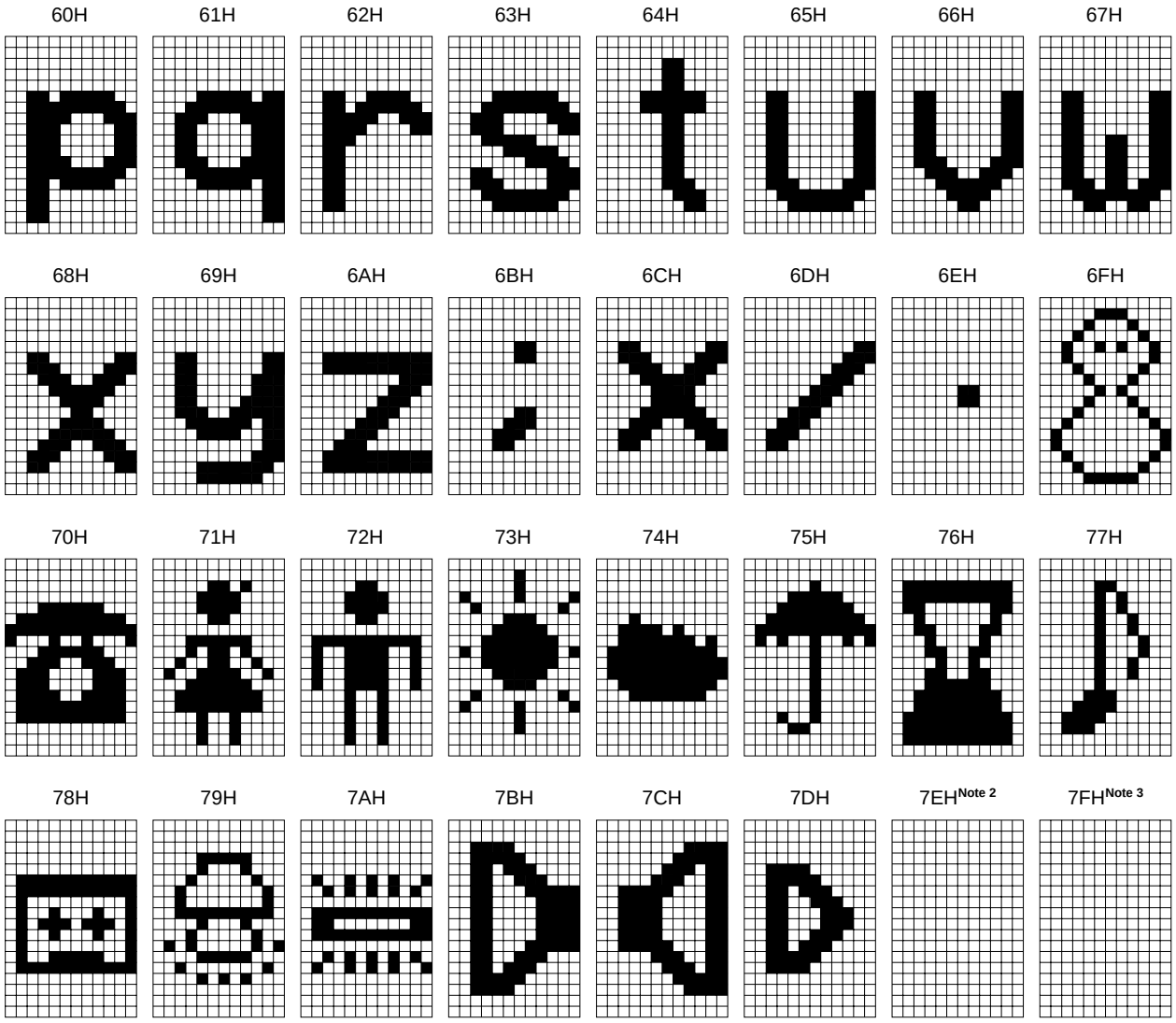
Notes 1. Blank data

2. Display-off data (fixed at this address)

3. End code for second-byte continuous input (fixed at this address)

μPD6462GS-001 Character Patterns


30H
31H
32H
33H
34H
35H
36H
37H
38H
39H
3AH
3BH
3CH
3DH
3EH
3FH
40H
41H
42H
43H
44H
45H
46H
47H
48H
49H
4AH
4BH
4CH
4DH
4EH
4FH
50H
51H
52H
53H
54H
55H
56H
57H
58H
59H
5AH
5BH
5CH
5DH
5EH
5FH



Notes 1. Blank data

2. Display-off data (fixed at this address)

3. End code for second-byte continuous input (fixed at this address)

6. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	μPD6461GS, 6462GS	μPD6461GT	Unit
Supply voltage	V_{DD}	7		V
Input pin voltage	V_{IN}	−0.3 to V_{DD} + 0.3		V
Output pin voltage	V_{OUT}	−0.3 to V_{DD} + 0.3		V
Operating ambient temperature	T_A	−20 to +75		°C
Storage temperature	T_{stg}	−40 to +125		°C
Permissible package power dissipation (T_A = 75 °C)	P_D	180	320	mW
Output current	I_O	±5		mA

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		2.7		5.5	V
Oscillation frequency (LC oscillation)	f_{OSC}	V_{DD} = 2.7 to 5.5 V	6.0		8.0	MHz
Oscillation frequency (external clock)	f_{OSC}	V_{DD} = 2.7 to 5.5 V	4.0		8.0	MHz
Operating temperature	T_A		–20		+75	˚C

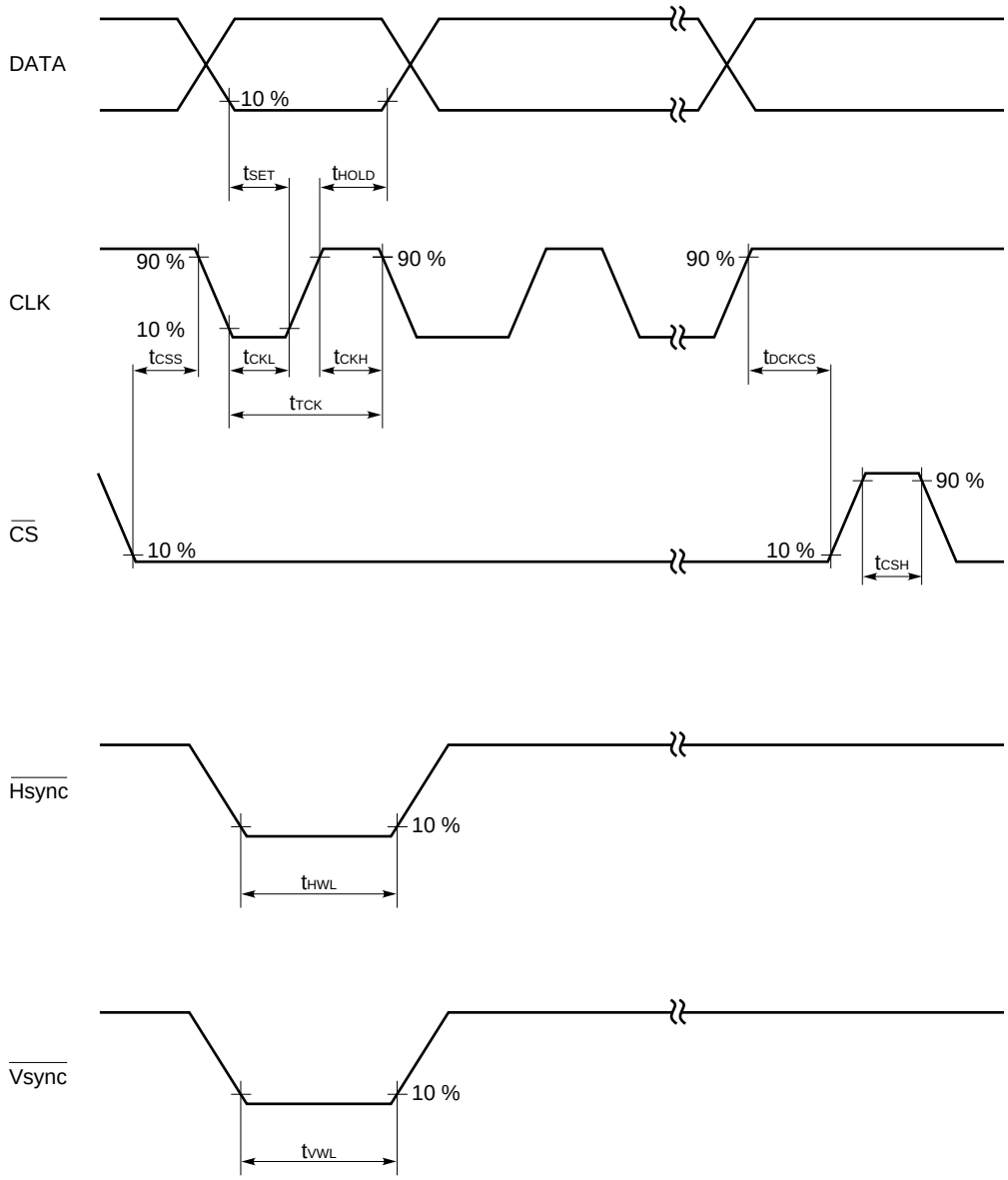
ELECTRICAL CHARACTERISTICS (T_A = −20 to +75 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		2.7	5.0	5.5	V
Supply current 1	I_{DD}	f_{OSC} = 8.0 MHz, V_{DD} = 5.0 V		5.0	10.0	mA
Supply current 2	I_{DD}	f_{OSC} = 8.0 MHz, V_{DD} = 3.0 V		3.0	6.0	mA
Control input high level voltage	V_{CIH}	DATA, CLK, $\overline{CS}$, $\overline{PCL}$	0.7V_{DD}			V
Control input low level voltage	V_{CIL}				0.3V_{DD}	V
Synchronizing signal input high level voltage	V_{ISH}	$\overline{Hsync}$, $\overline{Vsync}$	0.48V_{DD}			V
Synchronizing signal input low level voltage	V_{ISL}				0.16V_{DD}	V
Signal output high level voltage	V_{OSH}	I_{OSL} = −1 mA (V_{DD} = 5 V) / −0.5 mA (V_{DD} = 3 V)	0.9V_{DD}			V
Signal output low level voltage	V_{OSL}	I_{OSL} = 1 mA (V_{DD} = 5 V) / 0.5 mA (V_{DD} = 3 V)			0.1V_{DD}	V
Oscillation output low level voltage	V_{OST}	$\overline{CK_{OUT}}$ I_{OST} = −0.5 mA (V_{DD} = 5 V)			0.1V_{DD}	V

Remark Signal input : DATA, CLK, $\overline{CS}$, $\overline{PCL}$, $\overline{Hsync}$, $\overline{Vsync}$
Signal output: $\overline{CK_{OUT}}$, V_R, V_G, V_B, V_{C1}, V_{C2}, V_{BLK}, BLK1, BLK2 (R_{BLK}, G_{BLK}, B_{BLK})
( ) : Set by a mask option

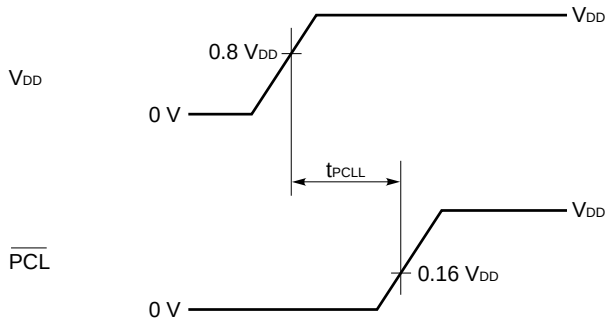
RECOMMENDED OPERATING TIMINGS (T_A = –20 to +75 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Setup time	t_{SET}		200			ns
Hold time	t_{HOLD}		200			ns
Minimum low level width of clock	t_{CKL}		400			ns
Minimum high level width of clock	t_{CKH}		400			ns
Clock cycle	t_{TCK}		1.0			μs
$\overline{CS}$ setup time	t_{CSS}		400			ns
$\overline{CS}$ hold time	t_{CSH}		400			ns
Delay from CLK↑ to $\overline{CS}$↑	t_{DCKCS}		400			ns
Minimum low level width of $\overline{Hsync}$	t_{HWL}		4			μs
Minimum low level width of $\overline{Vsync}$	t_{VWL}		4			μs



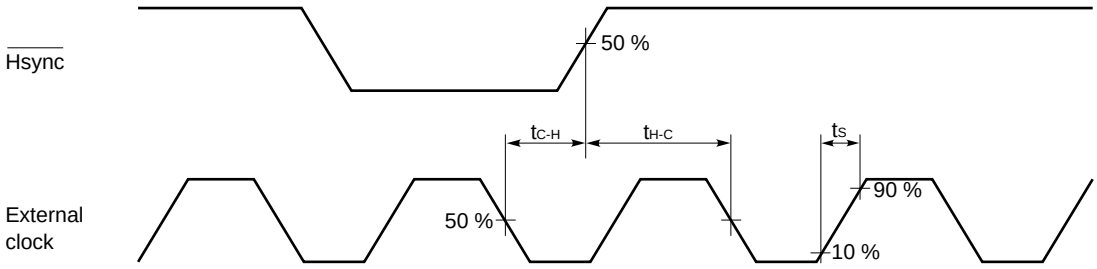
POWER-ON CLEAR SPECIFICATIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{PCL}$ pin low level hold time	t_{PCLL}		10			μs



EXTERNAL CLOCK INPUT

Timing for external clock input (valid when selected with mask option)



Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Time from external clock fall to synchronizing signal rise	t_{C-H}		30			ns
Time from synchronizing signal rise to external clock fall	t_{H-C}		30			ns
t_S (rising slew rate)	t_S				**Note**	ns

Note 10% of the external clock cycle

Example: When the external clock frequency is 8 MHz

Clock cycle = 125 ns

The maximum slew rate is 10% of 125 ns, giving 12.5 ns.

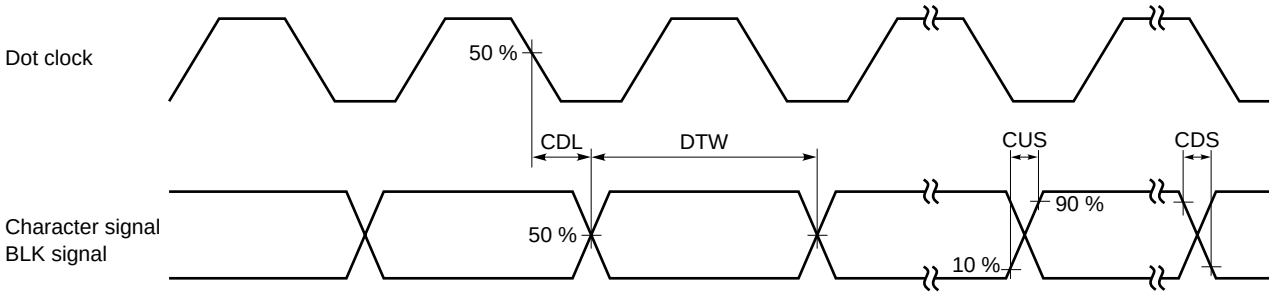
Remarks 1. Keep the external clock in phase with the rising edges of $\overline{Hsync}$.

2. Design the input of $\overline{Hsync}$ so that noise of more than 100 ns is suppressed.

3. When using an external clock, leave the OSC_{OUT} pin open.

CHARACTER AND BLK SIGNAL OUTPUT

Character and BLK signals are output in synchronization with the falling edges of the dot clock.



OUTPUT TIMINGS (T_A = –20 to +75°C, pins: V_R, V_G, V_B, V_{BLK}, V_{C1}, BLK1, V_{C2}, BLK2, (R_{BLK}, G_{BLK}, B_{BLK}))

Pins in parentheses are selected by specifying a mask option.

	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
★	Output delay of character/BLK signal	CDL	V_{DD} = 4.5 to 5.5 V, output load capacity = 10 pF	10	18	30	ns
★	Output delay of character/BLK signal	CDL	V_{DD} = 2.7 to 3.3 V, output load capacity = 10 pF	15	35	80	ns
	Rise time of character/BLK signal	CUS	V_{DD} = 4.5 to 5.5 V, output load capacity = 10 pF	2		10	ns
	Rise time of character/BLK signal	CUS	V_{DD} = 2.7 to 3.3 V, output load capacity = 10 pF	4		25	ns
	Fall time of character/BLK signal	CDS	V_{DD} = 4.5 to 5.5 V, output load capacity = 10 pF	2		10	ns
	Fall time of character/BLK signal	CDS	V_{DD} = 2.7 to 3.3 V, output load capacity = 10 pF	4		25	ns
	Time equivalent to minimum dot	DTW	V_{DD} = 4.5 to 5.5 V, output load capacity = 10 pF	(1 /Oscillation frequency) ±5 Note			ns
	Time equivalent to minimum dot	DTW	V_{DD} = 2.7 to 3.3 V, output load capacity = 10 pF	(1 /Oscillation frequency) ±5 Note			ns

Note Min.: (1/f_{OSC}) – 5 ns, Max.: (1/f_{OSC}) + 5 ns

f_{OSC}: Frequency of LC oscillation or external input clock.

TIMING FOR CONTINUOUS COMMAND INPUT

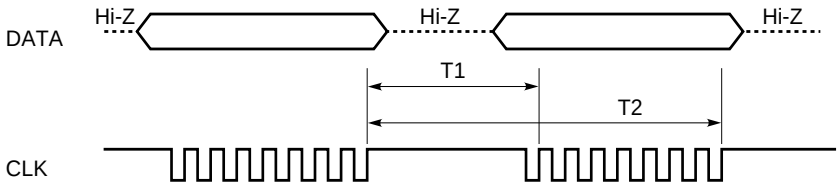
When inputting commands continuously, the following timing requirements must be observed:

(T_A = –20 to +75°C, V_{DD} = 2.7 to 5.5 V)

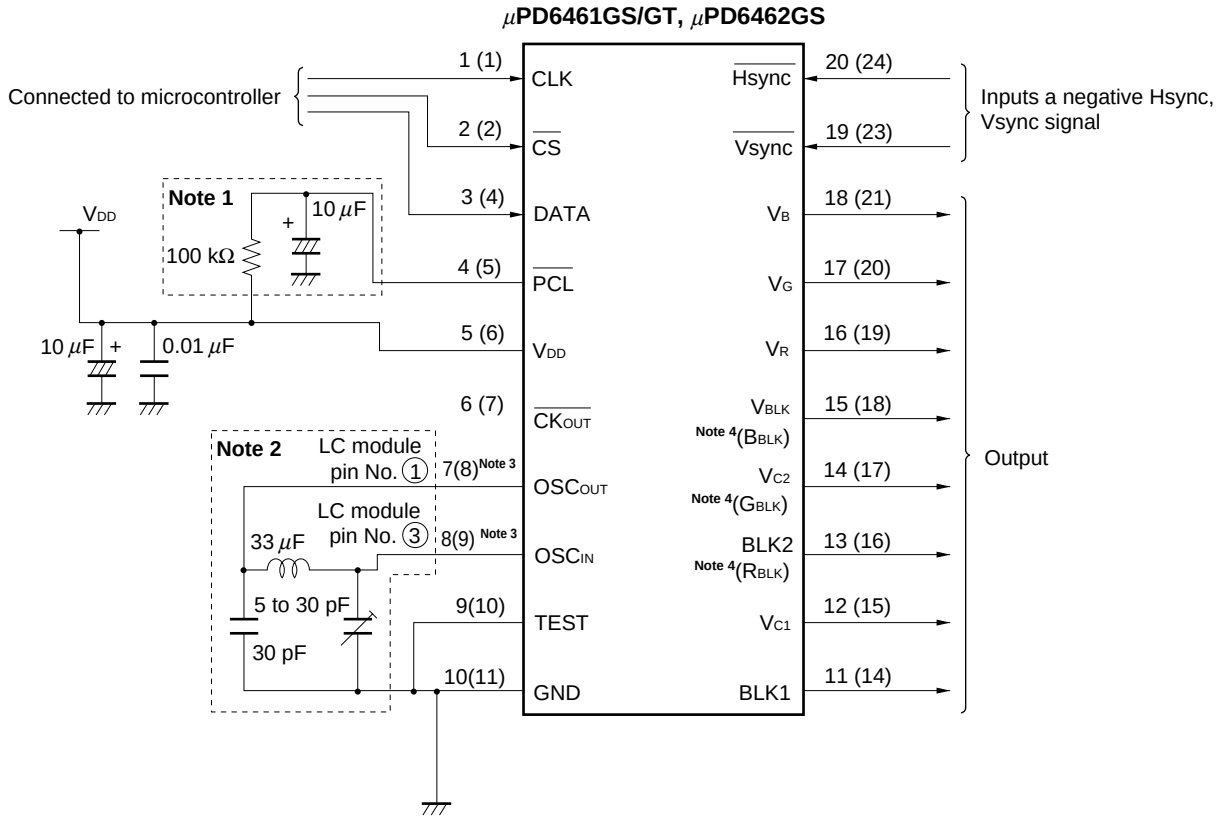
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Continuous command input timing 1	T1	For all commands		2.0			μs
Continuous command input timing 2	T2	For VRAM write commands	When display is turned on	2 μs + (21/f_{OSC}) × S + t_{HWL}			μs
			When display is turned off	2 μs + (12/f_{OSC}) × S			μs

f_{OSC}: Frequency of LC oscillation or external input clock (MHz), S: Character size (single (minimum) or double), t_{HWL}: $\overline{\text{Hsync}}$ width.

Commands other than VRAM write commands may not comply with T2 provided the control clock cycle satisfies the specifications.



7. APPLICATION CIRCUIT EXAMPLE



Notes 1. CR constant must be satisfied with Power-ON Clear Specification (refer to **6. ELECTRICAL CHARACTERISTICS**).

2. This circuit can reduce the number of external components and facilitates the adjustment of oscillation frequency, using LC module (part number: Q285NCIS-11181, manufactured by Toko, Inc.)

3. Connect these pins as follows when inputting external clock:
OSC_{IN} pin: external clock input, OSC_{OUT} pin: open

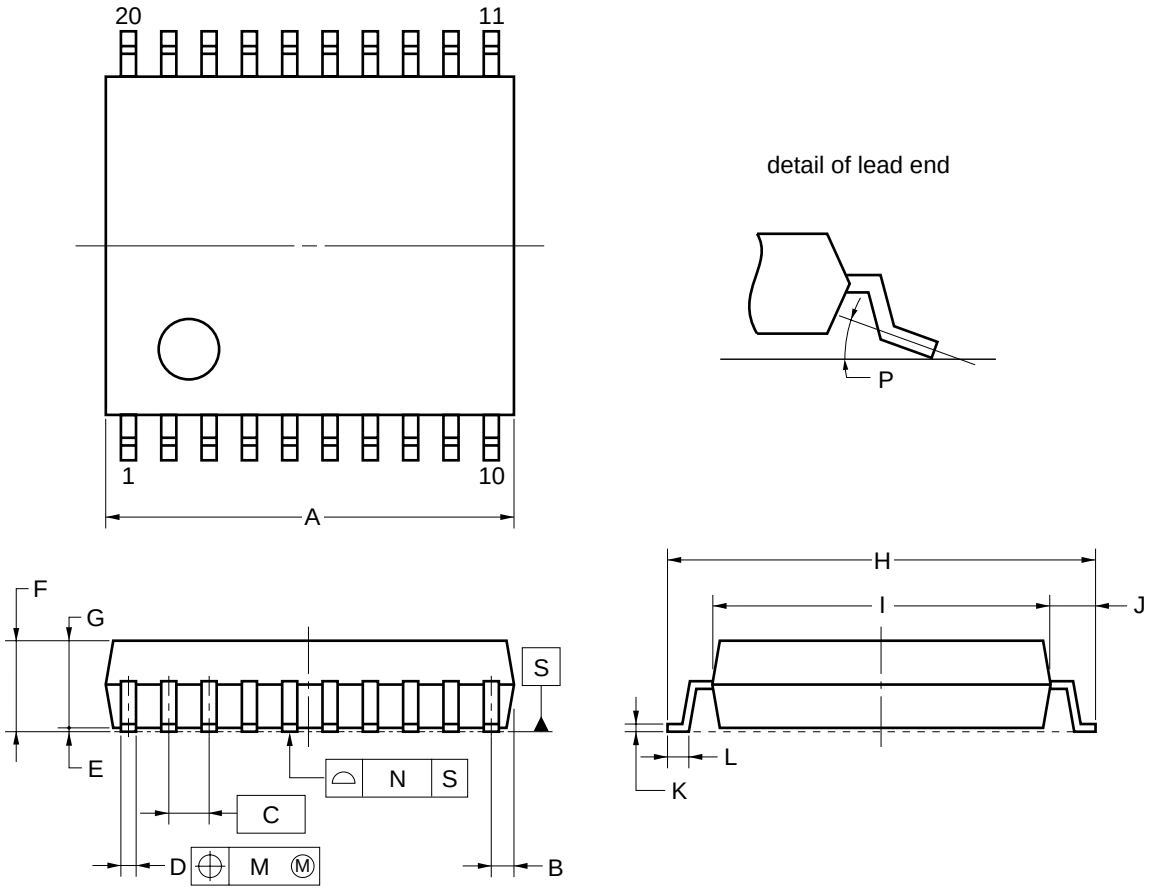
4. Signals in ( ) are set by a mask option (RGB + RGB compatible blanking).

Remarks 1. The number in the parentheses indicates the pin number of the μPD6461GT-xxx.

2. With the μPD6461GT-xxx, influence by noise via lead frame can be surpressed by connecting the N.C. pins (3, 12, 13, 22) to GND.

8. PACKAGE DRAWINGS

20 PIN PLASTIC SHRINK SOP (300 mil)



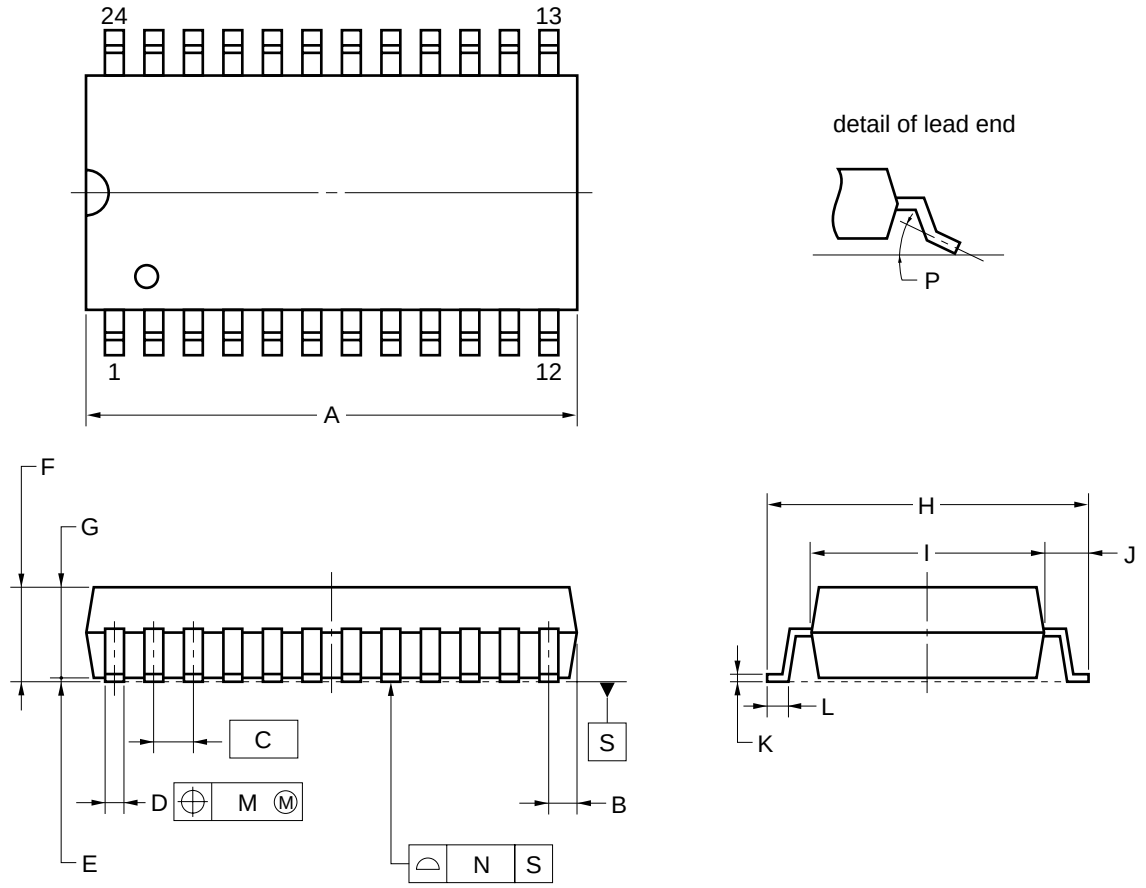
NOTE

1. Controlling dimension—— millimeter.
2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	6.7±0.3	$0.264^{+0.012}_{-0.013}$
B	0.575 MAX.	0.023 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	$0.013^{+0.003}_{-0.004}$
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7±0.1	$0.067^{+0.004}_{-0.005}$
H	8.1±0.3	0.319±0.012
I	6.1±0.2	0.240±0.008
J	1.0±0.2	$0.039^{+0.009}_{-0.008}$
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

P20GM-65-300B-3

24 PIN PLASTIC SOP (375 mil)



NOTE

1. Controlling dimention — millimeter.

2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$15.3^{+0.41}_{-0.2}$	$0.602^{+0.017}_{-0.008}$
B	0.87 MAX.	0.035 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	$0.017^{+0.003}_{-0.004}$
E	0.125±0.075	0.005±0.003
F	2.9 MAX.	0.115 MAX.
G	2.50±0.2	$0.098^{+0.009}_{-0.008}$
H	10.3±0.2	$0.406^{+0.008}_{-0.009}$
I	7.2±0.2	$0.283^{+0.009}_{-0.008}$
J	1.6±0.2	0.063±0.008
K	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P24GT-50-375B-2

9. RECOMMENDED SOLDERING CONDITIONS

When soldering these products, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Surface Mount Devices

μPD6461GS-xxx: 20-pin plastic shrink SOP (300 mil)
μPD6461GT-xxx: 24-pin plastic SOP (375 mil)
μPD6462GS-xxx: 20-pin plastic shrink SOP (300 mil)

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 235 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 2 times.	IR35-00-2
Vapor phase soldering	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 2 times.	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120 °C or below (Package surface temperature).	WS60-00-1
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	–

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

M4 96.5