

November 1988 Revised November 1999

74AC169

4-Stage Synchronous Bidirectional Counter

General Description

The AC169 is fully synchronous 4-stage up/down counter. The AC169 is a modulo-16 binary counter. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

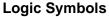
Features

- I_{CC} reduced by 50%
- Synchronous counting and loading
- Built-In lookahead carry capability
- Presettable for programmable operation
- Outputs source/sink 24 mA

Ordering Code:

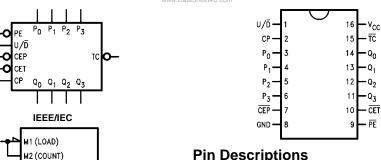
Order Number	Package Number	Package Description
74AC169SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74AC169SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC169MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC169PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.



CET CEP

Connection Diagram



Pin Descriptions

Pin Names	Description				
CEP	Count Enable Parallel Input				
CET	Count Enable Trickle Input				
CP	Clock Pulse Input				
P ₀ -P ₃	Parallel Data Inputs				
PE	Parallel Enable Input				
U/D	Up-Down Count Control Input				
Q ₀ –Q ₃	Flip-Flop Outputs				
TC	Terminal Count Output				

FACT™ is a trademark of Fairchild Semiconductor Corporation.

M3 (UP) 3,5CT = 15 M4 (DOWN) 4,5CT = 0

>2,3,5,6**+**/C7 2,4,5,6-,7D (1) (2)

(4)

(8)

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Q₁

 Q_2

Functional Description

The AC169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When PE is LOW, the data on the P_0 – P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{\text{CEP}}$ and $\overline{\text{CET}}$ must be LOW and $\overline{\text{PE}}$ must be HIGH; the U/D input then determines the direction of counting. The Terminal Count (TC) output is normally HIGH and goes LOW, provided that CET is LOW, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The TC output state is not a function of the Count Enable Parallel (CEP) input level. If an illegal state occurs, the AC169 will return to the legitimate sequence within two counts. Since the TC signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on \overline{TC} . For this reason the use of \overline{TC} as a clock signal is not recommended (see logic equations

- 1. Count Enable = CEP •CET PE
- 2. Up: $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 Q_3 \cdot (Up) \cdot \overline{CET}$
- 3. Down: $\overline{TC} = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (Down) \cdot \overline{CET}$

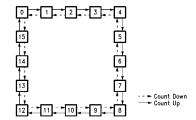
Mode Select Table

PE	CEP	CET	U/D	Action on Rising
PE	CEP	CEI	טוט	Clock Edge
L	Х	Х	Χ	Load (P _n to Q _n)
Н	L	L	Н	Count Up (Increment)
Н	L	L	L	Count Down (Decrement)
Н	Н	Х	Χ	No Change (Hold)
Н	Χ	Н	Χ	No Change (Hold)

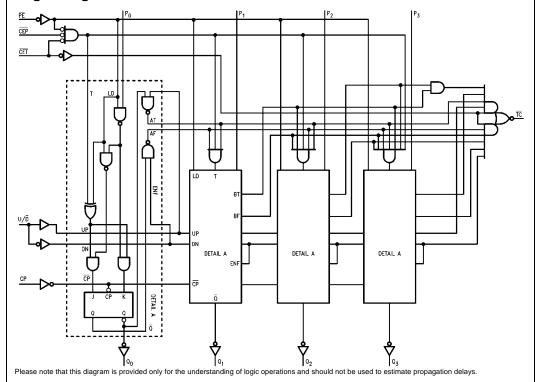
H = HIGH Voltage Level

- L = LOW Voltage Level
- X = Immaterial

State Diagram



Logic Diagram



Absolute Maximum Ratings(Note 1)

-0.5V to +7.0V

DC Input Diode Current (I_{IK})

Supply Voltage (V_{CC})

 $V_1 = -0.5V$ -20 mA $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) -0.5V to $V_{CC} + 0.5V$

DC Output Diode Current (I_{OK})

 $V_{O} = -0.5V$ -20 mA

 $V_O = V_{CC} + 0.5 V$ +20 mA $-0.5\mbox{V}$ to $\mbox{V}_{CC} + 0.5\mbox{V}$

DC Output Voltage (V_O) DC Output Source

or Sink Current (I_O) $\pm 50~\text{mA}$

DC V_{CC} or Ground Current

per Output Pin (I_{CC} or I_{GND}) ±50 mA

-65°C to +150°C Storage Temperature (T_{STG})

Junction Temperature (T_J)

140°C PDIP

Recommended Operating Conditions

Supply Voltage (V_{CC}) 2.0V to 6.0V

0V to V_{CC} Input Voltage (V_I) Output Voltage (V_O) 0V to V_{CC} Operating Temperature (T_A) -40°C to +85°C

Minimum Input Edge Rate $(\Delta V/\Delta t)$

 $V_{\mbox{\footnotesize{IN}}}$ from 30% to 70% of $V_{\mbox{\footnotesize{CC}}}$

V_{CC} @ 3.3V, 4.5V, 5.5V 125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions
Cymbol		(V)	Тур	Guaranteed Limits			Contantions
V _{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1		V _{OUT} = 0.1V
	Input Voltage	4.5	2.25	3.15	3.15	V	or V _{CC} – 0.1V
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9		V _{OUT} = 0.1V
	Input Voltage	4.5	2.25	1.35	1.35	V	or V _{CC} – 0.1V
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9		
	Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		3.0		2.56	2.46		$I_{OH} = -12 \text{ mA}$
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$
		5.5		4.86	4.76		I _{OH} = -24 mA (Note 2)
V _{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1		
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or V_{IH}
		3.0		0.36	0.44		$I_{OL} = 12 \text{ mA}$
		4.5		0.36	0.44	V	$I_{OL} = 24 \text{ mA}$
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 2)
I _{IN}	Maximum Input	5.5		10.4	14.0		V V OND
(Note 4)	Leakage Current	5.5		±0.1	±1.0	μА	$V_I = V_{CC}$, GND
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 3)	5.5			-75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent	5.5		4.0	40.0		$V_{IN} = V_{CC}$
(Note 4)	Supply Current	5.5		4.0	40.0	μΑ	or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

AC Electrical Characteristics

		V_{CC} (V) $T_{A} = +25^{\circ}C, C_{L} = 50 pF$			$T_A = -40^{\circ}C$ to +			
Symbol	Parameter	(Note 5)	Min	Тур	Max	Min	Max	Units
f _{MAX}	Maximum Clock	3.3	75	118		65		MHz
	Frequency	5.0	100	154		90		IVITIZ
t _{PLH}	Propagation Delay	3.3	2.5	9.5	13.0	2.0	14.5	ns
	CP to Q_n (PE HIGH or LOW)	5.0	1.5	7.0	10.0	1.5	11.0	ns
t _{PHL}	Propagation Delay	3.3	2.5	10.5	14.5	2.0	16.0	ns
	CP to Q_n (PE HIGH or LOW)	5.0	1.5	7.5	11.0	1.5	12.0	115
t _{PLH}	Propagation Delay	3.3	4.5	13.5	18.0	3.5	22.0	
	CP to TC	5.0	3.0	9.5	13.0	2.0	14.0	ns
t _{PHL}	Propagation Delay	3.3	3.5	13.5	18.0	3.0	20.5	no
	CP to TC	5.0	2.5	9.5	13.0	2.0	14.5	ns
t _{PLH}	Propagation Delay	3.3	3.5	11.0	15.0	3.0	16.5	ns
	CET to TC	5.0	3.0	8.0	10.5	2.5	12.0	115
t _{PHL}	Propagation Delay	3.3	3.0	9.5	12.5	2.5	14.5	no
	CET to TC	5.0	2.0	7.0	9.0	1.5	10.0	ns
t _{PLH}	Propagation Delay	3.3	3.5	11.0	15.0	3.0	17.0	no
	U/D to TC	5.0	2.5	8.0	10.5	2.0	12.0	ns
t _{PHL}	Propagation Delay	3.3	2.5	10.0	13.5	2.0	15.5	ns
	U/D to TC	5.0	1.5	7.0	9.5	1.5	10.5	115

Note 5: Voltage Range 3.3 is $3.3V \pm 0.3V$ Voltage Range 5.0 is $5.0V \pm 0.5V$

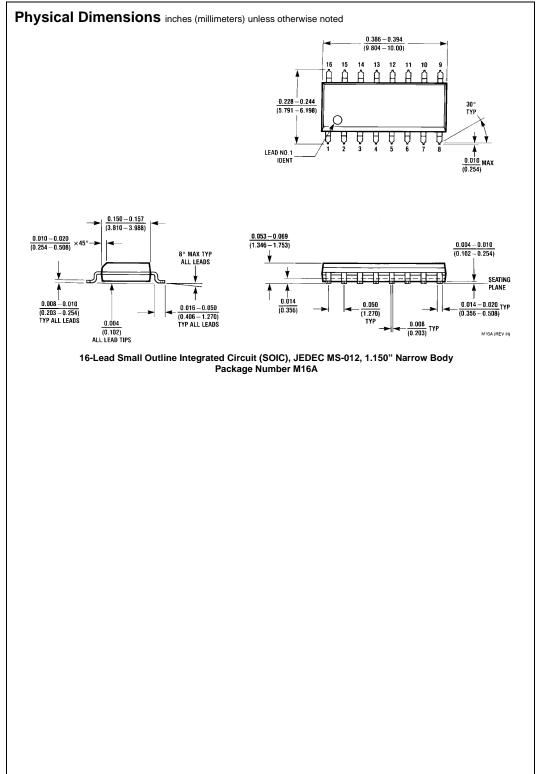
AC Operating Requirements

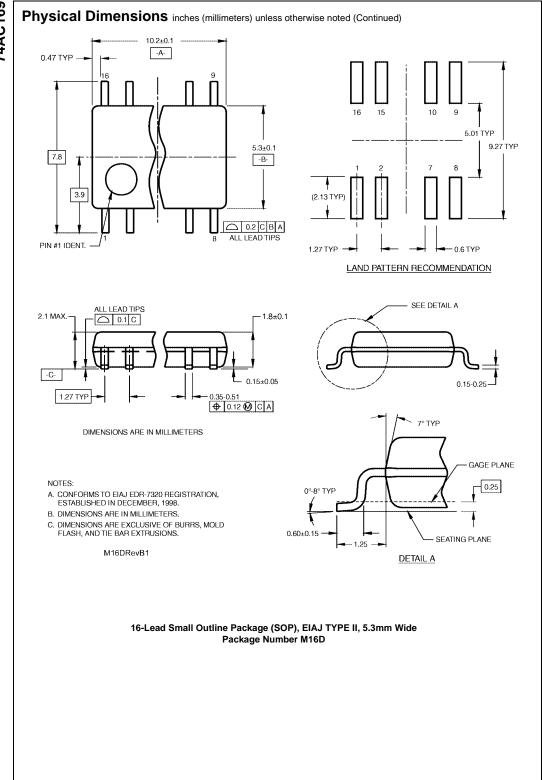
Parameter	(Note 6)					
0 · T 111011 1011/	(Тур	(Guaranteed Minimum	Units	
Setup Time, HIGH or LOW	3.3	3.0	4.5	5.0	ns	
P _n to CP	5.0	1.5	2.5	2.5	115	
Hold Time, HIGH or LOW	3.3	-1.5	0.5	0.5		
P _n to CP	5.0	-0.5	1.5	1.5	ns	
Setup Time, HIGH or LOW	3.3	7.5	10.5	12.5		
CEP to CP	5.0	4.5	7.0	8.0	ns	
Hold Time, HIGH or LOW	3.3	-4.5	0	0	ns	
CEP to CP	5.0	-2.0	0.5	1.0	115	
Setup Time, HIGH or LOW	3.3	7.0	10.0	12.0		
CET to CP	5.0	4.0	6.5	8.0	ns	
Hold Time, HIGH or LOW	3.3	-6.0	0	0		
CET to CP	5.0	-4.0	0.5	1.0	ns	
Setup Time, HIGH or LOW	3.3	3.5	5.5	6.5	ns	
PE to CP	5.0	2.0	3.5	4.0	ns	
Hold Time, HIGH or LOW	3.3	-3.5	0	0		
PE to CP	5.0	-1.5	0.5	0.5	ns	
Setup Time, HIGH or LOW	3.3	7.0	10.0	11.5		
U/D to CP	5.0	4.5	6.5	7.5	ns	
Hold Time, HIGH or LOW	3.3	-7.0	0	0	no	
U/D to CP	5.0	-4.0	0.5	0.5	ns	
CP Pulse Width,	3.3	2.0	3.0	4.0	no	
HIGH or LOW	5.0	2.0	3.0	3.0	ns	
	P _n to CP Hold Time, HIGH or LOW P _n to CP Setup Time, HIGH or LOW CEP to CP Hold Time, HIGH or LOW CEP to CP Setup Time, HIGH or LOW CET to CP Setup Time, HIGH or LOW CET to CP Hold Time, HIGH or LOW CET to CP Setup Time, HIGH or LOW PE to CP Setup Time, HIGH or LOW PE to CP Hold Time, HIGH or LOW PE to CP Setup Time, HIGH or LOW PE to CP Setup Time, HIGH or LOW U/O to CP Hold Time, HIGH or LOW U/O to CP CP Pulse Width,	Pn to CP 5.0 Hold Time, HIGH or LOW 3.3 Pn to CP 5.0 Setup Time, HIGH or LOW 3.3 CEP to CP 5.0 Hold Time, HIGH or LOW 3.3 CET to CP 5.0 Setup Time, HIGH or LOW 3.3 CET to CP 5.0 Hold Time, HIGH or LOW 3.3 PE to CP 5.0 Hold Time, HIGH or LOW 3.3 PE to CP 5.0 Setup Time, HIGH or LOW 3.3 PE to CP 5.0 Setup Time, HIGH or LOW 3.3 U/D to CP 5.0 Hold Time, HIGH or LOW 3.3 U/D to CP 5.0 CP Pulse Width, 3.3	Pn to CP 5.0 1.5 Hold Time, HIGH or LOW 3.3 −1.5 Pn to CP 5.0 −0.5 Setup Time, HIGH or LOW 3.3 7.5 CEP to CP 5.0 4.5 Hold Time, HIGH or LOW 3.3 −4.5 CEP to CP 5.0 −2.0 Setup Time, HIGH or LOW 3.3 7.0 CET to CP 5.0 4.0 Hold Time, HIGH or LOW 3.3 −6.0 CET to CP 5.0 −4.0 Setup Time, HIGH or LOW 3.3 3.5 PE to CP 5.0 −1.5 Setup Time, HIGH or LOW 3.3 7.0 U/D to CP 5.0 4.5 Hold Time, HIGH or LOW 3.3 7.0 U/D to CP 5.0 4.5 Hold Time, HIGH or LOW 3.3 −7.0 U/D to CP 5.0 −4.0 CP Pulse Width, 3.3 2.0	Pn to CP 5.0 1.5 2.5 Hold Time, HIGH or LOW 3.3 −1.5 0.5 Pn to CP 5.0 −0.5 1.5 Setup Time, HIGH or LOW 3.3 7.5 10.5 CEP to CP 5.0 4.5 7.0 Hold Time, HIGH or LOW 3.3 −4.5 0 CEP to CP 5.0 −2.0 0.5 Setup Time, HIGH or LOW 3.3 7.0 10.0 CET to CP 5.0 4.0 6.5 Hold Time, HIGH or LOW 3.3 −6.0 0 CET to CP 5.0 −4.0 0.5 Setup Time, HIGH or LOW 3.3 3.5 5.5 PE to CP 5.0 2.0 3.5 Hold Time, HIGH or LOW 3.3 7.0 10.0 U/D to CP 5.0 4.5 6.5 Hold Time, HIGH or LOW 3.3 7.0 10.0 U/D to CP 5.0 4.5 6.5 Hold Time, HIGH or LOW 3.3 <t< td=""><td>Pn to CP 5.0 1.5 2.5 2.5 Hold Time, HIGH or LOW 3.3 −1.5 0.5 0.5 Pn to CP 5.0 −0.5 1.5 1.5 Setup Time, HIGH or LOW 3.3 7.5 10.5 12.5 CEP to CP 5.0 4.5 7.0 8.0 Hold Time, HIGH or LOW 3.3 −4.5 0 0 CEP to CP 5.0 −2.0 0.5 1.0 Setup Time, HIGH or LOW 3.3 7.0 10.0 12.0 CET to CP 5.0 4.0 6.5 8.0 Hold Time, HIGH or LOW 3.3 −6.0 0 0 0 CET to CP 5.0 −4.0 0.5 1.0 1.0 Setup Time, HIGH or LOW 3.3 3.5 5.5 6.5 6.5 PE to CP 5.0 −1.5 0.5 0.5 0.5 Setup Time, HIGH or LOW 3.3 7.0 10.0 11.5 11.5 U/D to CP 5.0 4.5 6.5 7.5 Hold Time, HIGH or LOW<</td></t<>	Pn to CP 5.0 1.5 2.5 2.5 Hold Time, HIGH or LOW 3.3 −1.5 0.5 0.5 Pn to CP 5.0 −0.5 1.5 1.5 Setup Time, HIGH or LOW 3.3 7.5 10.5 12.5 CEP to CP 5.0 4.5 7.0 8.0 Hold Time, HIGH or LOW 3.3 −4.5 0 0 CEP to CP 5.0 −2.0 0.5 1.0 Setup Time, HIGH or LOW 3.3 7.0 10.0 12.0 CET to CP 5.0 4.0 6.5 8.0 Hold Time, HIGH or LOW 3.3 −6.0 0 0 0 CET to CP 5.0 −4.0 0.5 1.0 1.0 Setup Time, HIGH or LOW 3.3 3.5 5.5 6.5 6.5 PE to CP 5.0 −1.5 0.5 0.5 0.5 Setup Time, HIGH or LOW 3.3 7.0 10.0 11.5 11.5 U/D to CP 5.0 4.5 6.5 7.5 Hold Time, HIGH or LOW<	

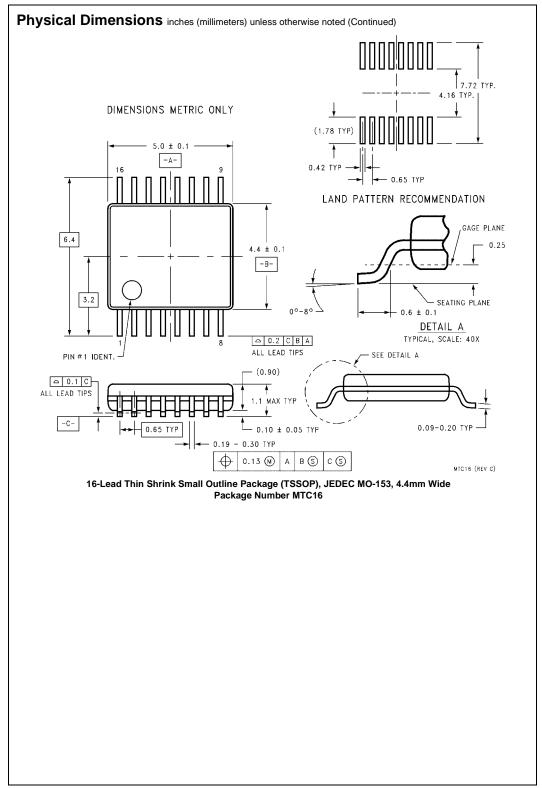
Note 6: Voltage Range 3.3 is $3.3 \text{V} \pm 0.3 \text{V}$ Voltage Range 5.0 is $5.0 \text{V} \pm 0.5 \text{V}$

Capacitance

Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.0V$







Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.780 0.090 (18.80 - 19.81)(2.286)<u>16 15 14 13 12 11 10 9</u> 16 15 INDEX AREA 0.250 ± 0.010 $\overline{(6.350 \pm 0.254)}$ PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 8 1 2 OPTION 01 OPTION 02 0.065 $\frac{0.130 \pm 0.005}{(3.302 \pm 0.127)}$ $\frac{0.060}{(1.524)}$ TYP (1.651)4° TYP 0.300 - 0.320OPTIONAL (7.620 - 8.128) 0.145 - 0.200 (3.683 - 5.080)95°±5° $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 90° ± 4° TYP 0.020 $\frac{0.280}{(7.112)}$ MIN (0.508)0.125 - 0.150 (3.175 - 3.810) 0.030 ± 0.015 (0.762 ± 0.381) 0.014 - 0.023 0.100 ± 0.010 (0.325 **+**0.040 **-**0.015 (0.356 - 0.584) (2.540 ± 0.254) 0.050 ± 0.010 N16E (REV F) TYP (1.270 ± 0.254)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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