FAIRCHILD SEMICONDUCTOR™

November 1988
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# 74AC169
# 4-Stage Synchronous Bidirectional Counter

## General Description

The AC169 is fully synchronous 4-stage up/down counter. The AC169 is a modulo-16 binary counter. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

## Features

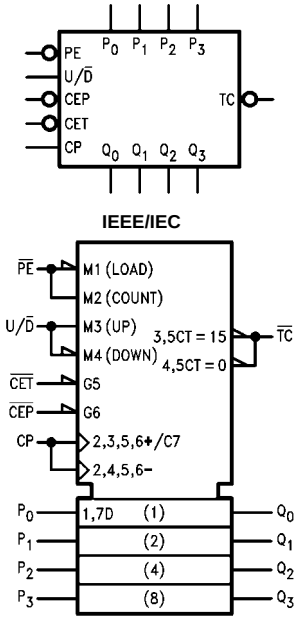
- $I_{CC}$ reduced by 50%
- Synchronous counting and loading
- Built-In lookahead carry capability
- Presettable for programmable operation
- Outputs source/sink 24 mA

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74AC169SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |
| 74AC169SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC169MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC169PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

## Logic Symbols

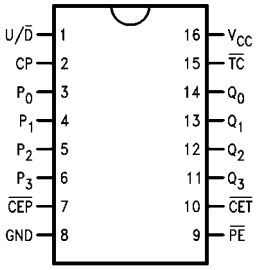



IEEE/IEC




## Connection Diagram






## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{CEP}$ | Count Enable Parallel Input |
| $\overline{CET}$ | Count Enable Trickle Input |
| CP | Clock Pulse Input |
| $P_0$–$P_3$ | Parallel Data Inputs |
| $\overline{PE}$ | Parallel Enable Input |
| U/$\overline{D}$ | Up-Down Count Control Input |
| $Q_0$–$Q_3$ | Flip-Flop Outputs |
| $\overline{TC}$ | Terminal Count Output |

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## Functional Description

The AC169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the $P_0$–$P_3$ inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. If an illegal state occurs, the AC169 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

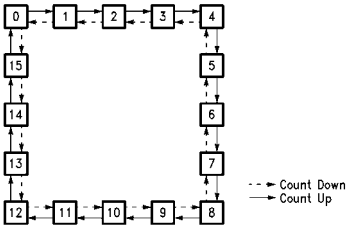
1. Count Enable = $\overline{CEP}$ •$\overline{CET}$ • $\overline{PE}$
2. Up: $\overline{TC}$ = $Q_0$•$Q_1$•$Q_2$$Q_3$•(Up)•$\overline{CET}$
3. Down: $\overline{TC}$ = $\overline{Q}_0$• $\overline{Q}_1$•$\overline{Q}_2$•$\overline{Q}_3$ •(Down)•$\overline{CET}$

## Mode Select Table

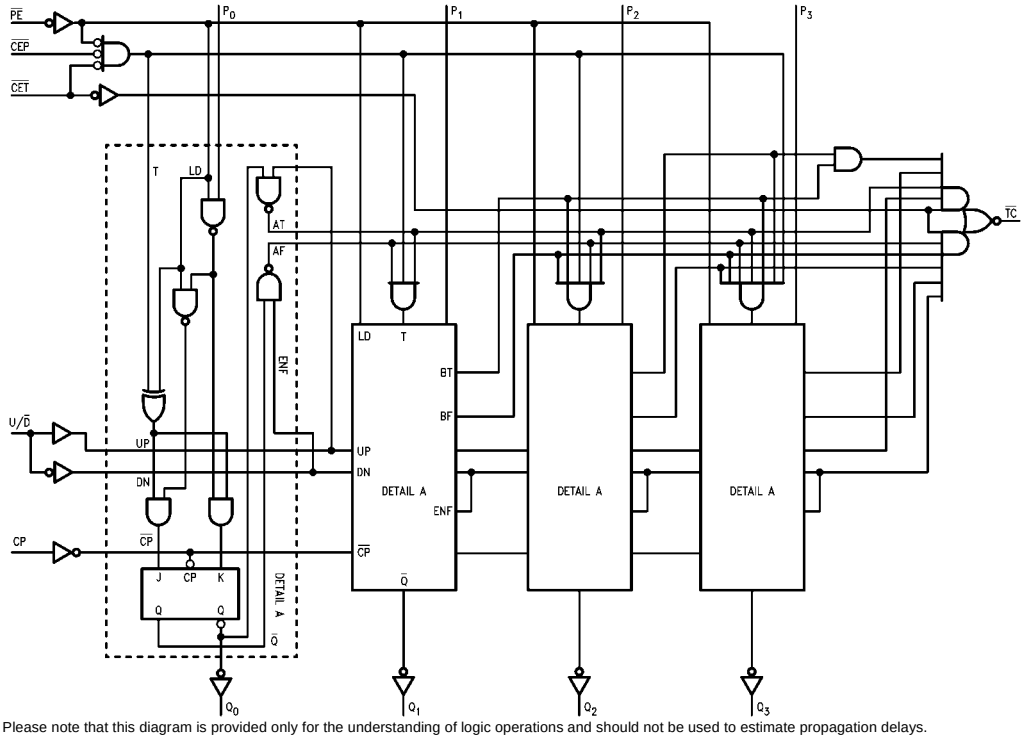
| $\overline{PE}$ | $\overline{CEP}$ | $\overline{CET}$ | U/$\overline{D}$ | Action on Rising Clock Edge |
|---|---|---|---|---|
| L | X | X | X | Load ($P_n$ to $Q_n$) |
| H | L | L | H | Count Up (Increment) |
| H | L | L | L | Count Down (Decrement) |
| H | H | X | X | No Change (Hold) |
| H | X | H | X | No Change (Hold) |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

## State Diagram




## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | –0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = –0.5V | –20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | –0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = –0.5V | –20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | –0.5V to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | –65°C to +150°C |
| Junction Temperature ($T_J$) | |
| PDIP | 140°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 2.0V to 6.0V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | –40°C to +85°C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| $V_{IN}$ from 30% to 70% of $V_{CC}$ | |
| $V_{CC}$ @ 3.3V, 4.5V, 5.5V | 125 mV/ns |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C | $T_A$ = –40°C to +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 3.0 | 1.5 | 2.1 | 2.1 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ – 0.1V |
| | | 4.5 | 2.25 | 3.15 | 3.15 | | |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 3.0 | 1.5 | 0.9 | 0.9 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ – 0.1V |
| | | 4.5 | 2.25 | 1.35 | 1.35 | | |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | V | $I_{OUT}$ = –50 µA |
| | | 4.5 | 4.49 | 4.4 | 4.4 | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 2.56 | 2.46 | V | $I_{OH}$ = –12 mA |
| | | 4.5 | | 3.86 | 3.76 | | $I_{OH}$ = –24 mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH}$ = –24 mA (Note 2) |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 µA |
| | | 4.5 | 0.001 | 0.1 | 0.1 | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 0.36 | 0.44 | V | $I_{OL}$ = 12 mA |
| | | 4.5 | | 0.36 | 0.44 | | $I_{OL}$ = 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL}$ = 24 mA (Note 2) |
| $I_{IN}$ (Note 4) | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | µA | $V_I$ = $V_{CC}$, GND |
| $I_{OLD}$ | Minimum Dynamic Output Current (Note 3) | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | | 5.5 | | | –75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ (Note 4) | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | µA | $V_{IN}$ = $V_{CC}$ or GND |

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** $I_{IN}$ and $I_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{CC}$.

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) (Note 5) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | 3.3 | 75 | 118 | | 65 | | MHz |
| | | 5.0 | 100 | 154 | | 90 | | |
| $t_{PLH}$ | Propagation Delay CP to $Q_n$ ($\overline{PE}$ HIGH or LOW) | 3.3 | 2.5 | 9.5 | 13.0 | 2.0 | 14.5 | ns |
| | | 5.0 | 1.5 | 7.0 | 10.0 | 1.5 | 11.0 | |
| $t_{PHL}$ | Propagation Delay CP to $Q_n$ ($\overline{PE}$ HIGH or LOW) | 3.3 | 2.5 | 10.5 | 14.5 | 2.0 | 16.0 | ns |
| | | 5.0 | 1.5 | 7.5 | 11.0 | 1.5 | 12.0 | |
| $t_{PLH}$ | Propagation Delay CP to $\overline{TC}$ | 3.3 | 4.5 | 13.5 | 18.0 | 3.5 | 22.0 | ns |
| | | 5.0 | 3.0 | 9.5 | 13.0 | 2.0 | 14.0 | |
| $t_{PHL}$ | Propagation Delay CP to $\overline{TC}$ | 3.3 | 3.5 | 13.5 | 18.0 | 3.0 | 20.5 | ns |
| | | 5.0 | 2.5 | 9.5 | 13.0 | 2.0 | 14.5 | |
| $t_{PLH}$ | Propagation Delay $\overline{CET}$ to $\overline{TC}$ | 3.3 | 3.5 | 11.0 | 15.0 | 3.0 | 16.5 | ns |
| | | 5.0 | 3.0 | 8.0 | 10.5 | 2.5 | 12.0 | |
| $t_{PHL}$ | Propagation Delay $\overline{CET}$ to $\overline{TC}$ | 3.3 | 3.0 | 9.5 | 12.5 | 2.5 | 14.5 | ns |
| | | 5.0 | 2.0 | 7.0 | 9.0 | 1.5 | 10.0 | |
| $t_{PLH}$ | Propagation Delay U/$\overline{D}$ to $\overline{TC}$ | 3.3 | 3.5 | 11.0 | 15.0 | 3.0 | 17.0 | ns |
| | | 5.0 | 2.5 | 8.0 | 10.5 | 2.0 | 12.0 | |
| $t_{PHL}$ | Propagation Delay U/$\overline{D}$ to $\overline{TC}$ | 3.3 | 2.5 | 10.0 | 13.5 | 2.0 | 15.5 | ns |
| | | 5.0 | 1.5 | 7.0 | 9.5 | 1.5 | 10.5 | |

**Note 5:** Voltage Range 3.3 is 3.3V ± 0.3V  Voltage Range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements

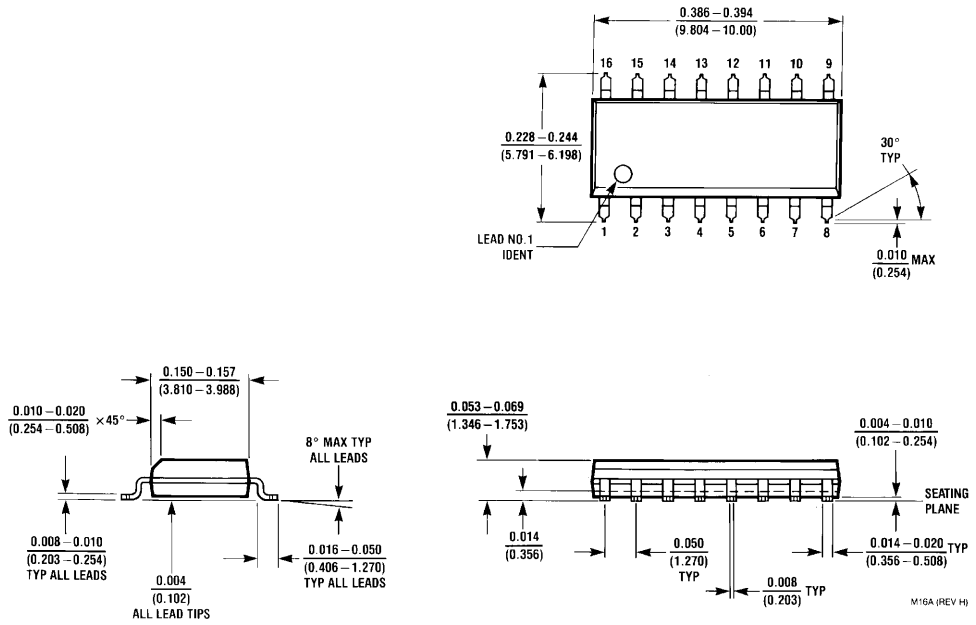
| Symbol | Parameter | $V_{CC}$ (V) (Note 6) | $T_A = +25°C$, $C_L = 50$ pF | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_S$ | Setup Time, HIGH or LOW $P_n$ to CP | 3.3 | 3.0 | 4.5 | 5.0 | ns |
| | | 5.0 | 1.5 | 2.5 | 2.5 | |
| $t_H$ | Hold Time, HIGH or LOW $P_n$ to CP | 3.3 | –1.5 | 0.5 | 0.5 | ns |
| | | 5.0 | –0.5 | 1.5 | 1.5 | |
| $t_S$ | Setup Time, HIGH or LOW $\overline{CEP}$ to CP | 3.3 | 7.5 | 10.5 | 12.5 | ns |
| | | 5.0 | 4.5 | 7.0 | 8.0 | |
| $t_H$ | Hold Time, HIGH or LOW $\overline{CEP}$ to CP | 3.3 | –4.5 | 0 | 0 | ns |
| | | 5.0 | –2.0 | 0.5 | 1.0 | |
| $t_S$ | Setup Time, HIGH or LOW $\overline{CET}$ to CP | 3.3 | 7.0 | 10.0 | 12.0 | ns |
| | | 5.0 | 4.0 | 6.5 | 8.0 | |
| $t_H$ | Hold Time, HIGH or LOW $\overline{CET}$ to CP | 3.3 | –6.0 | 0 | 0 | ns |
| | | 5.0 | –4.0 | 0.5 | 1.0 | |
| $t_S$ | Setup Time, HIGH or LOW $\overline{PE}$ to CP | 3.3 | 3.5 | 5.5 | 6.5 | ns |
| | | 5.0 | 2.0 | 3.5 | 4.0 | |
| $t_H$ | Hold Time, HIGH or LOW $\overline{PE}$ to CP | 3.3 | –3.5 | 0 | 0 | ns |
| | | 5.0 | –1.5 | 0.5 | 0.5 | |
| $t_S$ | Setup Time, HIGH or LOW U/$\overline{D}$ to CP | 3.3 | 7.0 | 10.0 | 11.5 | ns |
| | | 5.0 | 4.5 | 6.5 | 7.5 | |
| $t_H$ | Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$ | 3.3 | –7.0 | 0 | 0 | ns |
| | | 5.0 | –4.0 | 0.5 | 0.5 | |
| $t_W$ | CP Pulse Width, HIGH or LOW | 3.3 | 2.0 | 3.0 | 4.0 | ns |
| | | 5.0 | 2.0 | 3.0 | 3.0 | |

**Note 6:** Voltage Range 3.3 is 3.3V ± 0.3V  Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

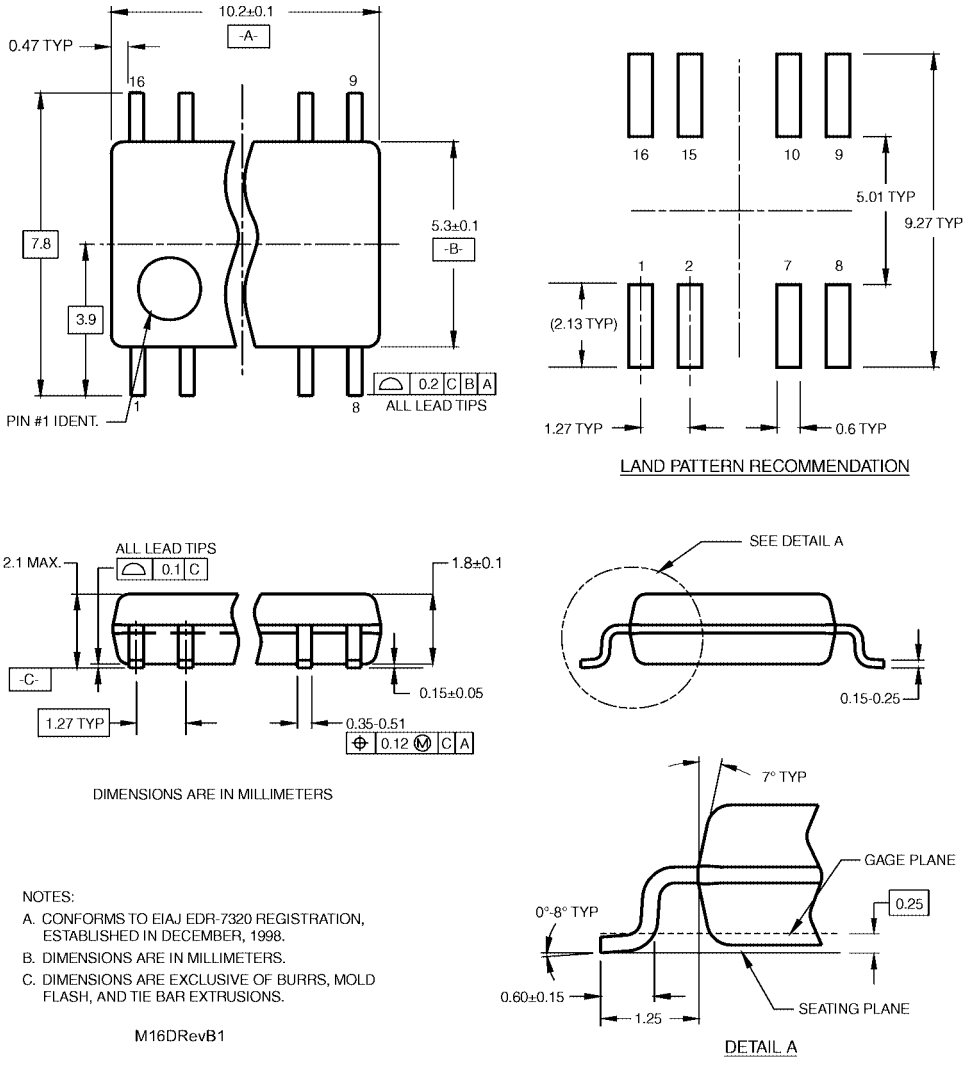
| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 60.0 | pF | $V_{CC}$ = 5.0V |

## Physical Dimensions inches (millimeters) unless otherwise noted




**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 1.150" Narrow Body**
**Package Number M16A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

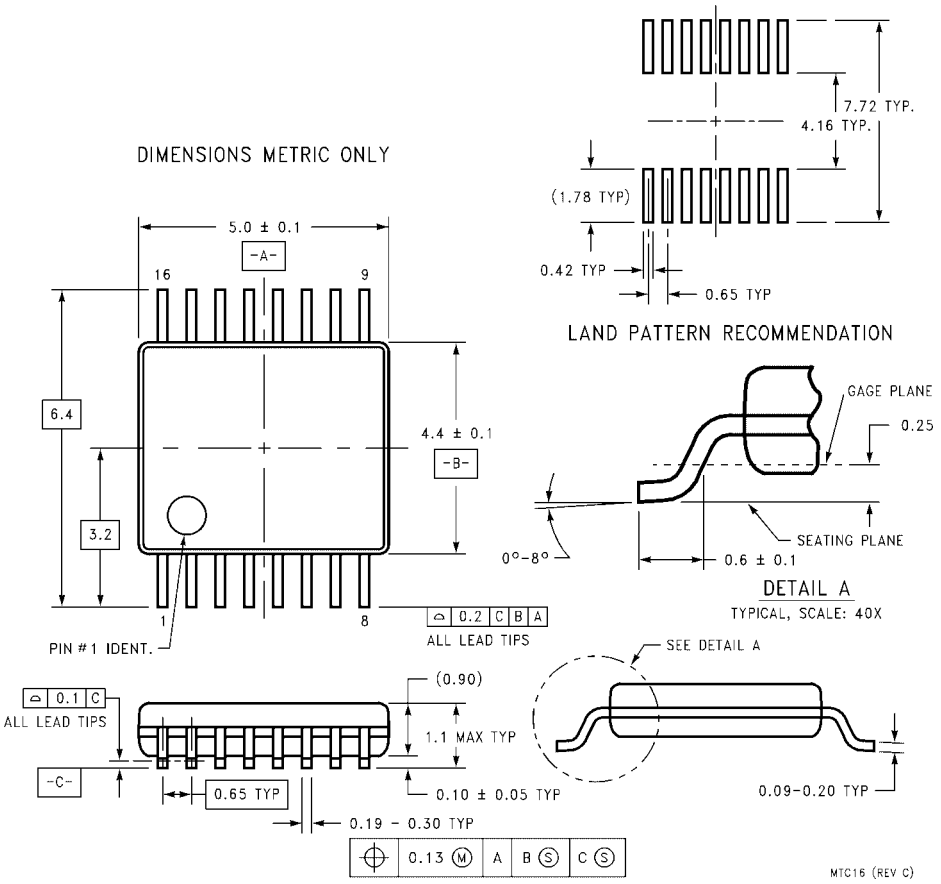
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

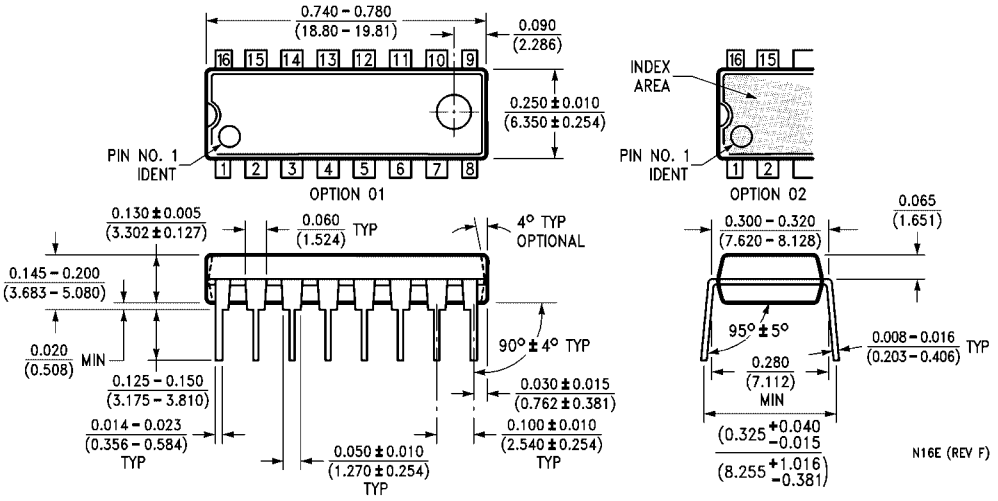
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M16D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**