

# DATA SHEET

## **74ABT273A** Octal D-type flip-flop

Product specification

1995 Sep 06

IC23 Data Handbook

## Octal D-type flip-flop

## 74ABT273A

## FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- Power-up reset
- See 74ABT377 for clock enable version
- See 74ABT373 for transparent latch version
- See 74ABT374 for 3-State version
- ESD protection exceeds 2000 V per Mil Std 833 Method 3015 and 200 V per machine model.

## DESCRIPTION

The 74ABT273A has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ( $\overline{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the  $\overline{MR}$  input. The device is useful for applications where the true output only is required and the CP and  $\overline{MR}$  are common elements.

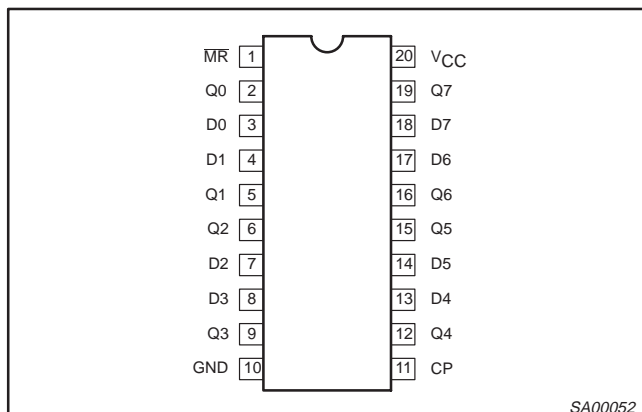
## QUICK REFERENCE DATA

| SYMBOL                 | PARAMETER                     | CONDITIONS<br>$T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$ | TYPICAL    | UNIT          |
|------------------------|-------------------------------|--|------------|---------------|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to Qn | $C_L = 50\text{pF}; V_{CC} = 5\text{V}$                              | 3.0<br>3.4 | ns            |
| $C_{IN}$               | Input capacitance             | $V_I = 0\text{V}$ or $V_{CC}$  | 3.5        | pF            |
| $I_{CCH}$              | Total supply current          | Outputs High; $V_{CC} = 5.5\text{V}$                                 | 150        | $\mu\text{A}$ |

## ORDERING INFORMATION

| PACKAGES                    | TEMPERATURE RANGE                              | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|-----------------------------|--|-----------------------|---------------|------------|
| 20-Pin Plastic DIP          | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 74ABT273A N           | 74ABT273A N   | SOT146-1   |
| 20-Pin plastic SO           | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 74ABT273A D           | 74ABT273A D   | SOT163-1   |
| 20-Pin Plastic SSOP Type II | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 74ABT273A DB          | 74ABT273A DB  | SOT339-1   |
| 20-Pin Plastic TSSOP Type I | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 74ABT273A PW          | 74ABT273A PW  | SOT360-1   |

## PIN CONFIGURATION



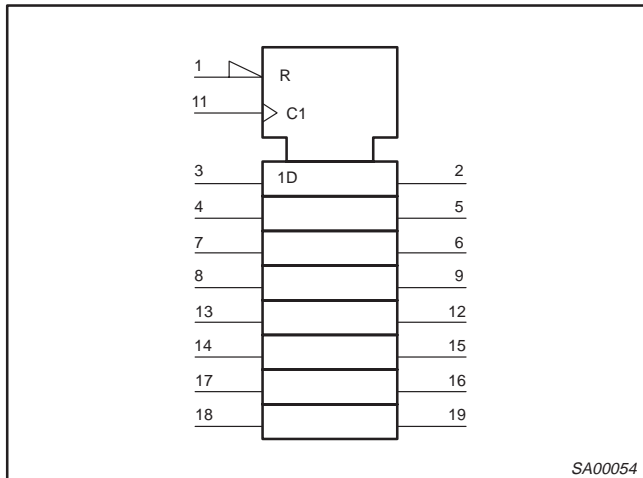
## PIN DESCRIPTION

| PIN NUMBER                 | SYMBOL          | NAME AND FUNCTION                      |
|----------------------------|-----------------|--|
| 11                         | CP              | Clock pulse input (active rising edge) |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0 - D7         | Data inputs                            |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q0 - Q7         | Data outputs                           |
| 1                          | $\overline{MR}$ | Master Reset input (active-Low)        |
| 10                         | GND             | Ground (0V)                            |
| 20                         | $V_{CC}$        | Positive supply voltage                |

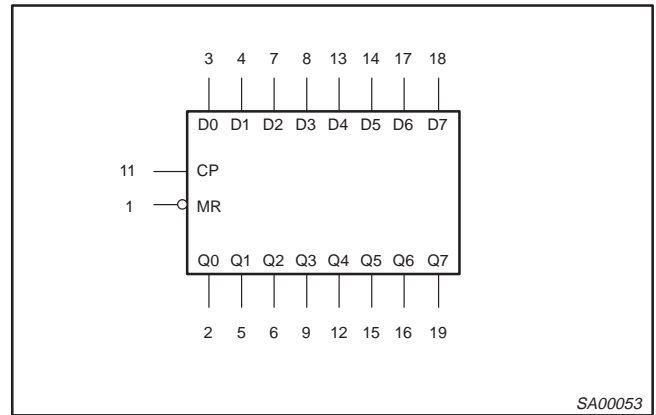
# Octal D-type flip-flop

# 74ABT273A

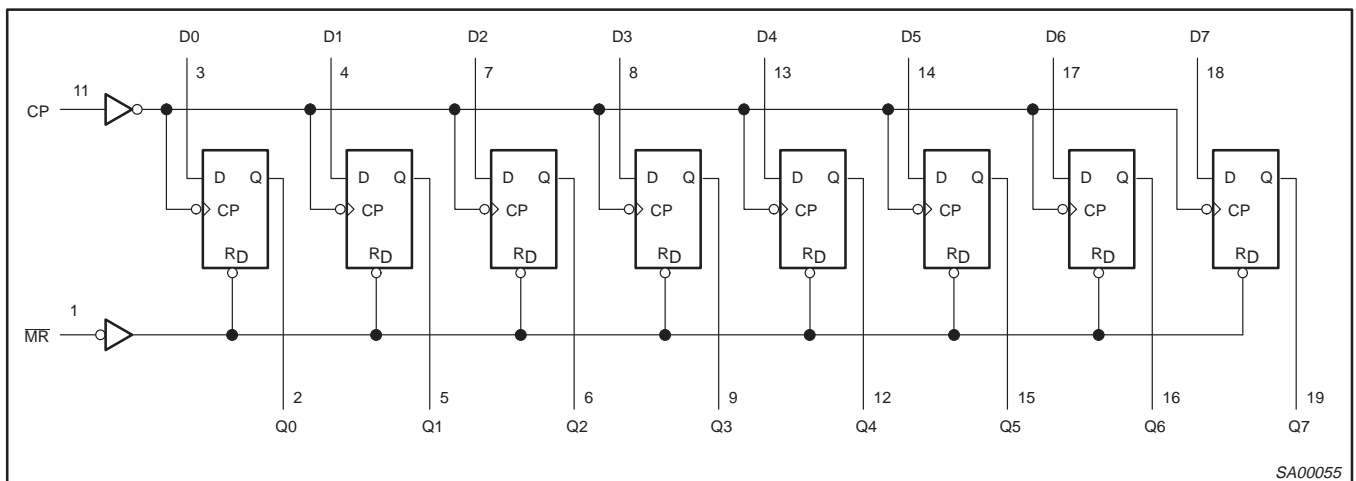
## LOGIC SYMBOL (IEEE/IEC)



## LOGIC SYMBOL



## LOGIC DIAGRAM



## FUNCTION TABLE

| INPUTS          |    |    | OUTPUTS | OPERATING MODE |
|-----------------|----|----|---------|----------------|
| $\overline{MR}$ | CP | Dn | Q0 - Q7 |                |
| L               | X  | X  | L       | Reset (clear)  |
| H               | ↑  | h  | H       | Load "1"       |
| H               | ↑  | l  | L       | Load "0"       |

H = High voltage level  
 h = High voltage level one set-up time prior to the Low-to-High clock transition  
 L = Low voltage level  
 l = Low voltage level one set-up time prior to the Low-to-High clock transition  
 X = Don't care  
 ↑ = Low-to-High clock transition

## Octal D-type flip-flop

74ABT273A

**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

| SYMBOL           | PARAMETER                      | CONDITIONS                  | RATING       | UNIT |
|------------------|--------------------------------|-----------------------------|--------------|------|
| V <sub>CC</sub>  | DC supply voltage              |                             | -0.5 to +7.0 | V    |
| I <sub>IK</sub>  | DC input diode current         | V <sub>I</sub> < 0          | -18          | mA   |
| V <sub>I</sub>   | DC input voltage <sup>3</sup>  |                             | -1.2 to +7.0 | V    |
| I <sub>OK</sub>  | DC output diode current        | V <sub>O</sub> < 0          | -50          | mA   |
| V <sub>OUT</sub> | DC output voltage <sup>3</sup> | output in Off or High state | -0.5 to +5.5 | V    |
| I <sub>OUT</sub> | DC output current              | output in Low state         | 128          | mA   |
| T <sub>stg</sub> | Storage temperature range      |                             | -65 to 150   | °C   |

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL           | PARAMETER                            | LIMITS |                 | UNIT |
|------------------|--------------------------------------|--------|-----------------|------|
|                  |                                      | Min    | Max             |      |
| V <sub>CC</sub>  | DC supply voltage                    | 4.5    | 5.5             | V    |
| V <sub>I</sub>   | Input voltage                        | 0      | V <sub>CC</sub> | V    |
| V <sub>IH</sub>  | High-level input voltage             | 2.0    |                 | V    |
| V <sub>IL</sub>  | Low-level input voltage              |        | 0.8             | V    |
| I <sub>OH</sub>  | High-level output current            |        | -32             | mA   |
| I <sub>OL</sub>  | Low-level output current             |        | 64              | mA   |
| Δt/Δv            | Input transition rise or fall rate   | 0      | 10              | ns/V |
| T <sub>amb</sub> | Operating free-air temperature range | -40    | +85             | °C   |

## Octal D-type flip-flop

74ABT273A

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL           | PARAMETER  | TEST CONDITIONS  | LIMITS                   |       |      |                                   |      | UNIT |
|------------------|--|--|--------------------------|-------|------|-----------------------------------|------|------|
|                  |  |  | T <sub>amb</sub> = +25°C |       |      | T <sub>amb</sub> = -40°C to +85°C |      |      |
|                  |  |  | Min                      | Typ   | Max  | Min                               | Max  |      |
| V <sub>IK</sub>  | Input clamp voltage                                  | V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA  |                          | -0.9  | -1.2 |                                   | -1.2 | V    |
| V <sub>OH</sub>  | High-level output voltage                            | V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>  | 2.5                      | 2.9   |      | 2.5                               |      | V    |
|                  |  | V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>  | 3.0                      | 3.4   |      | 3.0                               |      |      |
|                  |  | V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> | 2.0                      | 2.4   |      | 2.0                               |      |      |
| V <sub>OL</sub>  | Low-level output voltage                             | V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>  |                          | 0.42  | 0.55 |                                   | 0.55 | V    |
| V <sub>RST</sub> | Power-up output low voltage <sup>3</sup>             | V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>                |                          | 0.13  | 0.55 |                                   | 0.55 | V    |
| I <sub>I</sub>   | Input leakage current                                | V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V   |                          | ±0.01 | ±1.0 |                                   | ±1.0 | µA   |
| I <sub>OFF</sub> | Power-off leakage current                            | V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V                                      |                          | ±5.0  | ±100 |                                   | ±100 | µA   |
| I <sub>CEx</sub> | Output High leakage current                          | V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>               |                          | 5.0   | 50   |                                   | 50   | µA   |
| I <sub>O</sub>   | Output current <sup>1</sup>                          | V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V  | -50                      | -70   | -180 | -50                               | -180 | mA   |
| I <sub>CCH</sub> | Quiescent supply current                             | V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>                        |                          | 150   | 250  |                                   | 250  | µA   |
| I <sub>CCL</sub> |  | V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>                         |                          | 24    | 30   |                                   | 30   | mA   |
| ΔI <sub>CC</sub> | Additional supply current per input pin <sup>2</sup> | V <sub>CC</sub> = 5.5V; One data input at 3.4V, other inputs at V <sub>CC</sub> or GND               |                          | 0.5   | 1.5  |                                   | 1.5  | mA   |

## NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

## AC CHARACTERISTICS

GND = 0V; t<sub>R</sub> = t<sub>F</sub> = 2.5ns; C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω

| SYMBOL                               | PARAMETER                     | WAVEFORM | LIMITS  |     |     |  |     | UNIT |
|--------------------------------------|-------------------------------|----------|---|-----|-----|--|-----|------|
|                                      |                               |          | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V |     |     | T <sub>amb</sub> = -40°C to +85°C<br>V <sub>CC</sub> = +5.0V ±0.5V |     |      |
|                                      |                               |          | Min   | Typ | Max | Min  | Max |      |
| f <sub>MAX</sub>                     | Maximum clock frequency       | 1        | 250   | 350 |     | 250  |     | MHz  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>CP to Qn | 1        | 1.5   | 3.0 | 4.0 | 1.5  | 4.8 | ns   |
|                                      |                               |          | 2.0   | 3.4 | 4.6 | 2.0  | 4.8 |      |
| t <sub>PHL</sub>                     | Propagation delay<br>MR to Qn | 2        | 2.5   | 4.5 | 6.0 | 2.5  | 6.6 | ns   |

# Octal D-type flip-flop

# 74ABT273A

## AC SETUP REQUIREMENTS

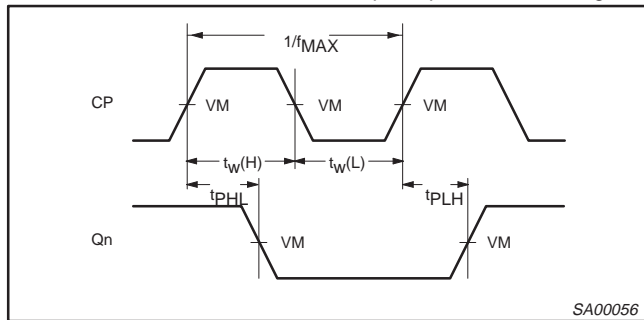
GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

| SYMBOL                             | PARAMETER                           | WAVEFORM | LIMITS   |              |  | UNIT |
|------------------------------------|-------------------------------------|----------|--|--------------|--|------|
|                                    |                                     |          | $T_{\text{amb}} = +25^\circ\text{C}$<br>$V_{\text{CC}} = +5.0\text{V}$ |              | $T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$<br>$V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$ |      |
|                                    |                                     |          | Min  | Typ          | Min  |      |
| $t_s(\text{H})$<br>$t_s(\text{L})$ | Setup time, High or Low<br>Dn to CP | 3        | 1.5<br>1.5   | 0.6<br>0.4   | 1.5<br>1.5   |      |
| $t_h(\text{H})$<br>$t_h(\text{L})$ | Hold time, High or Low<br>Dn to CP  | 3        | 0.7<br>0.7   | -0.5<br>-0.5 | 0.7<br>0.7   | ns   |
| $t_w(\text{H})$<br>$t_w(\text{L})$ | Clock pulse width<br>High or Low    | 1        | 1.5<br>2.0   | 0.8<br>1.0   | 1.5<br>2.0   | ns   |
| $t_w(\text{L})$                    | Master Reset pulse width, Low       | 2        | 1.5  | 0.8          | 1.5  | ns   |
| $t_{\text{REC}}$                   | Recovery time<br>MR to CP           | 2        | 1.5  | 0.5          | 1.5  | ns   |

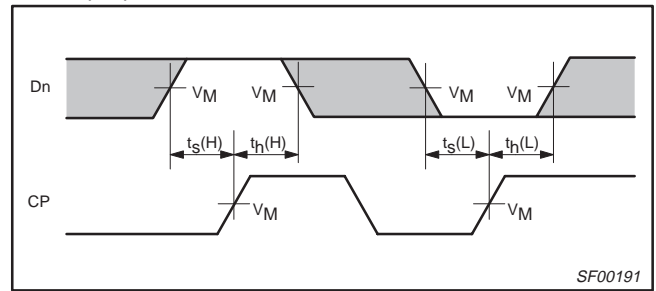
## AC WAVEFORMS

$V_M = 1.5\text{V}$ ,  $V_{\text{IN}} = \text{GND to } 3.0\text{V}$

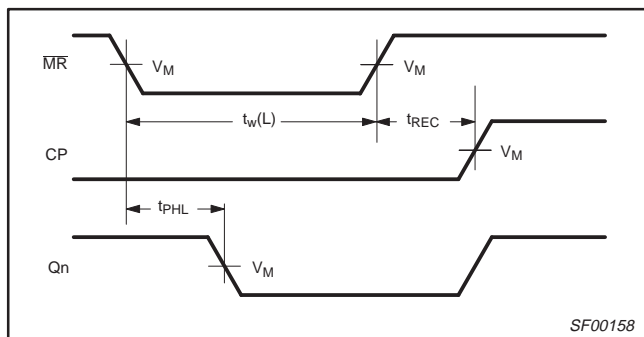
The shaded areas indicate when the input is permitted to change for predictable output performance.



**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**



**Waveform 3. Data Setup and Hold Times**

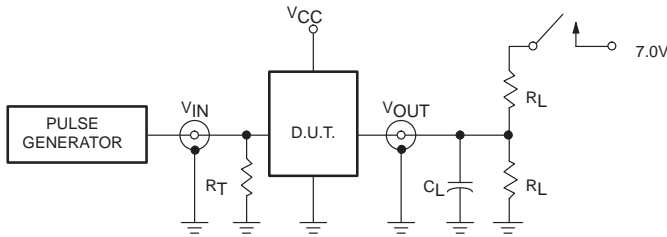


**Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**

# Octal D-type flip-flop

# 74ABT273A

## TEST CIRCUIT AND WAVEFORMS



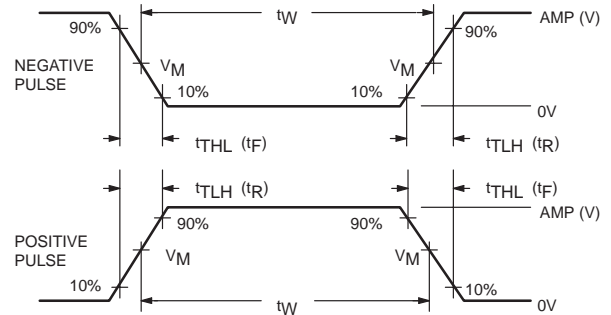
Test Circuit for 3-State Outputs

### SWITCH POSITION

| TEST | SWITCH |
|------|--------|
| All  | open   |

### DEFINITIONS

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

| FAMILY | INPUT PULSE REQUIREMENTS |           |       |       |       |
|--------|--------------------------|-----------|-------|-------|-------|
|        | Amplitude                | Rep. Rate | $t_W$ | $t_R$ | $t_F$ |
| 74ABT  | 3.0V                     | 1MHz      | 500ns | 2.5ns | 2.5ns |

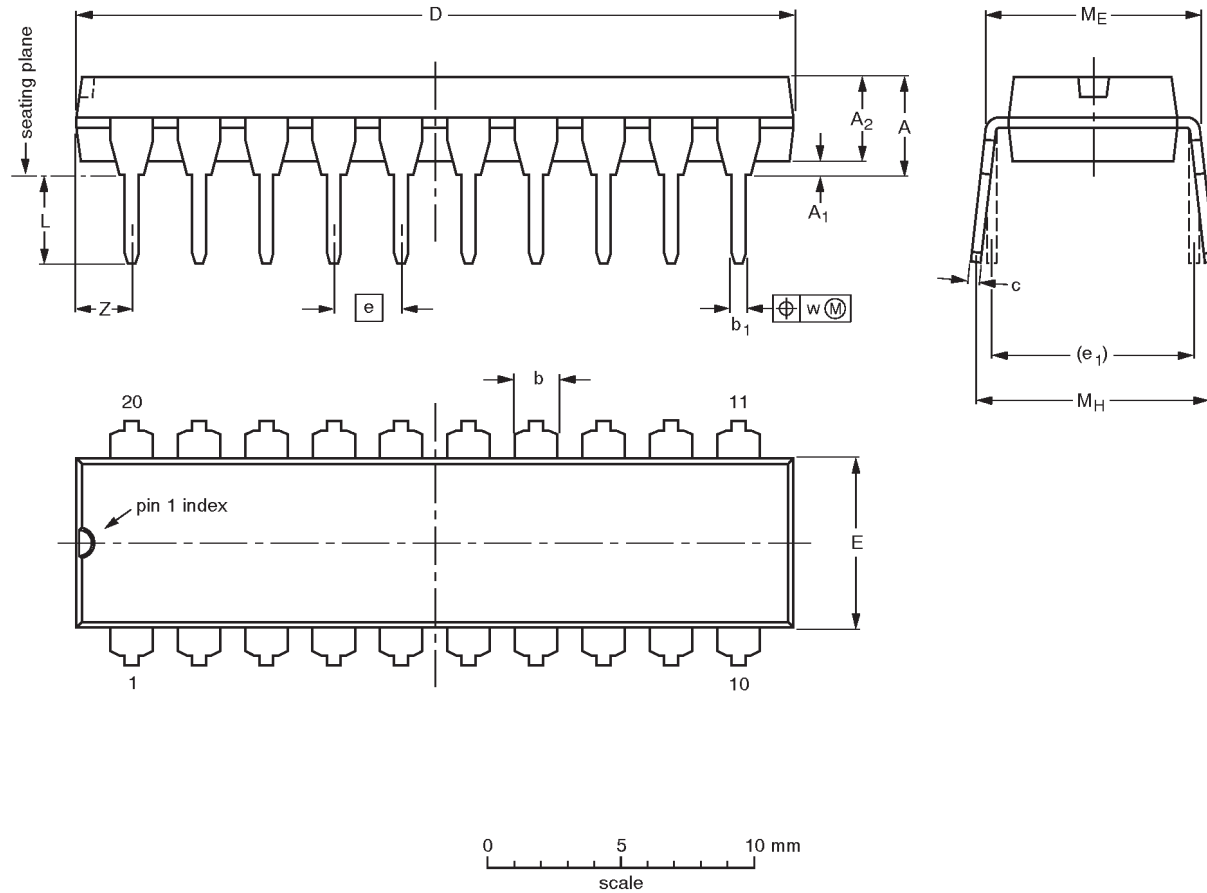
SA00057

# Octal D-type flip-flop

# 74ABT273A

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1




DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w     | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm     | 4.2    | 0.51                | 3.2                 | 1.73<br>1.30   | 0.53<br>0.38   | 0.36<br>0.23   | 26.92<br>26.54   | 6.40<br>6.22     | 2.54 | 7.62           | 3.60<br>3.05 | 8.25<br>7.80   | 10.0<br>8.3    | 0.254 | 2.0                   |
| inches | 0.17   | 0.020               | 0.13                | 0.068<br>0.051 | 0.021<br>0.015 | 0.014<br>0.009 | 1.060<br>1.045   | 0.25<br>0.24     | 0.10 | 0.30           | 0.14<br>0.12 | 0.32<br>0.31   | 0.39<br>0.33   | 0.01  | 0.078                 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |       |       |  | EUROPEAN PROJECTION   | ISSUE DATE           |
|-----------------|------------|-------|-------|--|---|----------------------|
|                 | IEC        | JEDEC | EIAJ  |  |   |                      |
| SOT146-1        |            |       | SC603 |  |  | 92-11-17<br>95-05-24 |

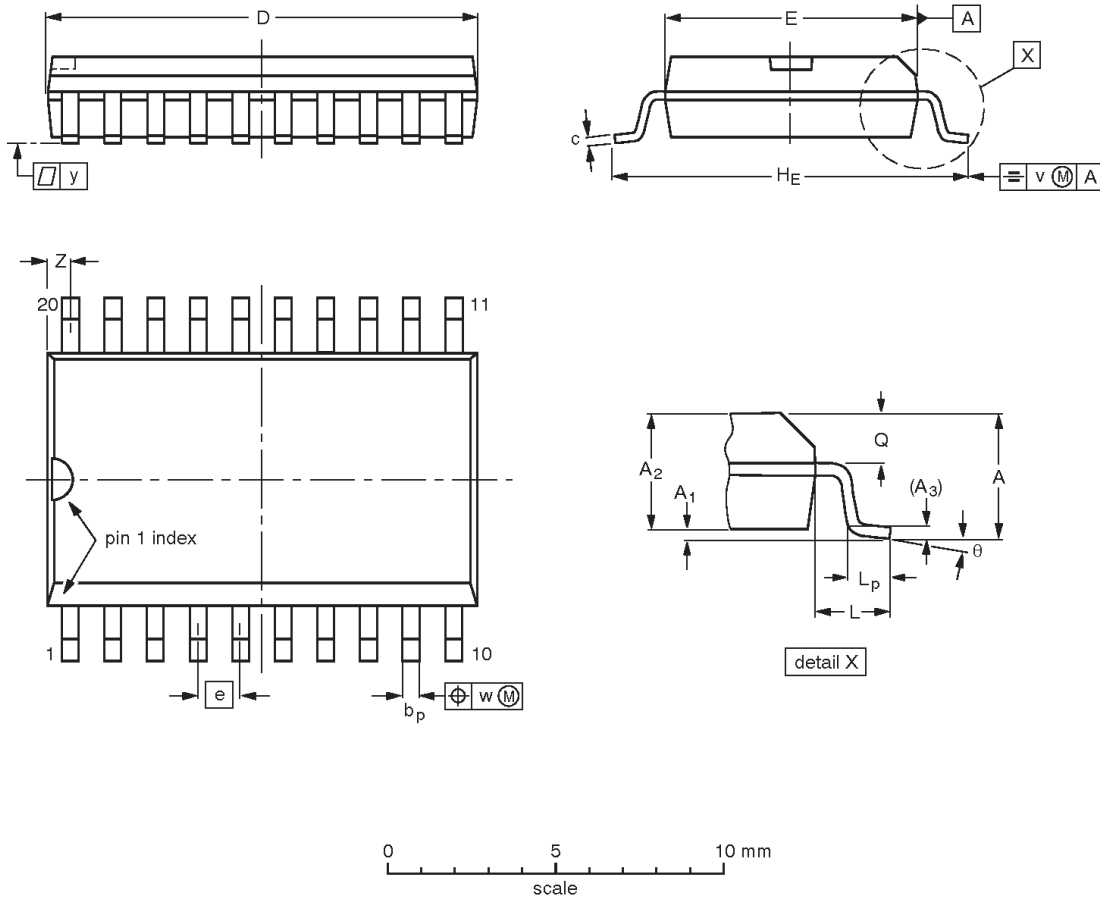


# Octal D-type flip-flop

# 74ABT273A

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 2.65   | 0.30<br>0.10   | 2.45<br>2.25   | 0.25           | 0.49<br>0.36   | 0.32<br>0.23   | 13.0<br>12.6     | 7.6<br>7.4       | 1.27  | 10.65<br>10.00 | 1.4   | 1.1<br>0.4     | 1.1<br>1.0     | 0.25 | 0.25 | 0.1   | 0.9<br>0.4       | 8°<br>0° |
| inches | 0.10   | 0.012<br>0.004 | 0.096<br>0.089 | 0.01           | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49     | 0.30<br>0.29     | 0.050 | 0.42<br>0.39   | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016   |          |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

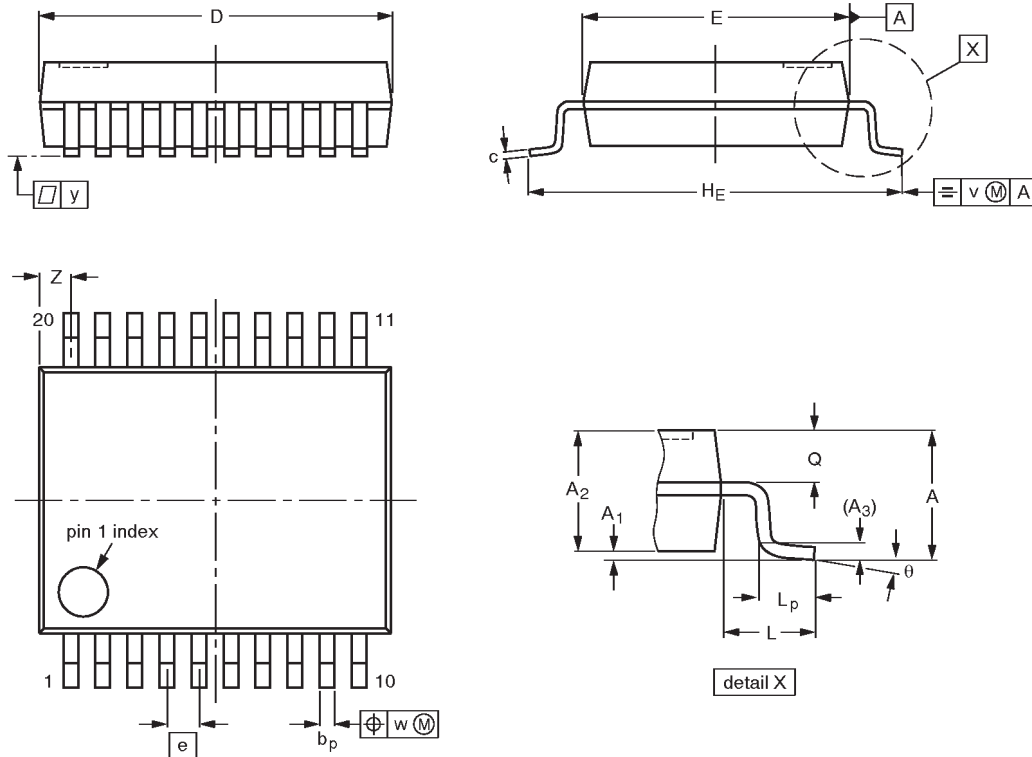
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE            |
|-----------------|------------|----------|------|--|---------------------|-----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                       |
| SOT163-1        | 075E04     | MS-013AC |      |  |                     | -92-11-17<br>95-01-24 |

# Octal D-type flip-flop

# 74ABT273A

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm**

**SOT339-1**



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | HE         | L    | L <sub>p</sub> | Q          | v   | w    | y   | Z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 2.0    | 0.21<br>0.05   | 1.80<br>1.65   | 0.25           | 0.38<br>0.25   | 0.20<br>0.09 | 7.4<br>7.0       | 5.4<br>5.2       | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63   | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 0.9<br>0.5       | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

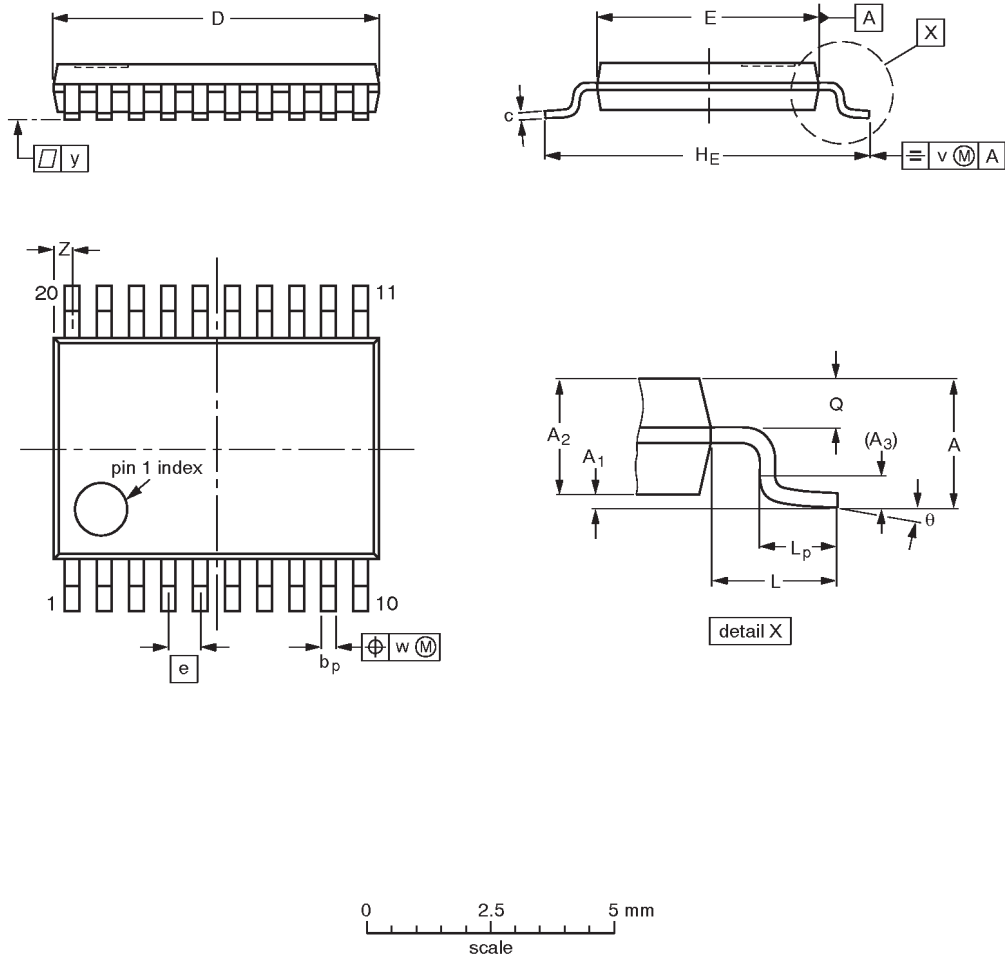
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT339-1        |            | MO-150AE |      |  |                     | 93-09-08<br>95-02-04 |

# Octal D-type flip-flop

# 74ABT273A

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D <sup>(1)</sup> | E <sup>(2)</sup> | e    | H <sub>E</sub> | L   | L <sub>p</sub> | Q          | v   | w    | y   | z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 1.10   | 0.15<br>0.05   | 0.95<br>0.80   | 0.25           | 0.30<br>0.19   | 0.2<br>0.1 | 6.6<br>6.4       | 4.5<br>4.3       | 0.65 | 6.6<br>6.2     | 1.0 | 0.75<br>0.50   | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2       | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE            |
|-----------------|------------|----------|------|--|---------------------|-----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                       |
| SOT360-1        |            | MO-153AC |      |  |                     | -93-06-16<br>95-02-04 |

## Octal D-type flip-flop

74ABT273A

## DEFINITIONS

| Data Sheet Identification        | Product Status                | Definition   |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i>   | <b>Formative or in Design</b> | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.   |
| <i>Preliminary Specification</i> | <b>Preproduction Product</b>  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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