

74ABT273 Octal D-Type Flip-Flop

General Description

The ABT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

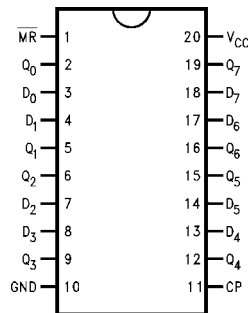
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See ABT377 for clock enable version
- See ABT373 for transparent latch version
- See ABT374 for 3-STATE version
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention

Ordering Code:

Order Number	Package Number	Package Description
74ABT273CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT273CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT273CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT273CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

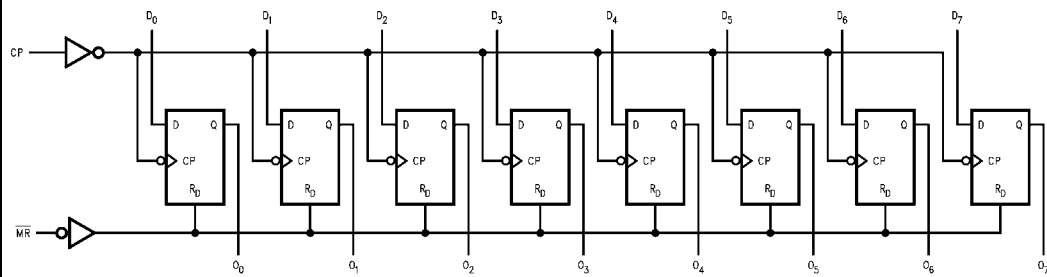
Pin Names	Description
D ₀ -D ₇	Data Inputs
\overline{MR}	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
Q ₀ -Q ₇	Data Outputs

Truth Table

Operating Mode	Inputs			Output
	$\overline{\text{MR}}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load "1"	H	↗	h	H
Load "0"	H	↗	l	L

H = HIGH Voltage Level steady state
 h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW Voltage Level steady state
 l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
 X = Immaterial
 ↗ = LOW-to-HIGH clock transition

Logic Diagram



Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to +4.75V
in the HIGH State	-0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current (Across Comm Operating Range)	-500 mA
Over Voltage Latchup	V _{CC} + 4.5V

Recommended Operating Conditions

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

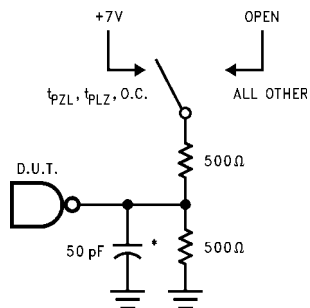
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.5 2.0			V	Min	I _{OH} = -3 mA I _{OH} = -32 mA
V _{OL}	Output LOW Voltage			0.55	V	Min	I _{OL} = 64 mA
I _{IH}	Input HIGH Current			1 1	μA	Max	V _{IN} = 2.7V (Note 3) V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-1 -1	μA	Max	V _{IN} = 0.5V (Note 3) V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OS}	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I _{CCT}	Maximum I _{CC} /Input Outputs Enabled			1.5	mA	Max	V _I = V _{CC} - 2.1V Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} No Load			0.3	mA/ MHz	Max	Outputs Open (Note 4) One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed but not tested.

Note 4: For 8 bits toggling, I_{CCD} < 0.5 mA/MHz.

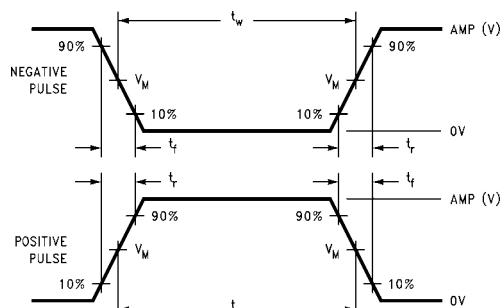
AC Electrical Characteristics									
(SSOIC package)									
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	150	200		150		150		MHz
t _{PLH}	Propagation Delay CP to O _n	2.0		6.0	1.0	7.0	2.0	6.0	ns
t _{PHL}	Propagation Delay MR to O _n	2.8		6.8	1.0	7.5	2.8	6.8	ns
t _{PHL}	Propagation Delay MR to O _n	2.5		7.4	1.0	8.2	2.5	7.4	ns
AC Operating Requirements									
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		Units	
		Min	Max	Min	Max	Min	Max		
t _S (H)	Setup Time, HIGH or LOW D _n to CP	2.0		2.0		2.0		ns	
t _S (L)	Setup Time, LOW or LOW D _n to CP	2.5		2.5		2.5		ns	
t _H (H)	Hold Time, HIGH or LOW D _n to CP	1.2		1.4		1.2		ns	
t _H (L)	Hold Time, LOW or LOW D _n to CP	1.2		1.4		1.2		ns	
t _W (H)	Pulse Width, CP, HIGH or LOW	3.3		3.3		3.3		ns	
t _W (L)	Pulse Width, CP, HIGH or LOW	3.3		3.3		3.3		ns	
t _W (L)	Master Reset Pulse Width, LOW	3.3		3.3		3.3		ns	
t _{REC}	Recovery Time MR to CP	2.0		2.0		2.0		ns	
Capacitance									
(SOIC package)									
Symbol	Parameter	Typ	Units	Conditions T _A = 25°C					
C _{IN}	Input Capacitance	5	pF	V _{CC} = 0V					
C _{OUT} (Note 5)	Output Capacitance	9	pF	V _{CC} = 5.0V					
Note 5: C _{OUT} is measured at frequency f = 1 MHz, per MIL-STD-833, Method 3012.									

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

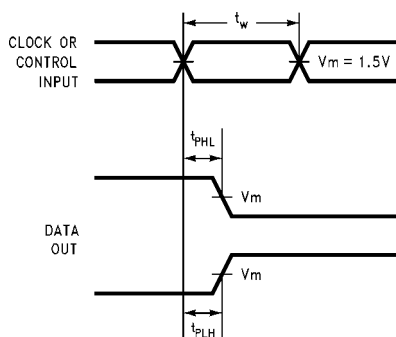


**FIGURE 2. $V_M = 1.5V$
Input Pulse Requirements**

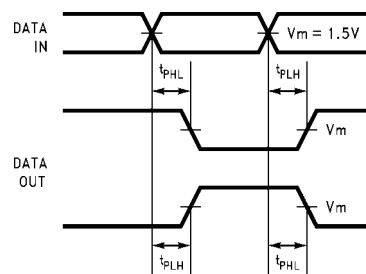
Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

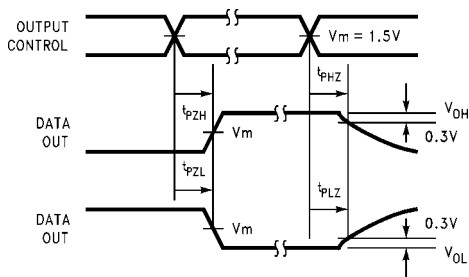
AC Waveforms



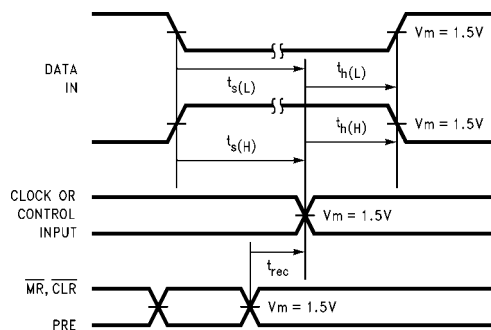
**FIGURE 4. Propagation Delay,
Pulse Width Waveforms**



**FIGURE 6. Propagation Delay Waveforms for
Inverting and Non-Inverting Functions**

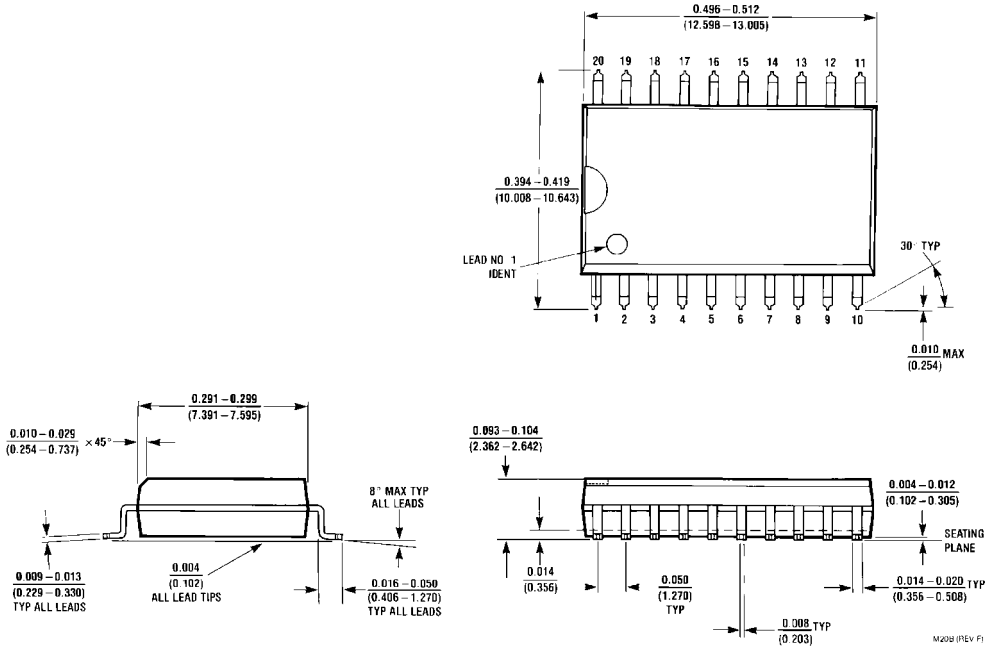


**FIGURE 5. 3-STATE Output HIGH
and LOW Enable and Disable Times**



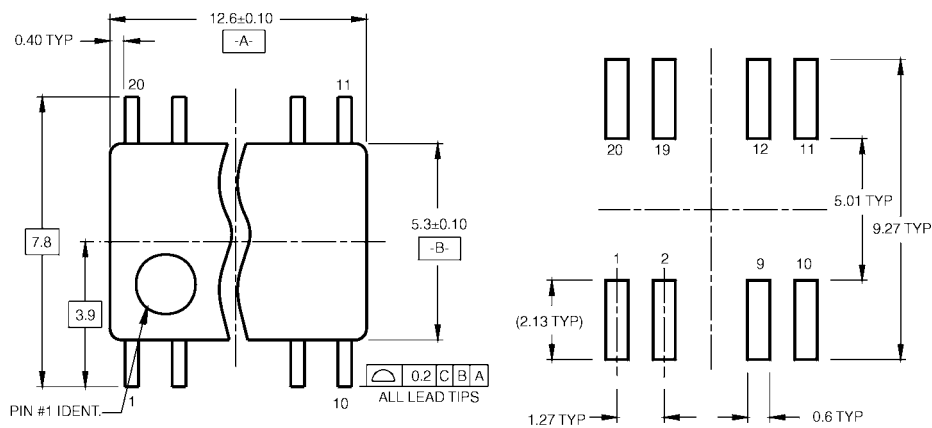
**FIGURE 7. Setup Time, Hold Time
and Recovery Time Waveforms**

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B**

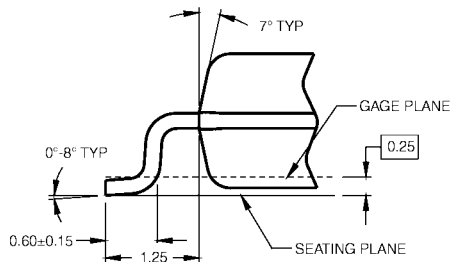
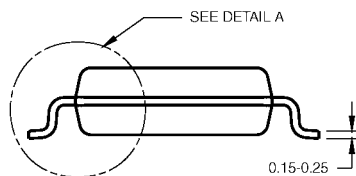
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



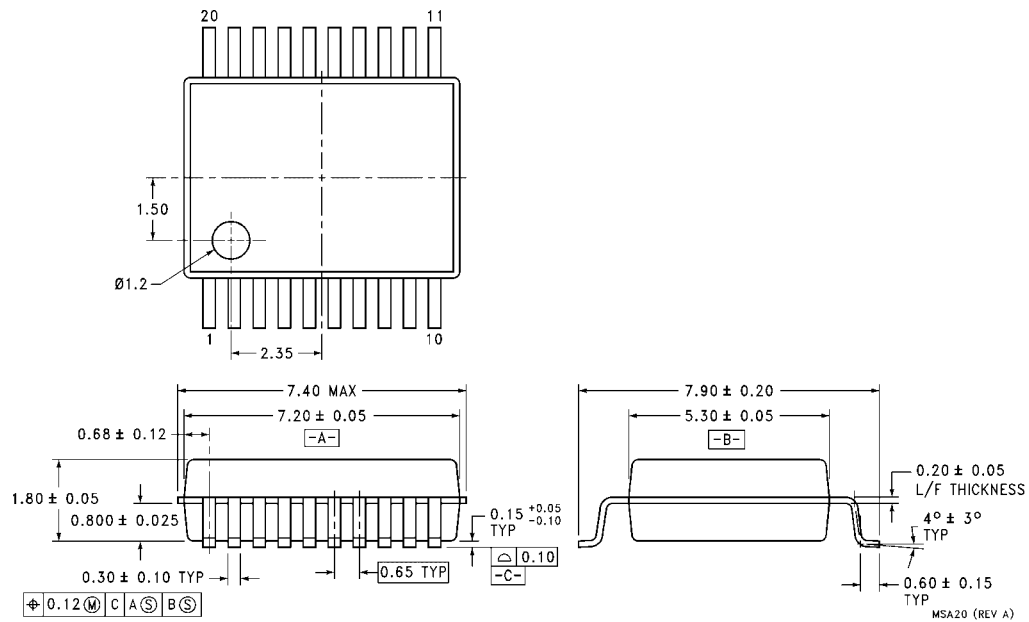
DETAIL A

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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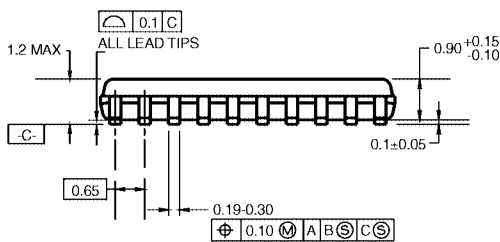
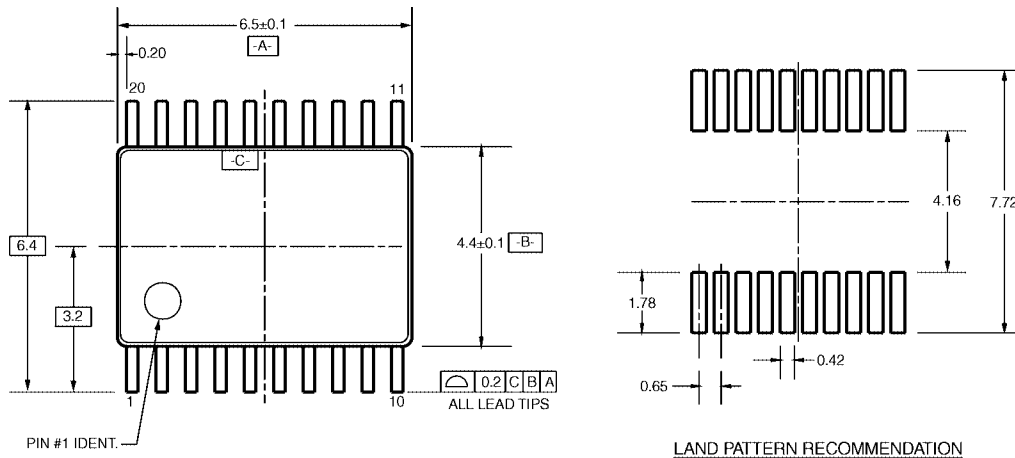
**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

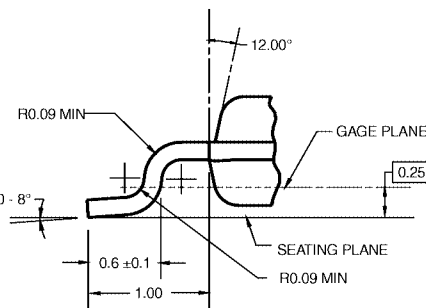
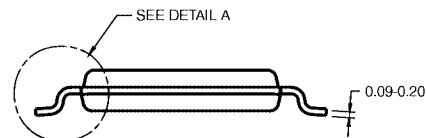


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1



DETAIL A

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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