# STLVDS385

## +3.3V PROGRAMMABLE LVDS TRANSMITTER 24-BIT FLAT PANEL DISPLAY (FPD) LINK-85MHZ

- 20 TO 85 MHz SHIFT CLOCK SUPPORT
- BEST–IN–CLASS SET & HOLD TIMES ON TxINPUTs
- Tx POWER CONSUMPTION <130 mW (typ) @85MHz GRAYSCALE
- Tx POWER-DOWN MODE <200µW (max)
- SUPPORTS VGA, SVGA, XGA aND SINGLE/ DUAL PIXEL SXGA.
- NARROW BUS REDUCES CABLE SIZE AND COST
- UP TO 2.38 Gbps THROUGHPUT
- UP TO 297.5 Megabytes/sec BANDWIDTH
- 345 mV (typ) SWING LVDS DEVICES FOR LOW EMI
- PLL REQUIRES NO EXTERNAL COMPONENTS
- COMPATIBLE WITH TIA/EIA -644 LVDS STANDARD

**TSSOP56**

### DESCRIPTION

The STLVDS385 transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 85 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 297.5 Mbytes/sec. The transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge or Falling edge strobe transmitter will inter operate with a Falling edge strobe Receiver without any translation logic.
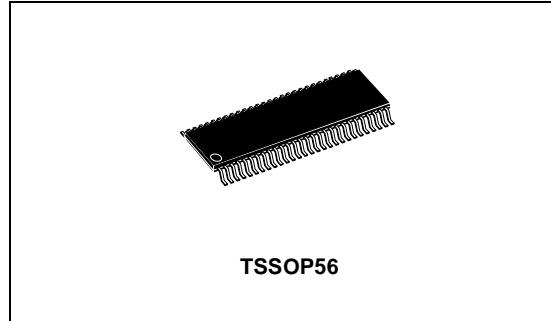
### ORDERING CODES

| Type | Temperature Range | Package | Comments |
|------|-------------------|---------|----------|
| STLVDS385BTR | -10 to 70°C | TSSOP56 (Tape & Reel) | 2000 parts per reel |

## PIN CONFIGURATION
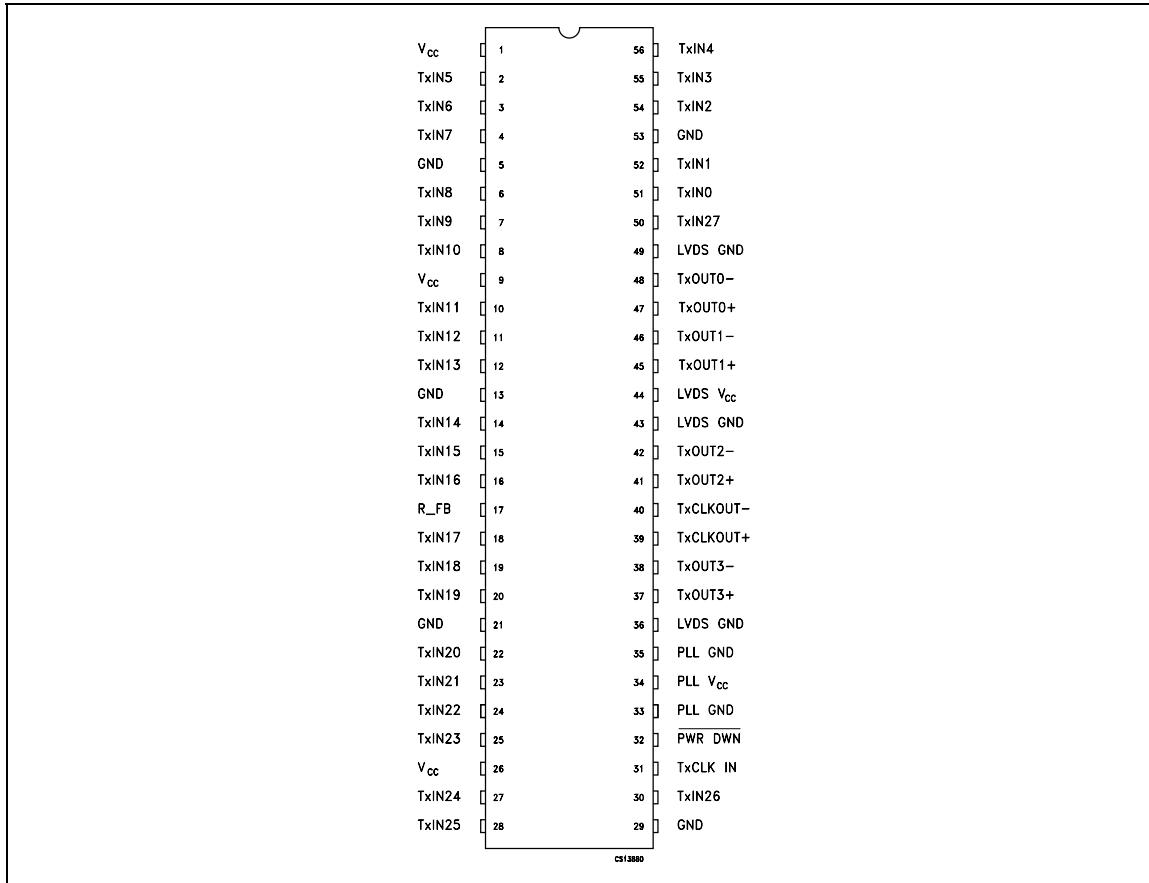


## PIN DESCRIPTION

| PIN N° | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 9, 26 | $V_{CC}$ | Power Supply pins for TTL Inputs |
| 2, 3, 4, 6, 7, 8, 10, 11, 12, 14, 15, 16, 18, 19, 20, 22, 23, 24, 25, 27, 28, 30, 50, 51, 52, 54, 55, 56 | $T_XIN$ | TTL level input. This includes: 8 Red, 8 Green, 8 Blue and 4 control lines-FPLINE, FPFRAME, and DRDY (also referred to as HSYNC, VSYNC, Data Enable) |
| 5, 13, 21, 29 | GND | Ground pins for TTL Inputs |
| 17 | R_FB | Programmable strobe select (See Table 1) |
| 31 | TxCLKIN | TTL level clock input. Pin name TxCLK IN |
| 32 | $\overline{PWRDWN}$ | TTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down |
| 33, 35 | PLL GND | Ground pins for PLL |
| 34 | PLL $V_{CC}$ | Power Supply pin for PLL |
| 36, 43, 49 | LVDS GND | Ground pins for LVDS outputs |
| 37, 41, 45, 47 | TxOUT+ | Positive LVDS differential data output |
| 38, 42, 46, 48 | TxOUT- | Negative LVDS differential data output |
| 39 | TxCLK OUT+ | Positive LVDS differential clock output |
| 40 | TxCLK OUT- | Negative LVDS differential clock output |
| 44 | LVDS $V_{CC}$ | Power Supply pin for LVDS outputs |

**TABLE 1 PROGRAMMABLE TRANSMITTER**

| PIN | CONDITION | STROBE STATUS |
|---|---|---|
| R_FB | R_FB = $V_{CC}$ | Rising edge strobe |
| R_FB | R_FB = GND or NC | Falling edge strobe |

**ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 to 4 | V |
| $V_I$ | CMOS/TTL Input Voltage | -0.5 to ($V_{CC}$ + 0.3) | V |
| $V_{DO}$ | LVDS Driver Output Voltage | -0.3 to ($V_{CC}$ + 0.3) | V |
| $I_{OSD}$ | LVDS Output Short Circuit Duration | Continuous | |
| ESD | HBM | 7 | KV |
| | EIAJ | 500 | V |
| $I_{LATCH}$ | Latch Up Tolerance | ± 300 | mA |
| $T_J$ | Junction Temperature | +150 | °C |
| $T_{stg}$ | Storage Temperature Range | -65 to +150 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| $T_A$ | Operating Free Air Temperature | 0 | | 70 | °C |
| $\Delta V_{CC}$ | Supply Noise Voltage | | | 100 | $mV_{PP}$ |
| $f_{TxCLKIN}$ | TxCLKIN frequency | 20 | | 85 | MHz |

**RECOMMENDED TRANSMITTER INPUT CHARACTERISTICS** ($V_{CC}$ = 3.3V, $T_J$ = -10 to 70°C unless otherwise noted. Typical values are referred to $T_A$ = 25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{CIT}$ | TxCLK IN Transition Time (Fig. 5) | 1.0 | | 6.0 | ns |
| $t_{CIP}$ | TxCLK IN Period (Fig. 6) | 11.76 | T | 50 | ns |
| $t_{CIH}$ | TxCLK IN High Time (Fig. 6) | 0.35T | 0.5T | 0.65T | ns |
| $t_{CIL}$ | TxCLK IN Low Time (Fig. 6) | 0.35T | 0.5T | 0.65T | ns |
| $t_{XIT}$ | TxIN Transition Time | 1.5 | | 6.0 | ns |

**ELECTRICAL CHARACTERISTICS**

**LVCMOS/LVTTL DC SPECIFICATIONS** ($V_{CC}$ = 3.3V, $T_J$ = -10 to 70°C unless otherwise noted. Typical values are referred to $T_A$ = 25°C)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | 2.0 | | $V_{CC}$ | mV |
| $V_{IL}$ | Low Level Input Voltage | | GND | | 0.8 | mV |
| $V_{CL}$ | Input Clamp Voltage | $I_{CL}$ = -18mA | | -0.79 | -1.5 | V |
| $I_I$ | Input Current | $V_I$ =0.4 V, 2.5 or $V_{CC}$ | | | 10 | µA |
| | | $V_I$ = GND | -10 | 0 | | µA |

**LVDS DC SPECIFICATIONS** ($V_{CC}$ = 3.3V, $T_J$ = -10 to 70°C unless otherwise noted. Typical values are referred to $T_A$ = 25°C)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
| $V_{OD}$ | Differential Output Voltage | $R_L$ = 100Ω | 250 | 345 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between Complimentary Output States | $R_L$ = 100Ω | | | 35 | mV |
| $V_{OS}$ | Offset Voltage (Note 2) | $R_L$ = 100Ω | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between Complimentary Output States | $R_L$ = 100Ω | | | 35 | mV |
| $I_{OS}$ | Output Short Circuit Current | $V_O$ = 0,      $R_L$ = 100Ω | | -3.5 | -5 | mA |
| $I_{OZ}$ | Output Tri-State Current | POWERDOWN = 0, $V_O$ = 0 or $V_{CC}$ | | ±1 | ±10 | µA |

**TRANSMITTER SUPPLY CURRENT** ($V_{CC}$ = 3.3V, $T_J$ = -10 to 70°C unless otherwise noted. Typical values are referred to $T_A$ = 25°C)

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|---|------|------|------|------|
| ICCTW | Transmitter Supply Current Worst Case | $R_L$ = 100Ω, $C_L$ = 5pF, Worst Case Pattern (Fig. 1, 3) | f = 32.5 MHz | | 31 | 45 | mA |
| | | | f = 40 MHz | | 32 | 50 | |
| | | | f = 65 MHz | | 37 | 55 | |
| | | | f = 85 MHz | | 42 | 60 | |
| ICCTG | Transmitter Supply Current 16 Grayscale | $R_L$ = 100Ω, $C_L$ = 5pF, 16 Grayscale Pattern (Fig. 1, 3) | f = 32.5 MHz | | 29 | 38 | mA |
| | | | f = 40 MHz | | 30 | 40 | |
| | | | f = 65 MHz | | 35 | 45 | |
| | | | f = 85 MHz | | 39 | 50 | |
| ICCTZ | Transmitter Supply Current Power Down | Powerdown = Low Driver Outputs in Tri-State under Power Down Mode | | | 10 | 55 | µA |

**TRANSMITTER SWITCHING CHARACTERISTICS** ($V_{CC}$ = 3.3V, $T_J$ = -10 to 70°C unless otherwise noted. Typical values are referred to $T_A$ = 25°C)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{LLHT}$ | LVDS Low-to-High Transition Time (Fig. 4) | | | 0.75 | 1.5 | ns |
| $t_{LLLT}$ | LVDS High-to-Low Transition Time (Fig. 4) | | | 0.75 | 1.5 | ns |
| $t_{TPP0}$ | Transmitter Output Pulse Position for BIT 0 (Fig.11 - Note 3) | f = 40 MHz | -0.25 | 0 | 0.25 | ns |
| $t_{TPP1}$ | Transmitter Output Pulse Position for BIT 1 | | 3.32 | 3.57 | 3.82 | ns |
| $t_{TPP2}$ | Transmitter Output Pulse Position for BIT 2 | | 6.89 | 7.14 | 7.39 | ns |
| $t_{TPP3}$ | Transmitter Output Pulse Position for BIT 3 | | 10.46 | 10.71 | 10.96 | ns |
| $t_{TPP4}$ | Transmitter Output Pulse Position for BIT 4 | | 14.04 | 14.29 | 14.54 | ns |
| $t_{TPP5}$ | Transmitter Output Pulse Position for BIT 5 | | 17.61 | 17.86 | 18.11 | ns |
| $t_{TPP6}$ | Transmitter Output Pulse Position for BIT 6 | | 21.18 | 21.43 | 21.68 | ns |
| $t_{TPP0}$ | Transmitter Output Pulse Position for BIT 0 (Fig.11 - Note 3) | f = 65 MHz | -0.20 | 0 | 0.20 | ns |
| $t_{TPP1}$ | Transmitter Output Pulse Position for BIT 1 | | 2.00 | 2.20 | 2.40 | ns |
| $t_{TPP2}$ | Transmitter Output Pulse Position for BIT 2 | | 4.20 | 4.40 | 4.60 | ns |
| $t_{TPP3}$ | Transmitter Output Pulse Position for BIT 3 | | 6.39 | 6.59 | 6.79 | ns |
| $t_{TPP4}$ | Transmitter Output Pulse Position for BIT 4 | | 8.59 | 8.79 | 8.99 | ns |
| $t_{TPP5}$ | Transmitter Output Pulse Position for BIT 5 | | 10.79 | 10.99 | 11.19 | ns |
| $t_{TPP6}$ | Transmitter Output Pulse Position for BIT 6 | | 12.99 | 13.19 | 13.99 | ns |
| $t_{TPP0}$ | Transmitter Output Pulse Position for BIT 0 (Fig.11 - Note 3) | f = 85 MHz | -0.20 | 0 | 0.20 | ns |
| $t_{TPP1}$ | Transmitter Output Pulse Position for BIT 1 | | 1.48 | 1.68 | 1.88 | ns |
| $t_{TPP2}$ | Transmitter Output Pulse Position for BIT 2 | | 3.16 | 3.36 | 3.56 | ns |
| $t_{TPP3}$ | Transmitter Output Pulse Position for BIT 3 | | 4.84 | 5.04 | 5.24 | ns |
| $t_{TPP4}$ | Transmitter Output Pulse Position for BIT 4 | | 6.52 | 6.72 | 6.92 | ns |
| $t_{TPP5}$ | Transmitter Output Pulse Position for BIT 5 | | 8.20 | 8.40 | 8.60 | ns |
| $t_{TPP6}$ | Transmitter Output Pulse Position for BIT 6 | | 9.88 | 10.08 | 10.28 | ns |
| $t_{STC}$ | TxIN Setup to TxCLK IN (Fig. 6) | | 2.5 | | | ns |
| $t_{HTC}$ | TxIN Hold to TxCLK IN (Fig. 6) | | 0 | | | ns |
| $t_{CCD}$ | TxCLK IN to TxCLK OUT Delay (Fig. 7) | $T_A$ = 25°C, $V_{CC}$ = 3.3V | 3.8 | | 6.3 | ns |
| $t_{CCD}$ | TxCLK IN to TxCLK OUT Delay (Fig. 7) | | 2.8 | | 7.1 | ns |
| $t_{JCC}$ | Transmitter Jitter Cycle-to-Cycle (Fig. 12 - Note 4) | f = 85 MHz | | 110 | 150 | ps |
| | | f = 65 MHz | | 210 | 230 | |
| | | f = 40 MHz | | 350 | 370 | |
| $t_{PLLS}$ | Transmitter Phase Lock Loop Set (Fig. 8) | | | | 10 | ms |
| $t_{PDD}$ | Transmitter Power Down Delay (Fig. 10) | | | | 100 | ns |

Note 1: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except $V_{OD}$ and $\Delta V_{OD}$).
Note 2: $V_{OS}$ previously referred as $V_{CM}$.
Note 3: The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature range. This parameter is functionality tested only on Automatic Test Equipment (ATE).
Note 4: The limits are based on bench characterization of the device's jitter response over the power supply voltage range. Output clock jitter is measured with a cycle-to-cycle jitter of ± 3ns applied to the input clock signal while data inputs are switching (See Figures 15 and 16). A jitter event of 3ns, represents worse case jump in the clock edge from most graphics controller VGA chips currently available.
Note 5: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.
Note 6: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.
Note 7: Figures 1, 2 show a falling edge data strobe (TxCLK IN/RxCLK OUT).
Note 8: Recommended pin to signal mapping. Customer may choose to define differently.

## AC TIMING DIAGRAMS

**Figure 1 :** "Worst Case" Test Pattern (Note 5)
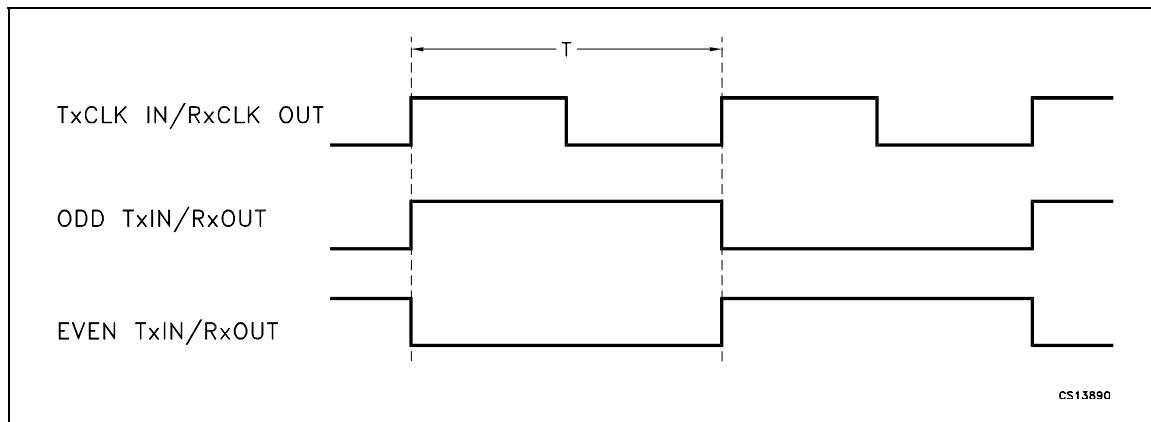
**Figure 2 :** "16 Grayscale" Test Patter (Notes 6, 7, 8)
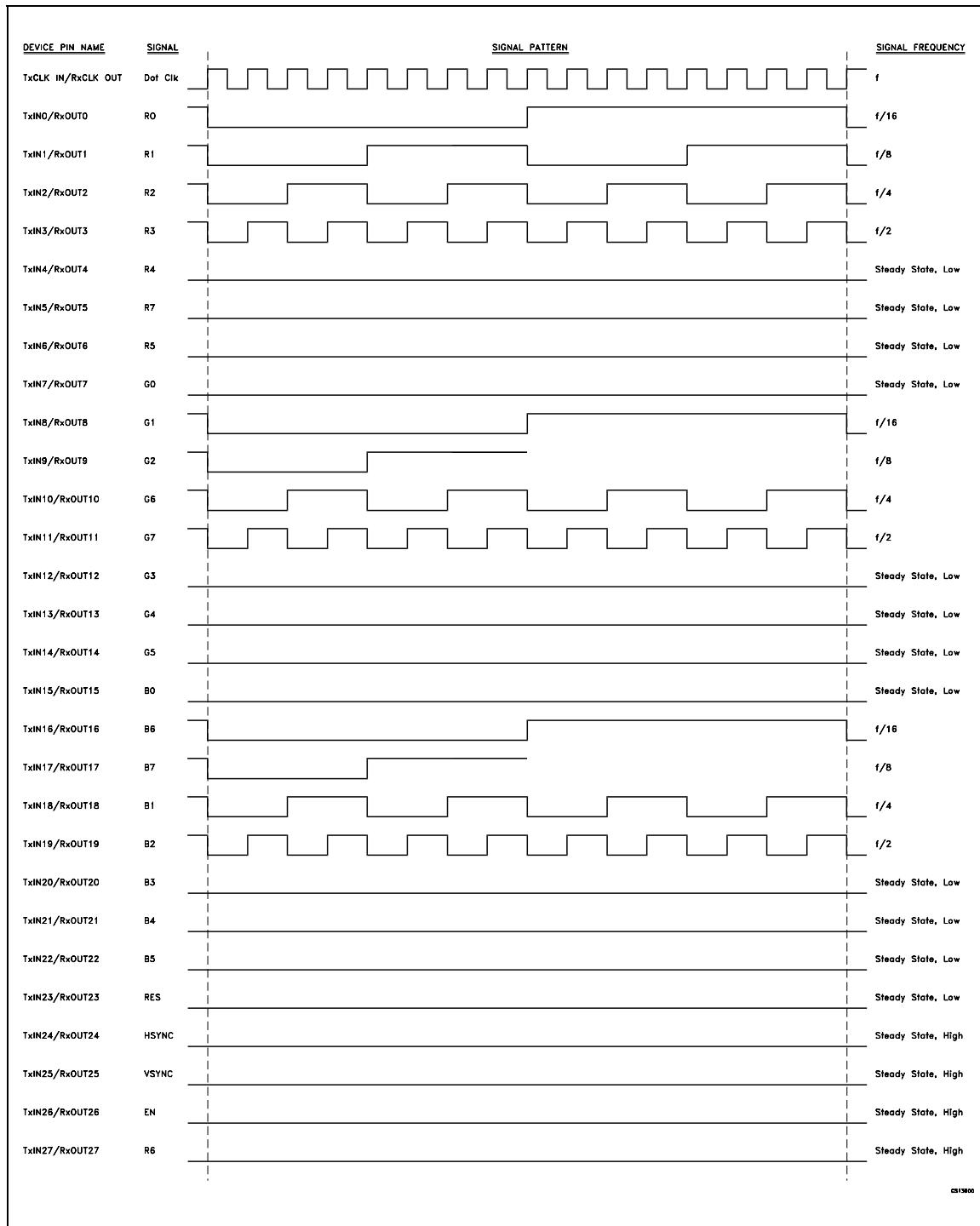
**Figure 3 :** (Transmitter) LVDS Output Load
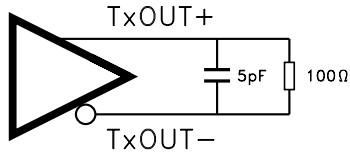


**Figure 4 :** (Transmitter) LVDS Transition Time
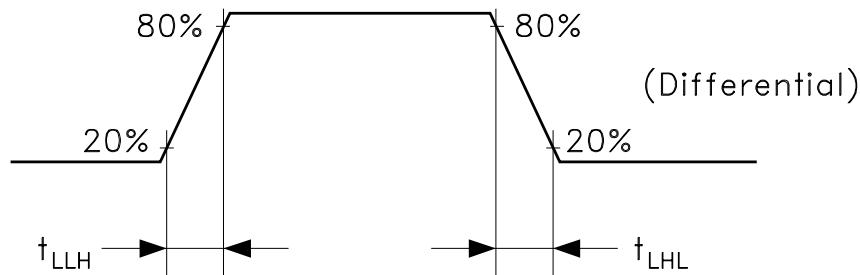


**Figure 5 :** (Transmitter) Input Clock Transition Time
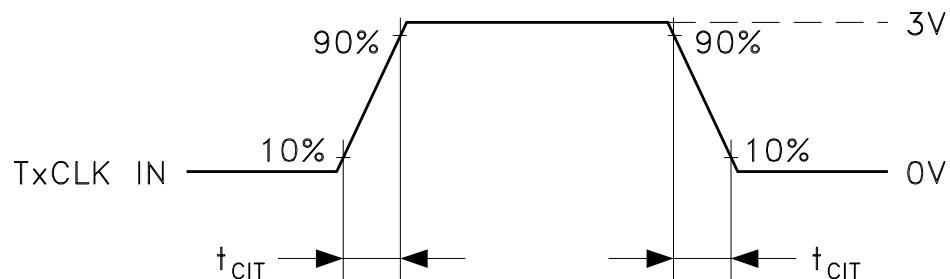
**Figure 6 :** (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)
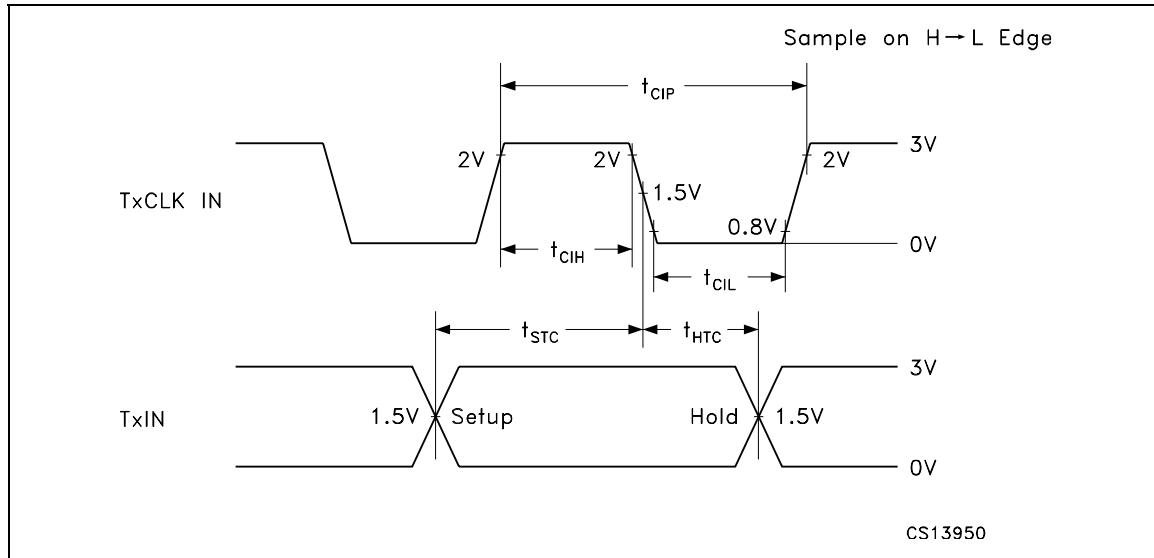


**Figure 7 :** (Transmitter) Clock In to Clock Out Delay
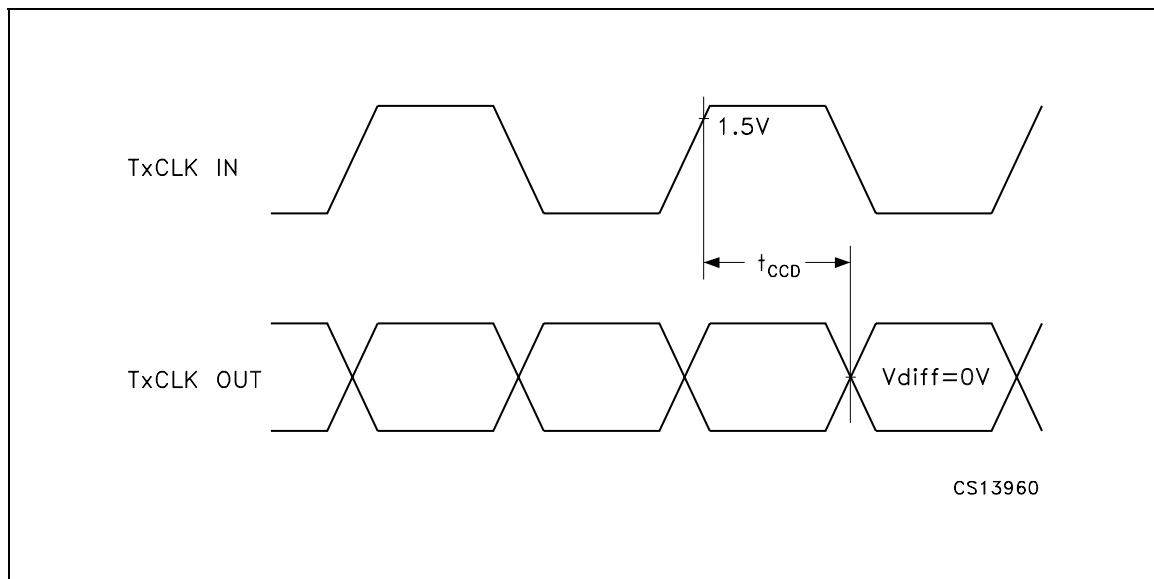
**Figure 8 :** (Transmitter) Phase Lock Loop Set Time
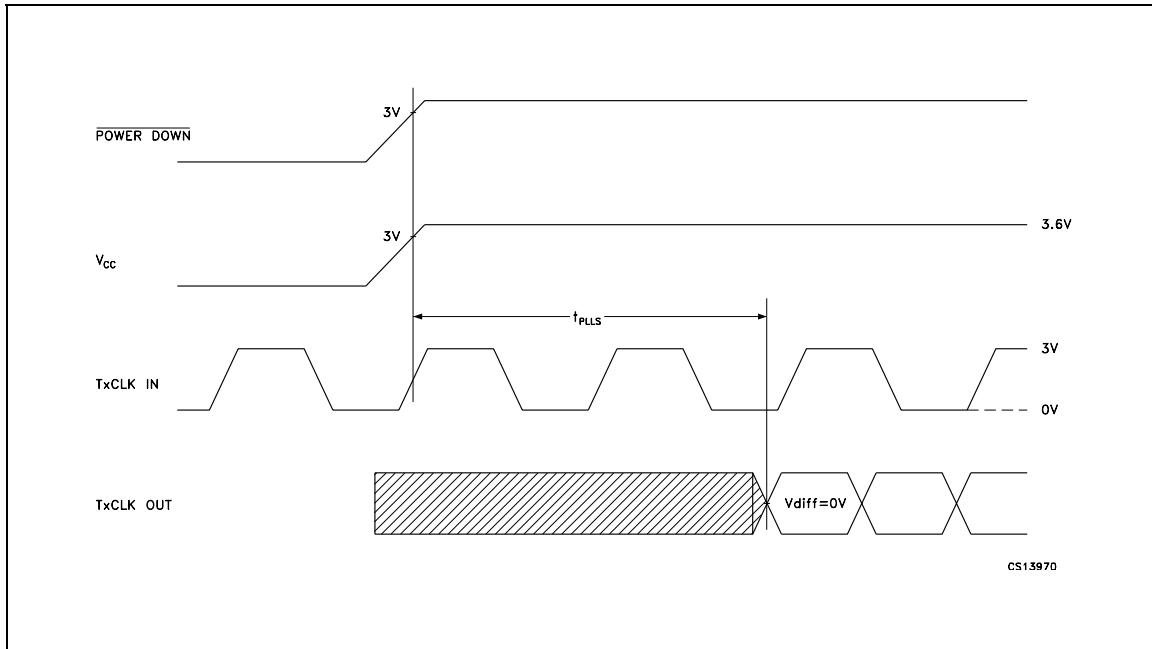


**Figure 9 :** 28 Parallel TTL Data Inputs Mapped to LVDS Outputs
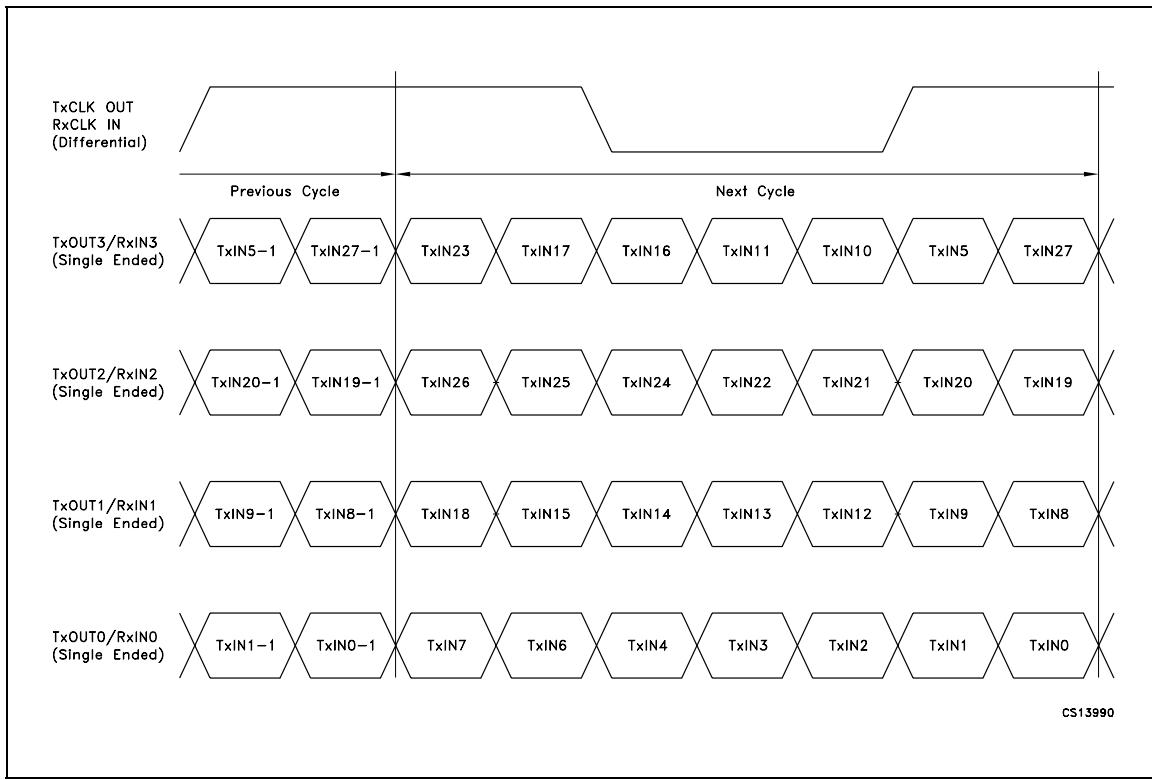
**Figure 10 :** Transmitter Power Down Delay
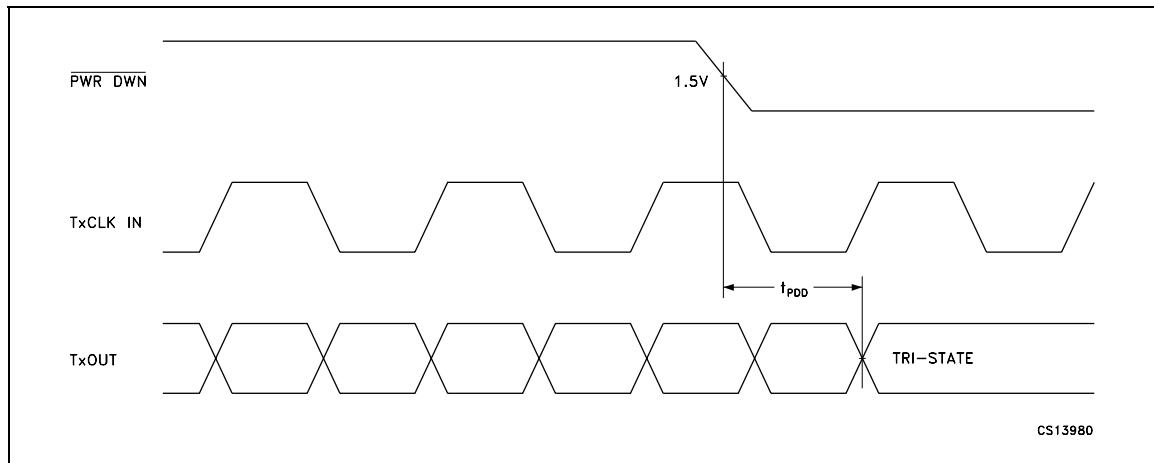


**Figure 11 :** Transmitter LVDS Output Pulse Position Measurement
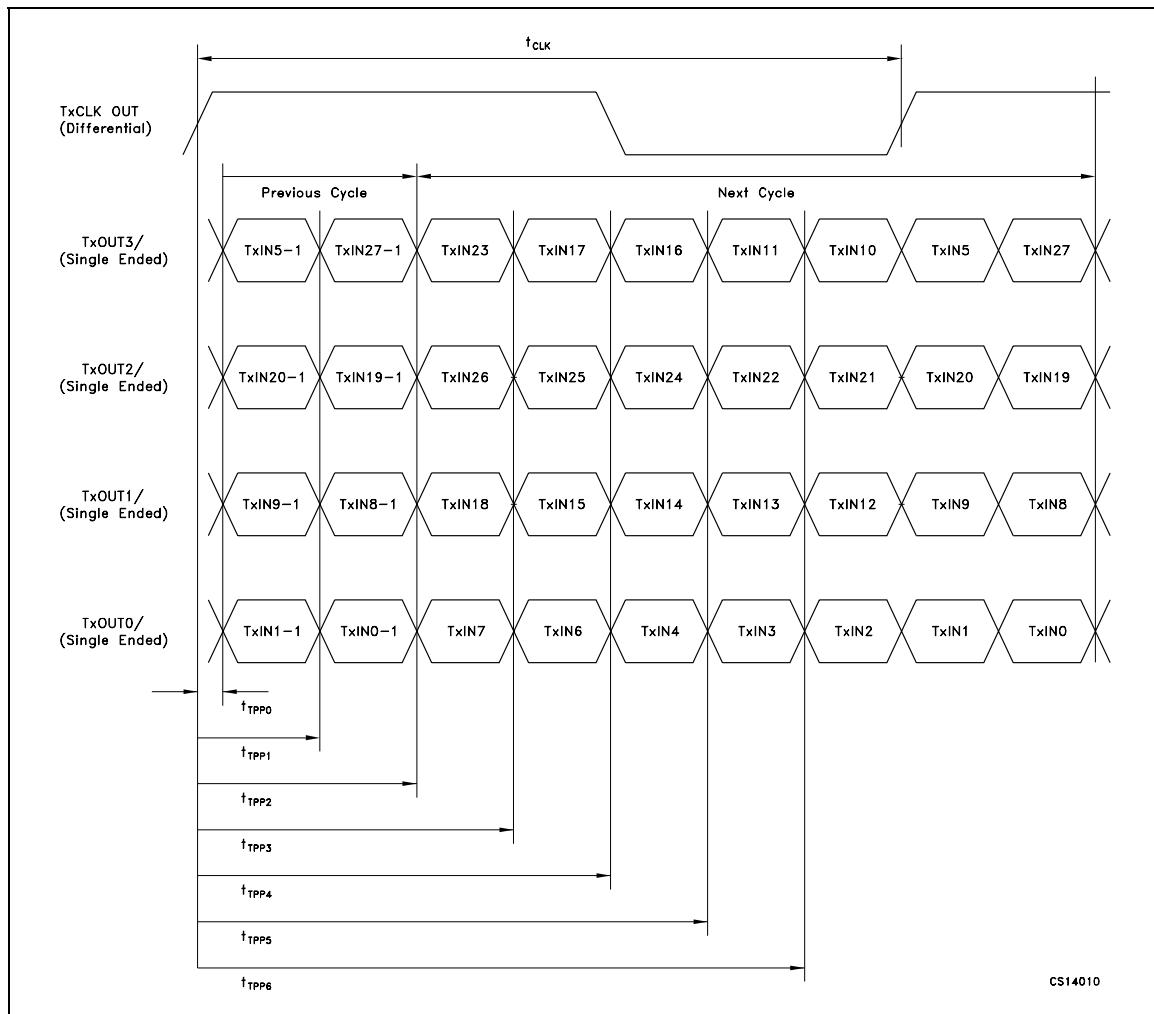
## TSSOP56 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|------|------|------|------|------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | | 0.9 | | | 0.035 | |
| b | 0.17 | | 0.27 | 0.0067 | | 0.011 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.0079 |
| D | 13.9 | | 14.1 | 0.547 | | 0.555 |
| E | 7.95 | | 8.25 | 0.313 | | 0.325 |
| E1 | 6.0 | | 6.2 | 0.236 | | 0.244 |
| e | | 0.5 BSC | | | 0.0197 BSC | |
| K | 0˚ | | 8˚ | 0˚ | | 8˚ |
| L | 0.45 | | 0.75 | 0.020 | | 0.030 |

PIN 1 IDENTIFICATION

7065590B
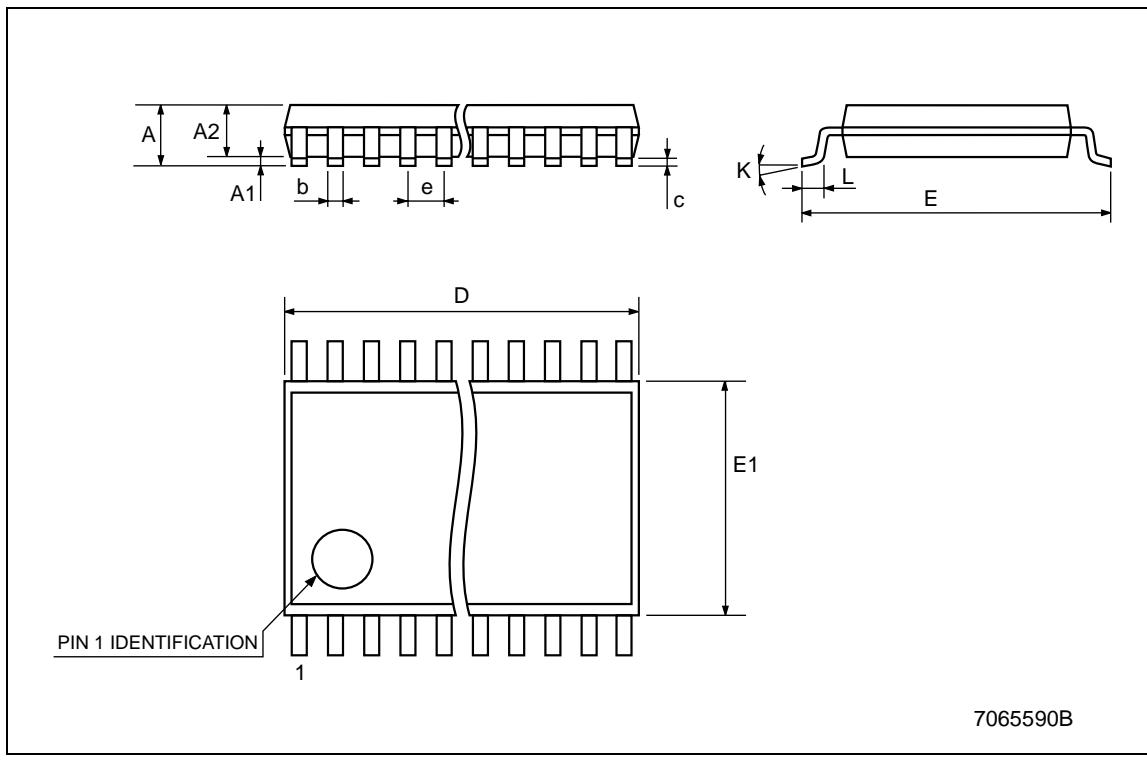
# Tape & Reel TSSOP56 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|-----|-----|------|------|------|------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 30.4 | | | 1.197 |
| Ao | 8.7 | | 8.9 | 0.342 | | 0.350 |
| Bo | 17.2 | | 17.4 | 0.677 | | 0.685 |
| Ko | 1.4 | | 1.6 | 0.055 | | 0.063 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 11.9 | | 12.1 | 0.468 | | 0.476 |

Note: Drawing not in scale