MOTOROLA

MC33206
MC33207

LOW VOLTAGE RAIL–TO–RAIL OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

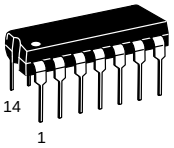
Rail-To-Rail Operational Amplifiers with Enable Feature

The MC33206/7 family of operational amplifiers provide rail–to–rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs and the output can swing within 50 mV of each rail. This rail–to–rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (±0.9 V) yet can operate with a single supply of up to 12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum.

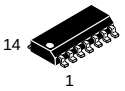
The MC33206/7 has an enable mode that can be controlled externally. The typical supply current in the standby mode is <1.0 μA (V_{Enable} = Gnd). The addition of an enable function makes this amplifier an ideal choice for power sensitive applications, battery powered equipment (instrumentation and monitoring), portable telecommunication, and sample–and–hold applications.

- Standby Mode (I_D ≤1.0 μA, Typ)
- Low Voltage, Single Supply Operation (1.8 V and Ground to 12 V and Ground)
- Rail–to–Rail Input Common Mode Voltage Range
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over–Driven Input Signals
- High Output Current (I_{SC} = 80 mA, Typ)
- Low Supply Current (I_D = 0.9 mA, Typ)
- 600 Ω Output Drive Capability
- Typical Gain Bandwidth Product = 2.2 MHz

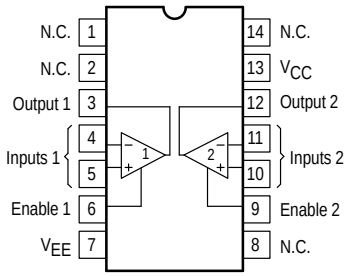
MC33206



P SUFFIX
PLASTIC PACKAGE
CASE 646

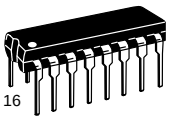


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



(Dual, Top View)

MC33207



P SUFFIX
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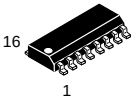
CASE 648



D SUFFIX
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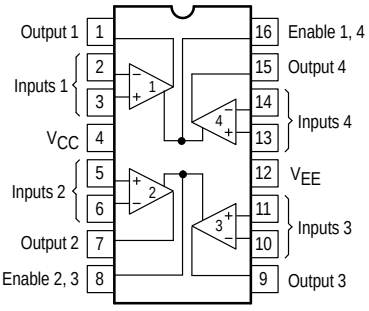
CASE 751B
(SO–16)



(Quad, Top View)

ORDERING INFORMATION

Operational Amplifier Function	Device	Operating Temperature Range	Package
Dual	MC33206D	T_A= –40 ° to +105°C	SO–14
	MC33206P		Plastic DIP
Quad	MC33207D		SO–16
	MC33207P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	13	V
ESD Protection Voltage at any Pin Human Body Model	V_{ESD}	2,000	V
Voltage at any Device Pin	V_{DP}	$V_S \pm 0.5$	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Common Mode Input Voltage Range (Note 2)	V_{CM}	V_{CC} + 0.5 to V_{EE} – 0.5	V
Output Short Circuit Duration (Note 3)	t_S	(Note 3)	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Maximum Power Dissipation	P_D	(Note 3)	mW

NOTES: 1. The differential input voltage of each amplifier is limited by two internal parallel back–to–back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
2. The common–mode input voltage range of each amplifier is limited by diodes connected from the inputs to both power supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
4. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{Enable} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} 0 to 0.5 V, V_{CM} 1.0 to 5.0 V)	–	V_{IO}				mV
MC33206: T_A = 25°C			–	0.5	8.0	
T_A = –40° to +105°C			–	1.0	11	
MC33207: T_A = 25°C			–	0.5	10	
T_A = –40° to +105°C			–	1.0	13	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω) T_A = –40° to +105°C	–	$\Delta V_{IO}/\Delta T$	–	2.0	–	µV/°C
Input Bias Current (V_{CM} = 0 to 0.5 V, V_{CM} = 1.0 to 5.0 V)	–	$\lvert I_{IB} \rvert$				nA
T_A = 25°C			–	80	200	
T_A = –40° to +105°C			–	100	250	
Input Offset Current (V_{CM} = 0 to 0.5 V, V_{CM} = 1.0 to 5.0 V)	–	$\lvert I_{IO} \rvert$				nA
T_A = 25°C			–	5.0	50	
T_A = –40° to +105°C			–	10	100	
Common Mode Input Voltage Range	–	V_{ICR}	– V_{EE}	V_{CC} + 0.2 V_{EE} – 0.2	V_{CC} –	V
Large Signal Voltage Gain (V_{CC} = 5.0 V, V_{EE} = –5.0 V)	–	A_{VOL}				kV/V
R_L = 10 kΩ			50	300	–	
R_L = 600 Ω			25	250	–	
Output Voltage Swing (V_{ID} = ±0.2 V)	–					V
R_L = 10 kΩ		V_{OH}	4.85	4.95	–	
R_L = 10 kΩ		V_{OL}	–	0.05	0.15	
R_L = 600 Ω		V_{OH}	4.75	4.85	–	
R_L = 600 Ω		V_{OL}	–	0.15	0.25	
Common Mode Rejection (V_{in} = 0 to 5.0 V)	–	CMR	60	90	–	dB
Power Supply Rejection Ratio	–	PSRR	–	25	500	µV/V
V_{CC}/V_{EE} = 5.0 V/Gnd to 3.0 V/Gnd		PSR	66	92	–	dB
Output Short Circuit Current (Source and Sink)	–	I_{SC}	50	80	–	mA

DC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{Enable} = 5.0 V, T_A = 25°C, unless otherwise noted.)

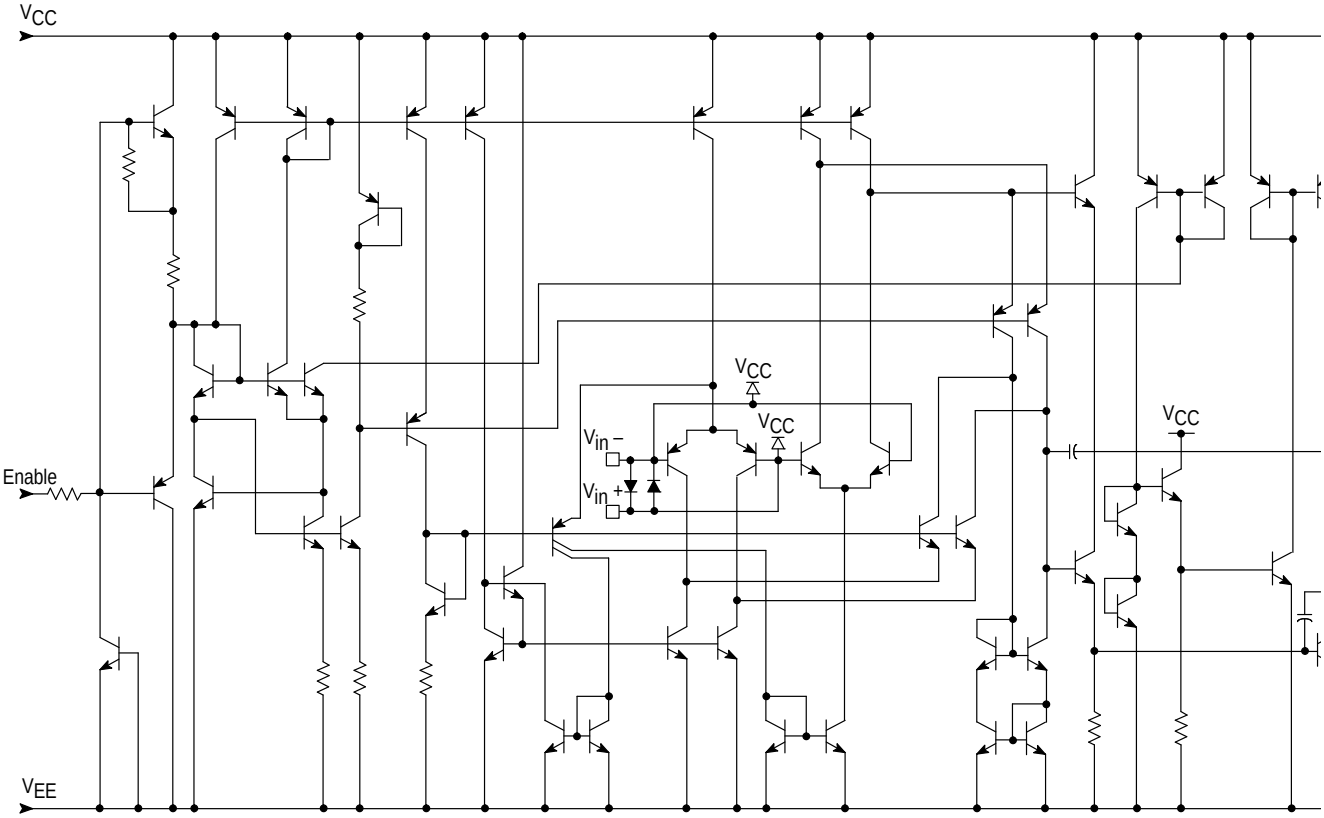
Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Power Supply Current (V_O = 2.5 V, T_A = –40° to +105°C, per Amplifier)	–	I_D				
MC33206: V_{Enable} = 5.0 Vdc			–	0.8	1.125	mA
V_{Enable} = Gnd (Standby)			–	0.5	6.0	μA
MC33207: V_{Enable} = 5.0 Vdc			–	1.5	2.25	mA
V_{Enable} = Gnd (Standby)			–	0.5	6.0	μA
Enable Input Voltage (per Amplifier)	–	V_{Enable}				V
Enabled – Amplifier “On”			–	V_{EE} + 1.8	–	
Disabled – Amplifier “Off” (Standby)			–	V_{EE} + 0.3	–	
Enable Input Current (Note 5) (per Amplifier)	–	I_{Enable}				μA
V_{Enable} = 12 V			–	2.5	–	
V_{Enable} = 5.0 V			–	2.2	–	
V_{Enable} = 1.8 V			–	0.8	–	
V_{Enable} = Gnd			–	0	–	

NOTE: 5. External control circuitry must provide for an initial turn–off transient of <10 μA.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{Enable} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_S = ±2.5 V, V_O = –2.0 to +2.0 V, R_L = 2.0 kΩ, A_V = 1.0)	–	SR	0.5	1.0	–	V/μs
Gain Bandwidth Product (f = 100 kHz)	–	GBW	–	2.2	–	MHz
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	–	ϕ_M	–	65	–	Deg
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	–	A_M	–	12	–	dB
Channel Separation (f = 1.0 Hz to 20 kHz, A_V = 100)	–	CS	–	90	–	dB
Power Bandwidth (V_O = 4.0 Vpp, R_L = 600 Ω, THD ≤ 1%)	–	BW_P	–	28	–	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 1.0 Vpp, A_V = 1.0)	–	THD				%
f = 1.0 kHz			–	0.002	–	
f = 10 kHz			–	0.008	–	
Open Loop Output Impedance (V_O = 0 V, f = 2.0 MHz, A_V = 10)	–	$\lvert Z_O \rvert$	–	100	–	Ω
Differential Input Resistance (V_{CM} = 0 V)	–	R_{in}	–	200	–	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	–	C_{in}	–	8.0	–	pF
Equivalent Input Noise Voltage (R_S = 100 Ω)	–	e_n				$\frac{nV}{\sqrt{Hz}}$
f = 10 Hz			–	25	–	
f = 1.0 kHz			–	20	–	
Equivalent Input Noise Current	–	i_n				$\frac{pA}{\sqrt{Hz}}$
f = 10 Hz			–	0.8	–	
f = 1.0 kHz			–	0.2	–	
Time Delay for Device to Turn On	–	t_{on}	–	10	–	μs
Time Delay for Device to Turn Off	–	t_{off}	–	2.0	–	μs

Figure 1. Circuit Schematic
(Each Amplifier)



This device contains 96 active transistors (each amplifier).

Figure 2. Maximum Power Dissipation versus Temperature

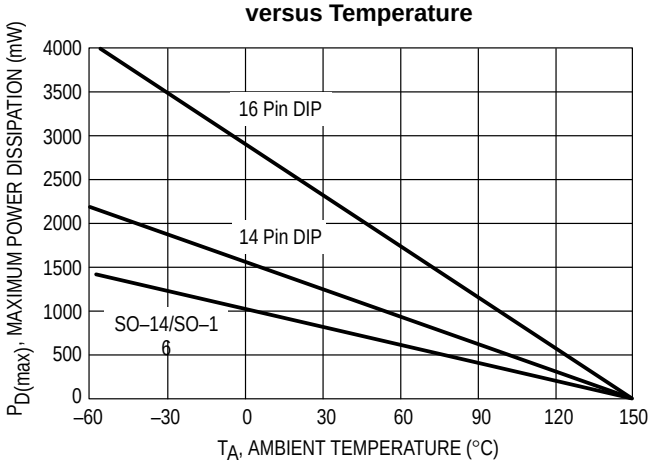


Figure 3. Input Offset Voltage Distribution

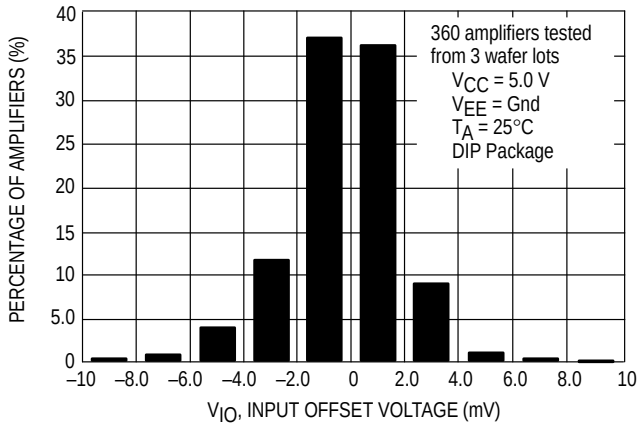


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

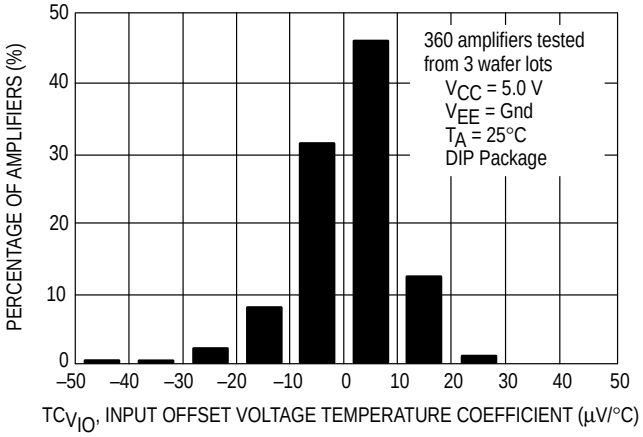


Figure 5. Input Bias Current versus Temperature

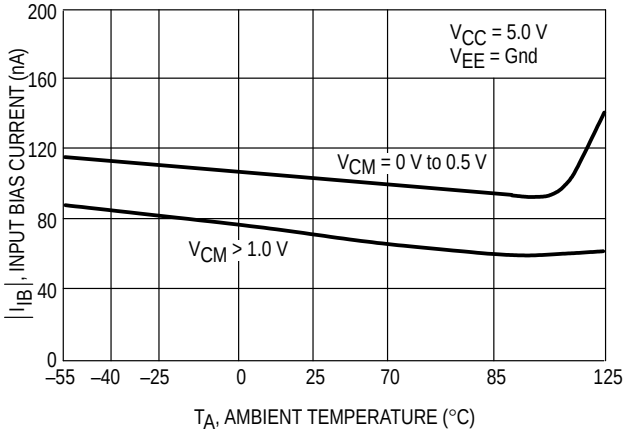


Figure 6. Input Bias Current versus Common Mode Voltage

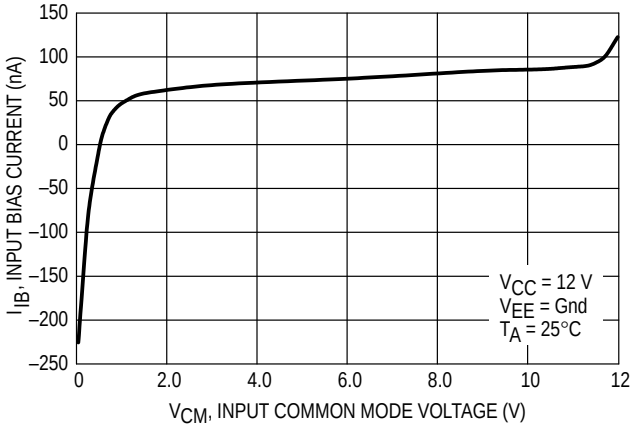


Figure 7. Open Loop Voltage Gain versus Temperature

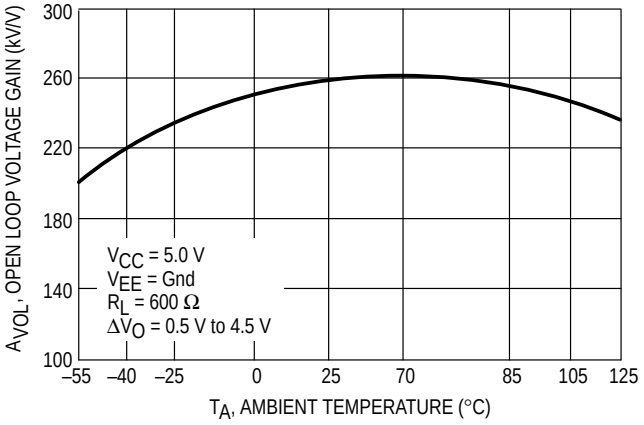


Figure 8. Output Voltage Swing versus Supply Voltage

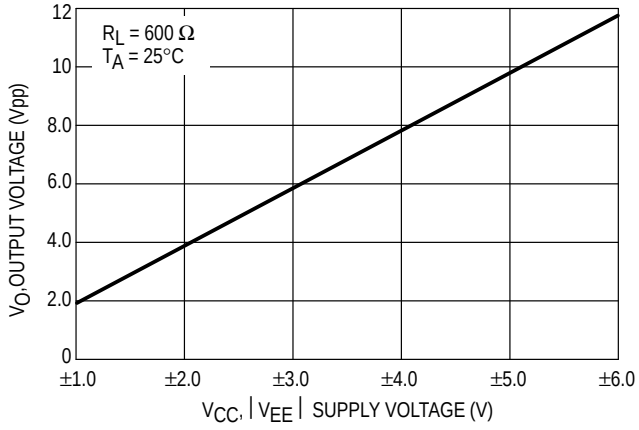


Figure 9. Output Saturation Voltage versus Load Current

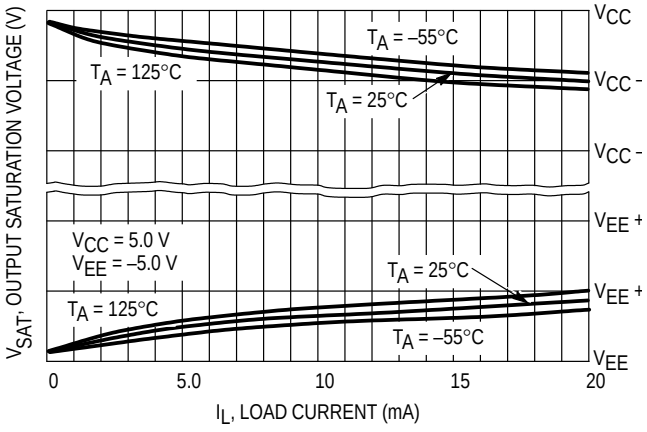


Figure 10. Output Voltage versus Frequency

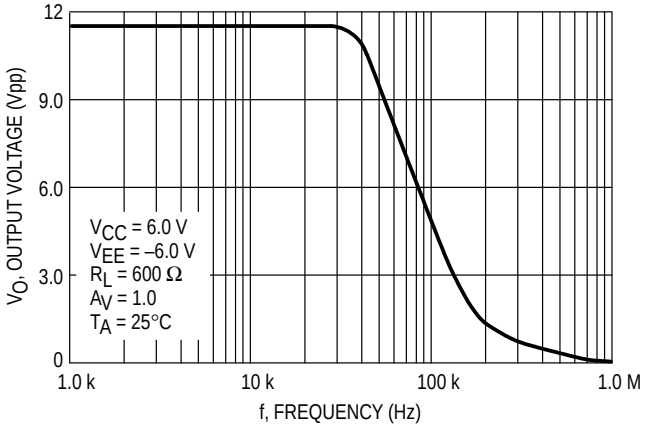


Figure 11. Common Mode Rejection versus Frequency

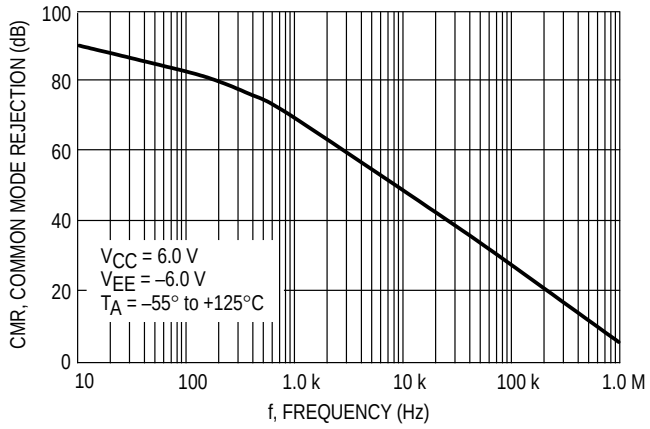


Figure 12. Power Supply Rejection versus Frequency

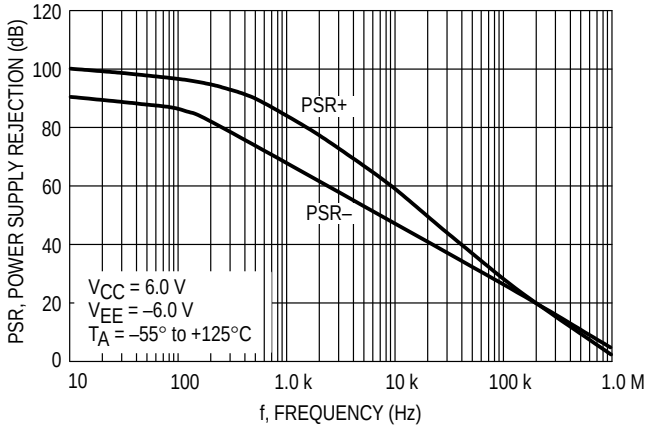


Figure 13. Output Short Circuit Current versus Output Voltage

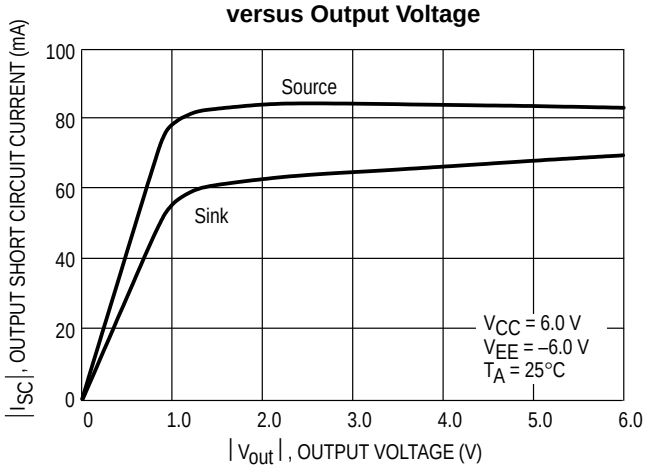


Figure 14. Output Short Circuit Current versus Temperature

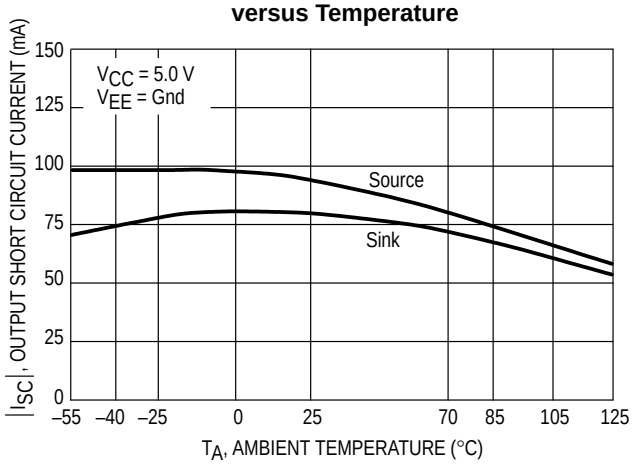


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

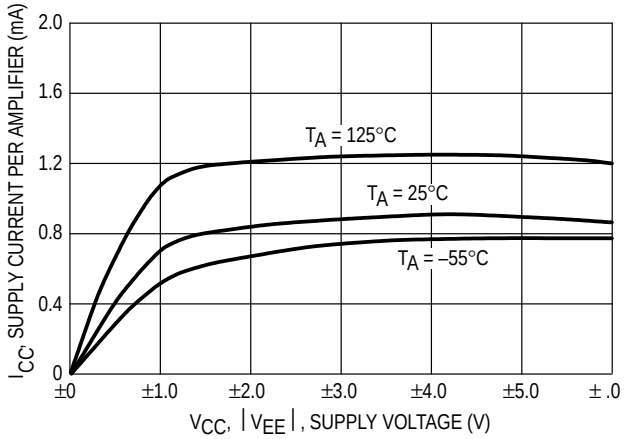


Figure 16. Slew Rate versus Temperature

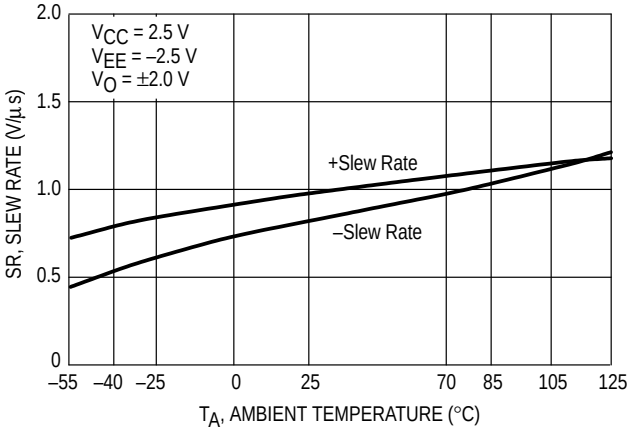


Figure 17. Gain Bandwidth Product versus Temperature

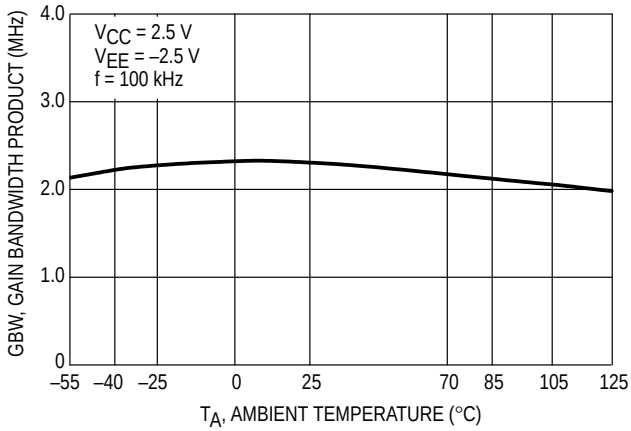


Figure 18. Voltage Gain and Phase versus Frequency

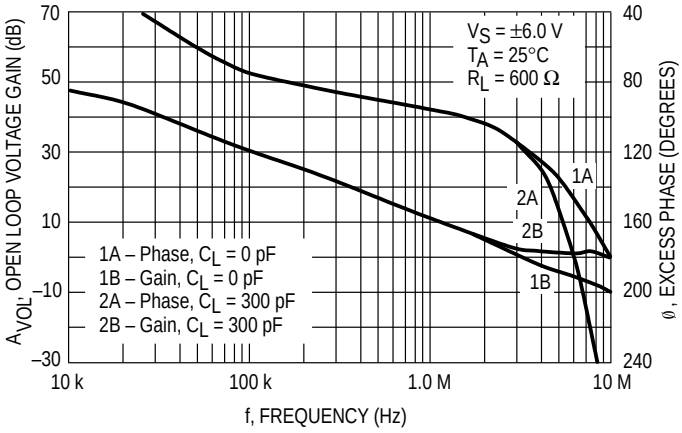


Figure 19. Voltage Gain and Phase versus Frequency

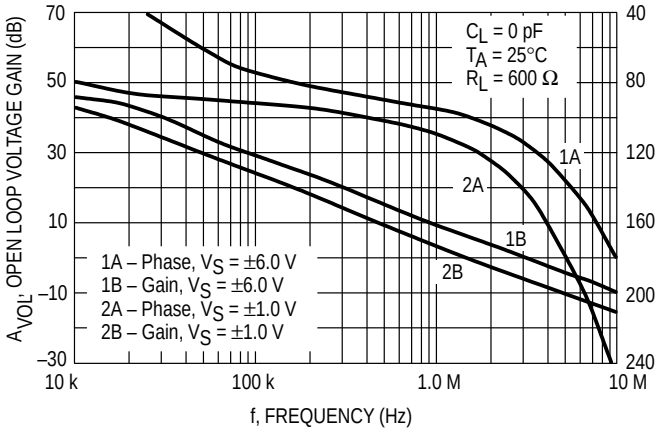


Figure 20. Gain and Phase Margin versus Temperature

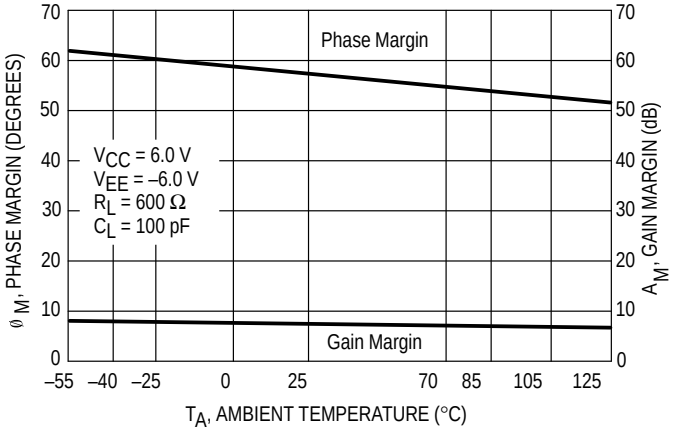


Figure 21. Gain and Phase Margin versus Differential Source Resistance

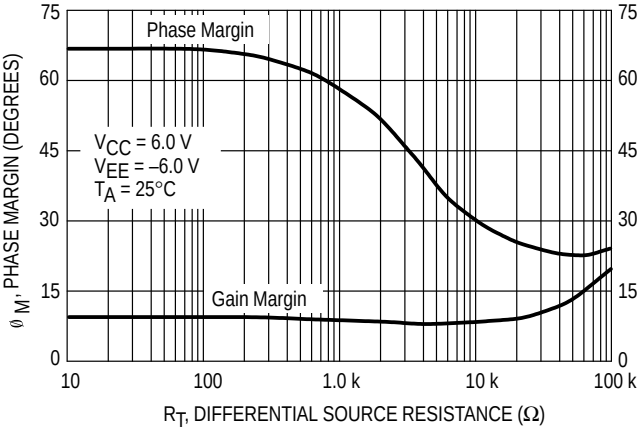


Figure 22. Gain and Phase Margin versus Capacitive Load

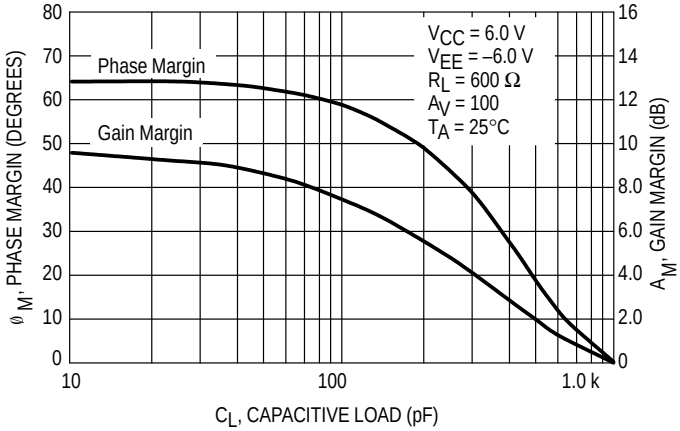


Figure 23. Output Voltage versus Load Resistance

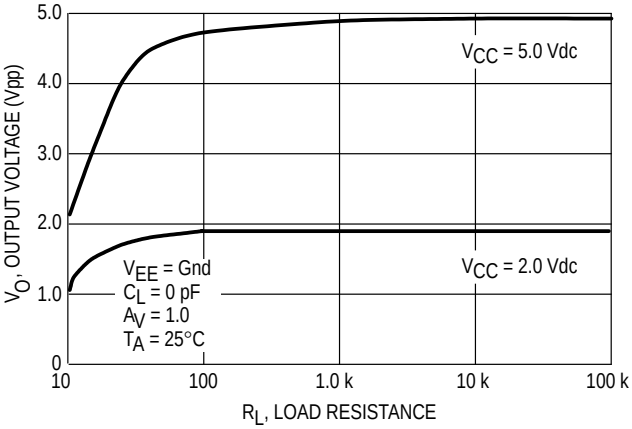


Figure 24. Channel Separation versus Frequency

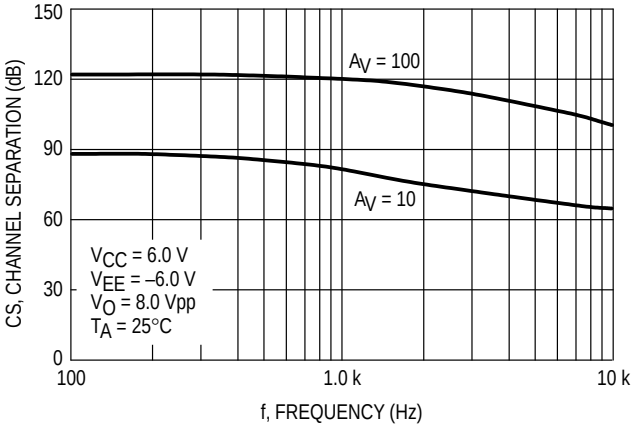


Figure 25. Total Harmonic Distortion versus Frequency

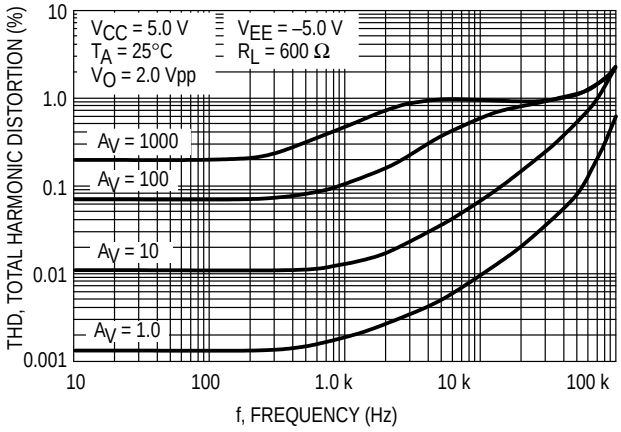
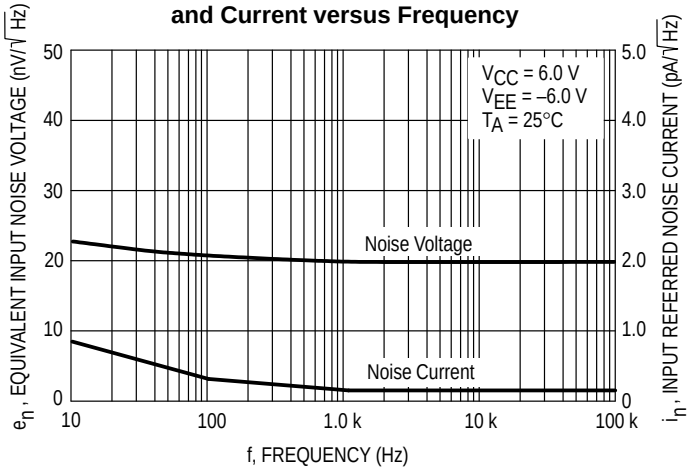


Figure 26. Equivalent Input Noise Voltage and Current versus Frequency



GENERAL INFORMATION

The MC33206/7 family of operational amplifiers are unique in their ability to swing rail–to–rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33206/7 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

CIRCUIT INFORMATION

Rail–to–rail performance is achieved at the input of the amplifiers by using parallel NPN–PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.

In addition to its rail–to–rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 Ω loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

Enable Function

The MC33206/07 enable pins allow the user to externally control the device. (Refer to the Pin Diagram on the first page of this data sheet for enable pin connections.) If the enable pins are pulled low (Gnd) each amplifier (MC33206) and amplifier pair (MC33207) will be disabled. When the enable pins are at a logic high ($V_{Enable} \geq V_{EE} = 1.8$ V) the amplifiers will turn “on”. Refer to the data sheet characteristics for the required levels needed to change logical state.

The time to change states (from device “on” to “off” and “off” to “on”) is defined as the time delay. The Circuit in Figure 27 is used to measure t_{on} and t_{off}. Typical t_{on} and t_{off} measurements are shown in Figures 28 and 29. When the device is turned off (V_{Enable} = Gnd) an internal regulator is shut off disabling the amplifier.

Figure 27. Test Circuit for t_{on} and t_{off}

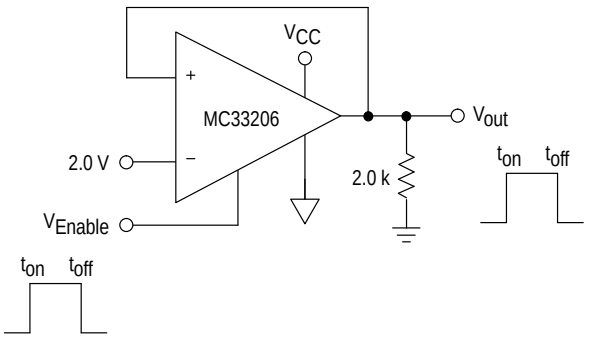
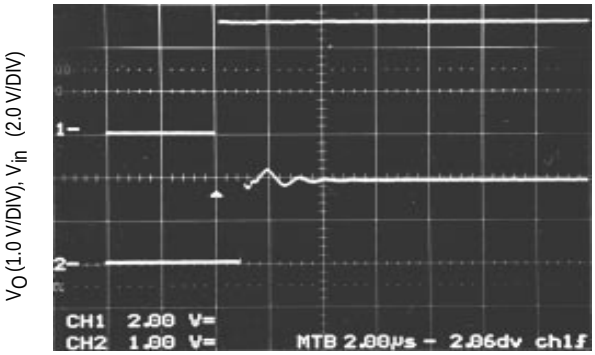
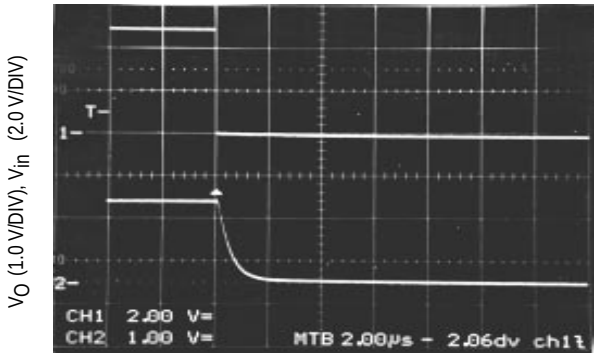


Figure 28. t_{on} Response



t_{on}, TIME (2.0 µs/DIV)

Figure 29. t_{off} Response



t_{off}, TIME (2.0 µs/DIV)

Low Voltage Operation

The MC33206/07 will operate at supply voltages down to 1.8 V and ground. Since this device is a rail–to–rail on both the input and output, one can be assured of continued operation in battery applications when battery voltages drop to low voltage levels. This is called End of Discharge (see Figure 30). Now, the user can select a minimum quantity of batteries best suited for the particular design depending on the type of battery chosen. This will minimize part count in many designs.

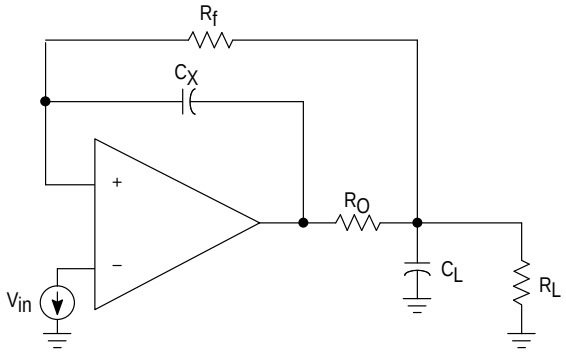
Figure 30. Typical Battery Characteristics

Type	Operating Voltage	End of Discharge
Alkaline	1.5 V	0.9 V
NiCd	1.2 V	1.0 V
NiMh	1.2 V	1.0 V
Silver Oxide	1.6 V	1.3 V
Lithium Ion	3.6 V	2.5 V

Compensating for Output Capacitance

The combination of device output impedance and increasing capacitive loading will cause phase delay (reducing the phase margin) in any amplifier (Figure 22). If the loading is excessive, the resulting response can be circuit oscillation. In other words, an amplifier can become unstable when the phase becomes greater than 180 degrees before the open loop gain drops to unity gain. Figures 18 and 19 show this situation as frequency increases for a given load. The MC33206/7 can typically drive up to 300 pF loads at unity gain without oscillating.

Figure 31. Capacitive Loads Compensation



There are several ways to compensate for this phenomena. Adding series resistance to the output is one way, but not an ideal solution. A dc voltage error will occur at the output. A better design solution to compensate for higher capacitive loads would be to use the circuit in Figure 31. This design helps to counteract the loss of phase margin by taking the high frequency output signal and feeding it back into the amplifier inverting input. This technique helps to overcome oscillation due to a highly capacitive load. Keep in mind that compensation will have the affect of lowering the Gain Bandwidth Product (GPW). The values of C_X and R0, are determined experimentally. Typical C_X and C_L will be the same value.

SPICE Model

If a SPICE Macromodel is desired for the MC33206/07, the user can define the characteristics from the following information. Obtain the SPICE Macromodel for the MC33204 Rail–to–Rail Operational Amplifier (device is the same as the MC33207). For the Enable feature of the MC33207, simulate it as a bipolar switch. The Macromodel does not include an input capacitance between the inverting and noninverting inputs. This capacitor is called C_{in}. Add 3.0 to 5.0 pF if stability analysis is required.

Figure 32. Noninverting Amplifier Slew Rate

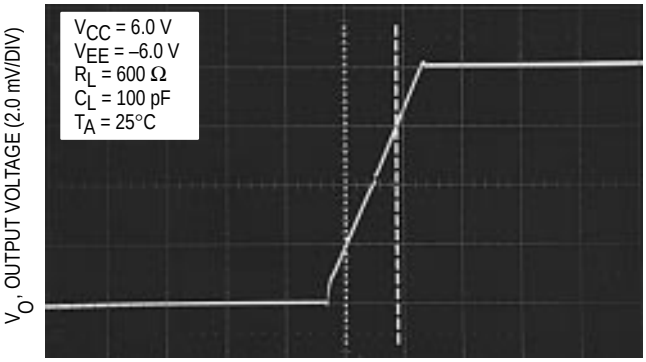


Figure 33. Small Signal Transient Response

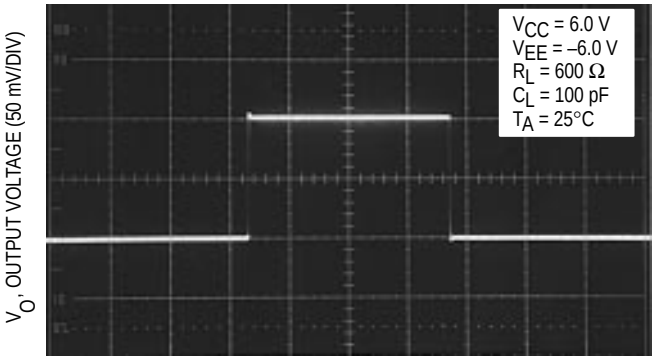
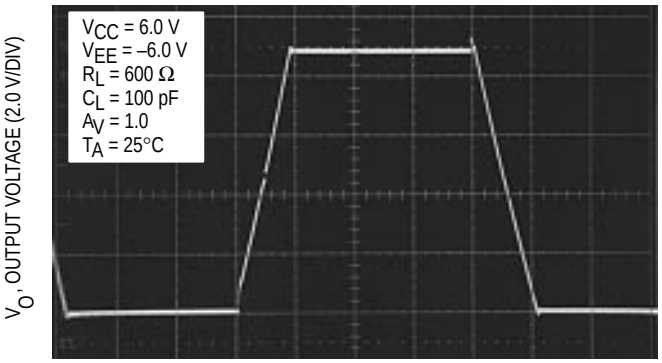
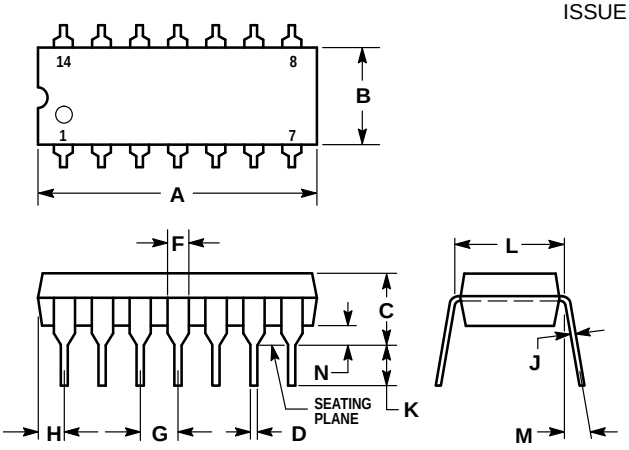


Figure 34. Large Signal Transient Response



OUTLINE DIMENSIONS

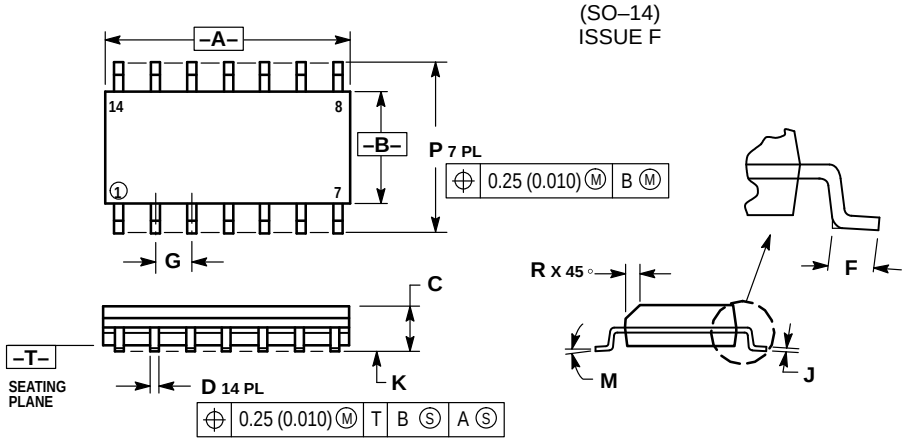
P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

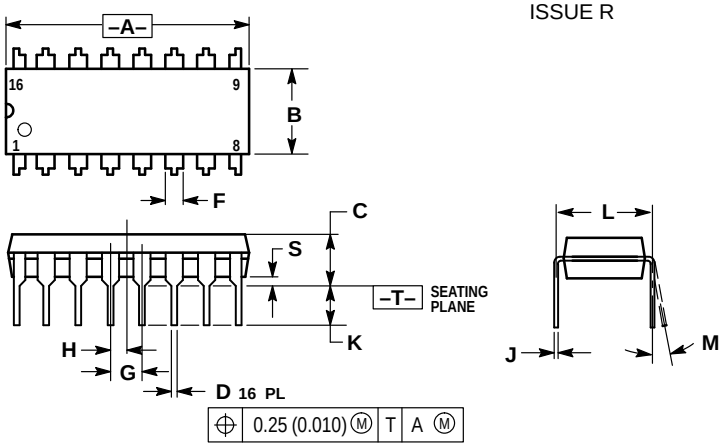
D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

P SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R

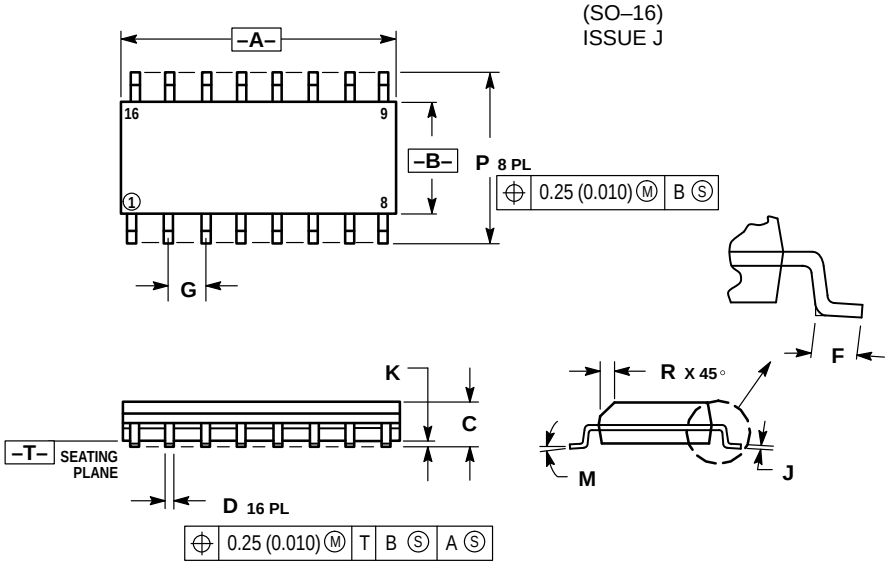


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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