

DATA SHEET

TDA8808T

TDA8808AT

Photo diode signal processor for
compact disc players

Product specification
File under Integrated Circuits, IC01

November 1987

Photo diode signal processor for compact disc players

TDA8808T
TDA8808AT

GENERAL DESCRIPTION

The TDA8808 is a bipolar integrated circuit designed for use in compact disc players with a single spot read-out system. It amplifies the photo-diode signals and processes the error signals for the focus- and radial control network.

Features

- Data amplifier with equalizer and AGC
- Offset-free pre-amplifier with AGC for the servo signals
- Trackloss and drop-out detection
- Start-up procedure for focus
- Normalizing focus error output signal to minimize radial error interference
- Laser supply amplifier and reference source
- Both TDA8808T and TDA8808AT versions suitable for car, portable and home applications
- Single and dual supply application
- Focus in-lock signal; ready signal output (RD).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	Supply voltage range		4,5	5,0	5,5	V
V_{ext}	External voltage range					
	TDA8808T		-5,5	-5,0	0	V
V_{ext}	TDA8808AT		V_P	10	12	V
I_Q	Quiescent supply current	$Si/\overline{RD} = 0\text{ V}$	7,5	10	12,5	mA
	HF input current					
$I_{HFIn(p-p)}$	(peak-to-peak value)	$f_{HFIn} = 100\text{ kHz}$	3	—	10	μA
	LF input current					
I_D	(for each diode input)		0	—	6	μA
I_{LO}	Laser supply output current	$Si/\overline{R7D} = \text{HIGH Z}$	-8	-4	-2	mA
	Operating ambient					
T_{amb}	temperature range		-30	—	+85	$^{\circ}\text{C}$

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A); SOT136-1; 1996 August 13.

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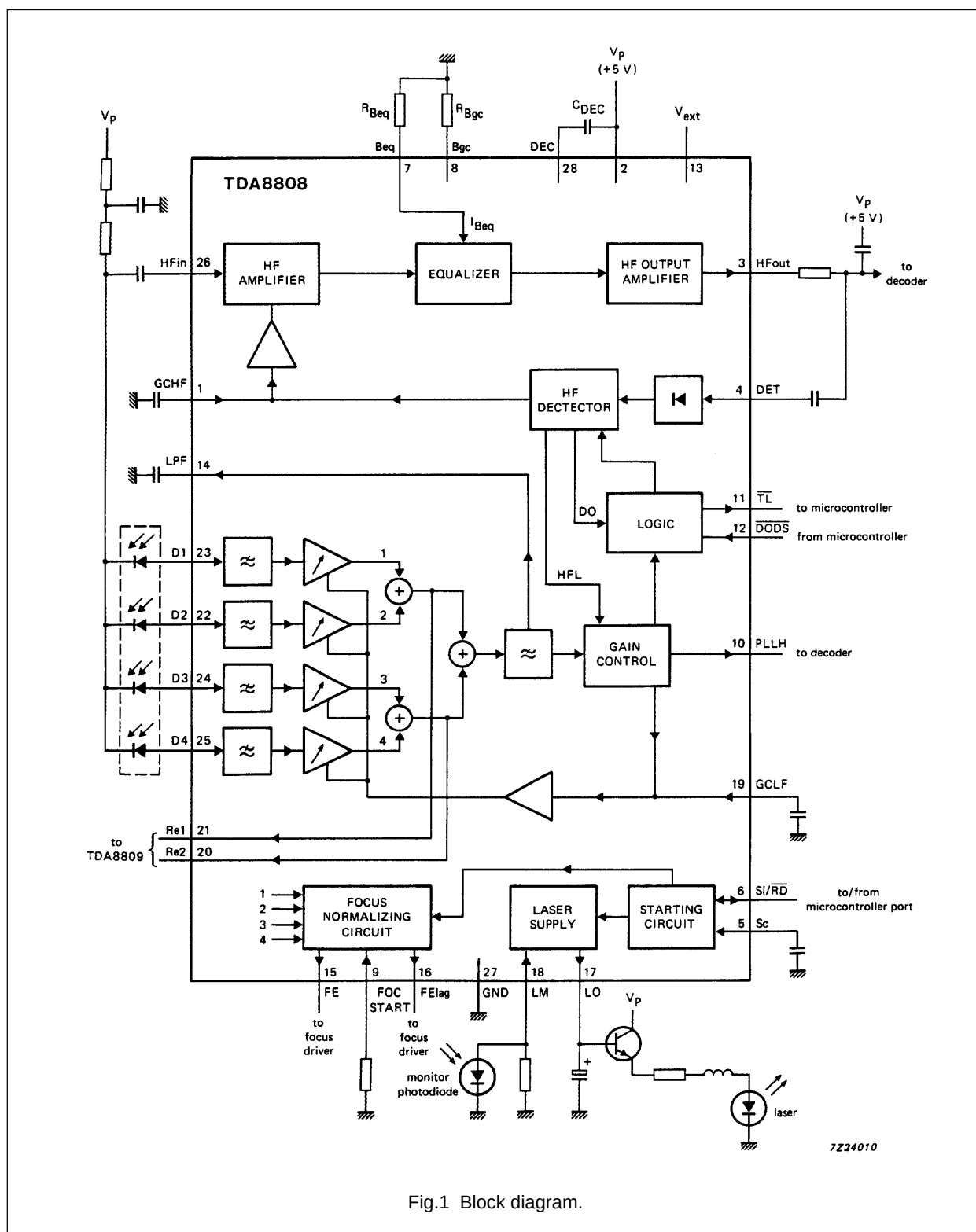


Fig.1 Block diagram.

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PINNING

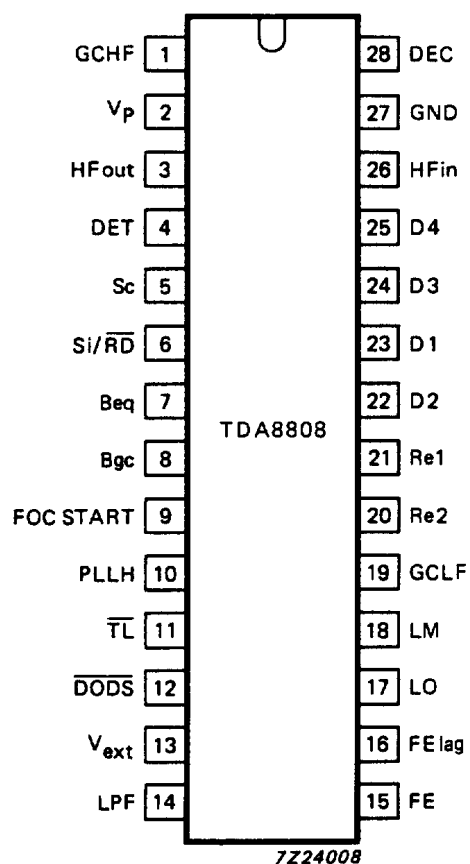


Fig.2 Pinning diagram.

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Pin functions

PIN	MNEMONIC	DESCRIPTION
1	GCHF	Gain control input of HF amplifier. Current output from HF amplitude detector
2	V _P	Positive supply voltage
3	HFout	HF amplifier and equalizer voltage output
4	DET	HF detector voltage input
5	Sc	Starting up capacitor input
6	Si/RD	On/off control (start input); ready signal output (starting up procedure successful)
7	Beq	Equalizer reference current input
8	Bgc	DC and LF gain control reference current input
9	FOC START	Focus normalizing circuit starting current
10	PLLH	PLL on hold output
11	TL	Track loss output
12	DODS	Drop out detector suppression input
13	V _{ext}	TDA8808T Negative supply connection for FE and FE _{lag} output stage; also substrate connection TDA8808AT Positive supply connection for FE and FE _{lag} output stage
14	LPF	Low pass filter for I _{ret} , used in track loss (TL) detector and LF gain control
15	FE	Current output of normalized, switched focus error signal
16	FE _{lag}	Current output of switched focus error signal, intended for lag network.
17	LO	Laser amplifier current output
18	LM	Laser monitor diode input
19	GCLF	Gain control input for AC and LF amplifiers. Current output from LF amplitude detector
20	Re2	Summation of amplified currents from D3 and D4
21	Re1	Summation of amplified currents from D1 and D2
23, 22	D1, D2	Current inputs to DC and LF photo diode amplifier
24, 25	D3, D4	Current inputs to DC and LF photo diode amplifier
26	HFin	Current input to HF amplifier
27	GND	Ground connection of device: also substrate connection for TDA8808AT
28	DEC	Decoupling input (internal bypass)

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
	Supply voltage ranges (see Fig.3)			
$V_P - V_{(ext)}$	TDA8808T pin 2 to pin 13	-0,3	13	V
$V_{GND} - V_{(ext)}$	pin 27 to pin 13	-0,3	13	V
	TDA8808AT			
$V_{ext} - V_{GND}$	pin 13 to 27	-0,3	13	V
$V_P - V_{GND}$	pin 2 to pin 27	-0,3	13	V
	Output voltage ranges			
V_O	except FE and FE_{lag}	0	V_P	V
V_O	FE and FE_{lag} (TDA8808T)	V_{ext}	V_P	V
V_O	FE and FE_{lag} (TDA8808AT)	V_{GND}	V_{ext}	V
V_O	LM (open loop)	V_{GND}	V_P	V
P_{tot}	Total power dissipation	see Fig.4		
T_{stg}	Storage temperature range	-55	+ 150	°C
T_{amb}	Operating ambient temperature range	-30	+ 85	°C
T_j	Operating junction temperature	-	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j-a}$ = 140 K/W

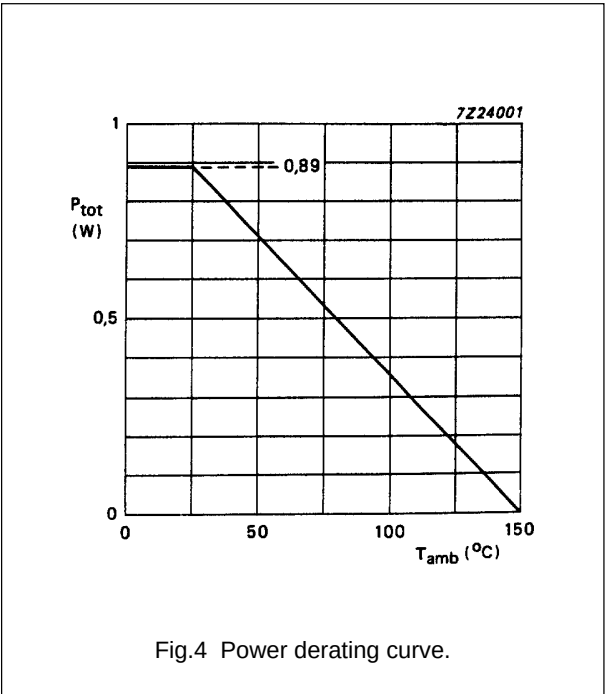
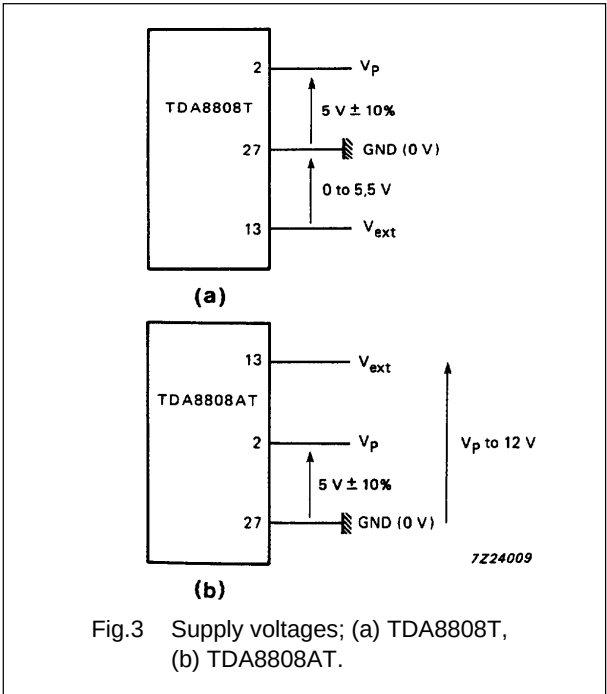


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CHARACTERISTICS

$V_P = +5\text{ V}$; $V_{GND} = 0\text{ V}$; $V_{ext} = -5\text{ V}$ (TDA8808T); $V_{ext} = +10\text{ V}$ (TDA8808AT); $V_{RE1} = V_{RE2} = 3,5\text{ V}$; $V_{FE} = V_{FElag} = 0\text{ V}$ (TDA8808T); $V_{FE} = V_{FElag} = 5\text{ V}$ (TDA8808AT); $R_{FOC\ START} = 3,3\text{ k}\Omega$; $I_{Beq} = I_{Bgc} = 50\text{ }\mu\text{A}$ (current sources); $T_{amb} = 25\text{ }^\circ\text{C}$; all voltages measured with respect to V_{GND} , unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	Supply voltage range		4,5	5,0	5,5	V
External voltage range						
V_{ext}	TDA8808T		-5,5	-5,0	0	V
V_{ext}	TDA8808AT		V_P	10	12	V
I_Q	Quiescent supply current	$V_{Si/RD} = 0\text{ V}$	7,5	10	12,5	mA
Reference input (Beq)						
V_{Beq}	Input voltage level		500	560	620	mV
I_{Beq}	Input current		—	-50	—	μA
Reference input (Bgc)						
V_{Bgc}	Input voltage level		1,15	1,25	1,35	V
I_{Bgc}	Input current		—	-50	—	μA
Decoupling input (DEC)						
V_{DEC}	Input voltage level		—	$V_P - 1,4$	—	V
$ Z_{DEC} $	Input impedance		—	2	—	k Ω
HF input (HFin)						
V_{HFin}	Input voltage level		—	1,4	—	V
HF input current						
$I_{HFin(p-p)}$	(peak-to-peak value)	$f_{HFin} = 100\text{ kHz}$	3	—	10	μA
$ Z_{HFin} $	Input impedance		0,5	1	2	k Ω
HF part						
DC characteristics						
Gain (G1) = $\frac{\Delta V_{HFout}}{\Delta I_{HFin}}$						
$I_{HFin} = \pm 1\text{ }\mu\text{A}$						
G1(max)	Maximum gain	$V_{GCHF} = 4\text{ V}$	390	480	570	mV/ μA
G1(min)	Minimum gain	$V_{GCHF} = 1,5\text{ V}$	-5	0	5	mV/ μA
AC characteristics						
G2	Gain (G2) = $20 \log \frac{V_{O1}}{V_{O2}}$	note 1	2	3,5	5	dB
G3	Gain (G3) = $20 \log \frac{V_{O1}}{V_{O2}}$	note 2	4	5,5	7	dB
ϕ	Phase of input/output signal at 1 MHz	note 3	—	$\pi/2$	—	rad.

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
τ_{300}	Group delay at $f_{HFin} = 300 \text{ kHz} + \Delta f$	note 3	—	290	—	ns
$\Delta\tau$	Flatness between 0,1 and 1 MHz	note 3	*	9	*	ns
	HF output (HFout)					
V_{HFout}	Output voltage at $I_{HFin} = 0$	$V_{GCHF} = 4 \text{ V}$	1,5	2,4	3,3	V
$V_{O1(p-p)}$	Output voltage (peak-to-peak value) at $I_{HFin(p-p)} = 7 \mu\text{A}$	note 4	1	1,20	—	V
$V_{O(p-p)}$	at $I_{HFin(p-p)} = 4 \text{ to } 10 \mu\text{A}$	note 5	−20%	M_1	+20%	V
$ Z_{HFout} $	Output impedance		—	60	—	Ω
	HF detector input (DET)	see Fig.5				
V_{DET0}	DC voltage level	$I_{DET} = 0$	—	2,2	—	V
V_{refp}	Positive reference voltage V_{DET} to V_{DET0}		−10%	540	+10%	mV
V_{refn}	Negative reference voltage V_{DET} to V_{DET0}		−5%	$-V_{refp}$	+5%	mV
$ Z_{DET} $	Input impedance		—	9	—	k Ω
	Gain control (GCHF)					
V_{GCHF}	Input voltage for: minimum HF gain		—	1,8	—	V
V_{GCHF}	maximum HF gain		—	3,4	—	V
$ Z_{GCHF} $	Input impedance at $V_{GCHF} = 1,5 \text{ to } 4 \text{ V}$		—	25	—	M Ω
	Output current (see Fig.5)					
I_{GCHF}	$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS} = \text{LOW}$	90	100	110	μA
I_{GCHF}	$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS} = \text{HIGH}$	86	96	106	μA
I_{GCHF}	$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETP1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS} = \text{LOW}$	−0,65	−0,35	−0,2	μA
I_{GCHF}	$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETP1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS} = \text{HIGH}$	−5,0	−4,4	−3,8	μA
I_{GCHF}	$V_{DETn1} < \Delta V_{DET} < V_{DETP1}$	$\overline{DODS} = X^{**}$	−0,65	−0,35	−0,2	μA
	V_{DETP1}/V_{refp} ; V_{DETn1}/V_{refn}		10	12,5	15	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{PLLHL}	PLLH output (pin 10) Output voltage LOW I _{PLLH} = 400 µA (sink current)	V _{GCLF} = 3,5 V	–	–	0,4	V
	Output voltage HIGH I _{PLLH} = –50 µA (source current)		2,4	–	–	V
I _{PLLH}	Output sink current		0,5	1,5	–	mA
I _{PLLH}	Output source current		–	–100	–50	µA
I _{DT1}	Threshold total LF current V _{DETP2} /V _{refp} ; V _{DETn2} /V _{refn}		–	2,0	–	µA
			57,5	62,5	67,5	%
LF photo diode inputs (pins 22 to 25) (values given for each input)						
V _D	DC voltage level		–	1,2	–	V
I _D	Input current range		0	–	6	µA
Z _D	Input impedance at 1 MHz	I _D = 1 µA	–	10	–	kΩ
LF gain Maximum DC gain						
for: $A_1 = \left \frac{I_{Re1}}{I_{D1} + I_{D2}} \right $; I _{D3} = I _{D4} = 0		V _{GCLF} = 3,5 V				
A ₁₁	at I _{D1} = 0 µA; I _{D2} = 1 µA		S ₁ –10%	S ₁	S ₁	
A ₁₂	at I _{D1} = 1 µA; I _{D2} = 0 µA		S ₁ or 55	S ₁	S ₁	
for: $A_2 = \left \frac{I_{Re2}}{I_{D3} + I_{D4}} \right $; I _{D1} = I _{D2} = 0		V _{GCLF} = 3,5 V				
A ₂₁	at I _{D3} = 0 µA; I _{D4} = 1 µA		S ₁ –10%	S ₁	S ₁	
A ₂₂	at I _{D3} = 1 µA; I _{D4} = 0 µA		S ₁ or 55	S ₁	S ₁	
S ₁ mean value of A ₁₁ , A ₁₂ , A ₂₁ , A ₂₂			55	64	84	
Minimum DC gain						
for: $A_3 = \left \frac{I_{Re1}}{I_{D1} + I_{D2}} \right $; I _{D3} = I _{D4} = 0		V _{GCLF} = 0,8 V				
A ₃₁	at I _{D1} = 0 µA; I _{D2} = 1 µA		S ₂ –1	S ₂	S ₂ +1	
A ₃₂	at I _{D1} = 1 µA; I _{D2} = 0 µA		S ₂ –1	S ₂	S ₂ +1	
for: $A_4 = \left \frac{I_{Re2}}{I_{D3} + I_{D4}} \right $; I _{D1} = I _{D2} = 0		V _{GCLF} = 0,8 V				
A ₄₁	at I _{D3} = 0 µA; I _{D4} = 1 µA		S ₂ –1	S ₂	S ₂ +1	

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
A ₄₂	at I _{D3} = 1 µA; I _{D4} = 0 µA S ₂ mean value of A ₃₁ , A ₃₂ , A ₄₁ , A ₄₂ AC gain for: G ₄ = 20 log P ₁ ; I _{D3} = I _{D4} = 0		S ₂ -1	S ₂	S ₂ +1	
			-0,1	0,7	3	
G ₄	at I _{D1} = 0; I _{D2(p-p)} = 1 µA + 2 µADC	note 6	-4,5	-3	-1,5	dB
G ₄	at I _{D1(p-p)} = 1 µA + 2 µADC; I _{D2} = 0	note 6	-4,5	-3	-1,5	dB
	G ₅ = 20 log P ₂ ; I _{D1} = I _{D2} = 0					
G ₅	at I _{D3} = 0; I _{D4(p-p)} = 1 µA + 2 µADC	note 7	-4,5	-3	-1,5	dB
G ₅	at I _{D3(p-p)} = 1 µA + 2 µADC; I _{D4} = 0	note 7	-4,5	-3	-1,5	dB
	Gain control (GCLF)					
	Input voltage for:					
V _{GCLF}	minimum LF gain		—	1	—	V
V _{GCLF}	maximum LF gain		—	2,8	—	V
Z _{GCLF}	Input impedance		—	25	—	MΩ
	Threshold total LF current	I _{DT3}	—	1,6	—	mA
	Output current (see Fig.7)					
I _{GCLF}	ΔV _{DET} < V _{DETn2} or ΔV _{DET} > V _{DETP2}	I _{DT} < I _{DT3}	—	-0,6	± 10	µA
				I _{Bgc}		
I _{GCLF}		I _{DT} > I _{DT3} ; note 8	S ₆ -10	S ₆	S ₆ +10	µA
I _{GCLF}	V _{DETn2} < ΔV _{DET} < V _{DETP2}		—	-0,2	± 2	µA
				I _{Bgc}		
	Re1, Re2 outputs (pin 21, pin 20)					
	Output current	V _{GCLF} = 3,5 V				
I _{Re1}	at I _{D1} = I _{D2} = 1 µA; I _{D3} = I _{D4} = 0		110	128	168	mA
I _{Re1}	at I _{D1} = I _{D2} = I _{D3} = I _{D4} = 0		—	0	—	mA
I _{Re2}	at I _{D1} = I _{D2} = 0; I _{D3} = I _{D4} = 1 µA		110	128	168	mA
I _{Re2}	at I _{D1} = I _{D2} = I _{D3} = I _{D4} = 0		—	0	—	mA
	Output voltage					
V _{Re1}	pin 21		1	—	V _P	V
V _{Re2}	pin 20		1	—	V _P	V
	Output impedance					
Z _{Re1}	pin 21		—	1	—	MΩ
Z _{Re2}	pin 20		—	1	—	MΩ
	Reference current (I_{ret})					
I _{ret}	I _{ret} = I _{Re1} = I _{Re2}	note	200	220	240	µA
	LPF output (pin 14)					
V _{LPF}	DC voltage level	note 9	V _P -2,1	V _P -1,7	V _P -1,4	V

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$ Z_{LPF} $	Input impedance		—	3	—	k Ω
	FOC START input (pin 9)					
I_{ST}	Start current (ST) for FE ($-I_{FOC\ START} = I_{ST}$)	$S_i/\overline{RD} = \text{HIGH } Z$	75	150	500	μA
I_{ST}		$S_i/\overline{RD} = \text{LOW}$	—	0	—	μA
V_{ST}	Start voltage (ST) for FE ($V_{FOC\ START} = V_{ST}$)	$S_i/\overline{RD} = \text{HIGH } Z$	430	530	630	mV
V_{ST}		$S_i/\overline{RD} = \text{LOW}$	—20	0	20	mV
	FElag output (pin 16)	see Fig.8				
V_{FElag}	Output voltage					
	TDA8808T		$V_{ext}+1,5$	—	$V_P-1,5$	V
V_{FElag}	TDA8808AT		+1,5	—	$V_{ext}-1,5$	V
$ Z_{FElag} $	Output impedance		—	8	—	M Ω
	Output current	$S_i/\overline{RD} = \text{HIGH } Z$; $V_{GCLF} = 3,5 \text{ V}$				
$I_{FElag}=I_O$	$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1 \mu A$	$V_{Sc} = V_P$	—10	0	+10	μA
I_{FElag}	$I_{D2} = I_{D3} = 1 \mu A$; $I_{D1} = I_{D4} = 2 \mu A$	$V_{Sc} = V_P$	—10%	$-2S_1$ + I_O	+10%	μA
I_{FElag}	$I_{D2} = I_{D3} = 2 \mu A$; $I_{D1} = I_{D4} = 1 \mu A$	$V_{Sc} = V_P$	—10%	$-2S_1$ + I_O	+10%	μA
I_{FElag}	$I_{D2} = I_{D3} = 2 \mu A$; $I_{D1} = I_{D4} = 1 \mu A$	$V_{Sc} = 1,5 \text{ V}$	—5	0	+5	μA
I_{FElag}	$I_{D2} = I_{D3} = 1 \mu A$; $I_{D1} = I_{D4} = 2 \mu A$	$V_{Sc} = 1,5 \text{ V}$	—5	0	+5	μA
	FE output (pin 15)	see Fig.8				
V_{FE}	Output voltage					
	TDA8808T		$V_{ext}+1,5$	—	$V_P-1,5$	V
V_{FE}	TDA8808AT		+1,5	—	$V_{ext}-1,5$	V
$ Z_{FE} $	Output impedance		—	8	—	M Ω
	Output current	note 10				
I_{FE}	$I_{D1} = I_{D4} = 2 \mu A$; $I_{D2} = I_{D3} = 1 \mu A$	$V_{Sc} = 0$	—10%	$-2S_1-134-I_{ST}$	+10%	μA
I_{FE}	$I_{D1} = I_{D4} = 1 \mu A$; $I_{D2} = I_{D3} = 2 \mu A$	$V_{Sc} = 0$	—10%	$-4S_1-67-I_{ST}$	+10%	μA
I_{FE}	$I_{D1} = I_{D4} = 2 \mu A$; $I_{D2} = I_{D3} = 1 \mu A$	$V_{Sc} = 1,25 \text{ V}$	—10%	$-2S_1-134+I_{ST}$	+20%	μA
I_{FE}	$I_{D1} = I_{D4} = 1 \mu A$; $I_{D2} = I_{D3} = 2 \mu A$	$V_{Sc} = 1,25 \text{ V}$	—10%	$-4S_1-67+I_{ST}$	+20%	μA

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I_{FE}	$I_{D1} = I_{D4} = 2 \mu A$; $I_{D2} = I_{D3} = 1 \mu A$	$V_{Sc} = 1,75 V$	-20%	$-2S_1+67+I_{ST}$	+10%	μA
I_{FE}	$I_{D1} = I_{D4} = 1 \mu A$; $I_{D2} = I_{D3} = 2 \mu A$	$V_{Sc} = 1,75 V$	-10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{FE} = S_6$	$I_{D1} = I_{D4} = 2 \mu A$; $I_{D2} = I_{D3} = 1 \mu A$	$V_{Sc} = V_P$	-20%	67	+20%	μA
I_{FE}	$I_{D1} = I_{D4} = 1 \mu A$; $I_{D2} = I_{D3} = 2 \mu A$	$V_{Sc} = V_P$	-15%	$-S_6$	+15%	μA
I_{FE}	$I_{D1} = I_{D2} =$ $I_{D3} = I_{D4} = 1 \mu A$	$V_{Sc} = V_P$	-10	0	+10	μA
I_{FE}	$I_{D1} = I_{D2} =$ $I_{D3} = I_{D4} = 0$	$V_{Sc} = V_P$	-5	0	+5	μA
	DODS logic input (pin 12)					
	Switching levels					
$\overline{VDODS}$	input voltage LOW		-	-	+0,8	V
$\overline{VDODS}$	input voltage HIGH		+2	-	-	V
$\overline{IDODS}$	Input source current		-35	-25	-15	μA
	Starting input (S_c)					
	see Fig.9					
V_{Sc}	Output voltage	$S_i/\overline{RD} = \text{LOW}$	-	0	-	V
V_{Sc}	Output voltage	$S_1/\overline{RD} = \text{HIGH Z}$	-	-	$V_P-0,5$	V
$ Z_{Sc} $	Output impedance		-	*	-	M Ω
	Output source current	$S_i/\overline{RD} = \text{HIGH Z};$				
I_{Sc}		$V_{Sc} = 1,5 V$	-1,2	-1	-0,8	μA
I_{Sc}	Output sink current	$S_i/\overline{RD} = \text{LOW}$	0,5	1,2	2,0	mA
	$S_i/\overline{RD}$ logic input/output					
	(pin 20)					
	Voltage 'forced LOW'					
	see Fig.9					
$V_{S_i/\overline{RD}}$		$I_{S_i/\overline{RD}} = 400 \mu A$; $V_{Sc} = 2,5 V$; $V_{GCLF} < 2,8 V$	-	0,15	0,4	V
	Switching levels					
$V_{S_i/\overline{RD}}$	input voltage LOW		-	-	+0,8	V
$V_{S_i/\overline{RD}}$	input voltage HIGH Z	$I_{S_i/\overline{RD}} = -5 \mu A$	2,4	2,8	-	V
$I_{S_i/\overline{RD}}$	Input source current LOW		-35	-25	-15	μA
	$\overline{TL}$ logic output (pin 11)					
	see Fig.6					
$V_{\overline{TL}}$	Output voltage level LOW	$I_{\overline{TL}} = 400 \mu A$; (sink current)	-	0,15	0,4	V
$V_{\overline{TL}}$	Output voltage level HIGH	$I_{\overline{TL}} = -50 \mu A$; (source current)	2,4	-	-	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Threshold total LF current	I_{DT2}	—	3,9	—	μA
	Output voltage	DODS = HIGH ($\geq 2,4 \text{ V}$)	—	—	—	—
$V_{\overline{\text{TL}}}$	$\Delta V_{\text{DET}} < V_{\text{DETn2}}$ or $\Delta V_{\text{DET}} > V_{\text{DETP2}}$	I_{DT} don't care	2,4	—	—	V
$V_{\overline{\text{TL}}}$	$V_{\text{DETn1}} < \Delta V_{\text{DET}} < V_{\text{DETP1}}$	I_{DT} don't care	2,4	—	—	V
$V_{\overline{\text{TL}}}$	$V_{\text{DETn2}} < V_{\text{DET}} < V_{\text{DETn1}}$ or $V_{\text{DETP1}} < \Delta V_{\text{DET}} < V_{\text{DETP2}}$	$I_{\text{DT}} < I_{\text{DT2}}$	2,4	—	—	V
$V_{\overline{\text{TL}}}$	$V_{\text{DETn2}} < V_{\text{DET}} < V_{\text{DETn1}}$ or $V_{\text{DETP1}} < V_{\text{DET}} < V_{\text{DETP2}}$	$I_{\text{DT}} > I_{\text{DT2}}$	—	0,15	0,4	V
	Output voltage	DODS = LOW ($\leq 0,8 \text{ V}$)	—	—	—	—
$V_{\overline{\text{TL}}}$	$\Delta V_{\text{DET}} < V_{\text{DETn2}}$ or $\Delta V_{\text{DET}} > V_{\text{DETP2}}$	I_{DT} don't care	2,4	—	—	V
$V_{\overline{\text{TL}}}$	$V_{\text{DETn2}} < \Delta V_{\text{DET}} < V_{\text{DETP2}}$	$I_{\text{DT}} < I_{\text{DT2}}$	2,4	—	—	V
$V_{\overline{\text{TL}}}$	$V_{\text{DETn2}} < \Delta V_{\text{DET}} < V_{\text{DETP2}}$	$I_{\text{DT}} > I_{\text{DT2}}$	—	0,15	0,4	V
$I_{\overline{\text{TL}}}$	Output sink current	$V_{\overline{\text{TL}}} = \text{LOW}$	1	2,2	—	mA
$I_{\overline{\text{TL}}}$	Output source current	$V_{\overline{\text{TL}}} = \text{HIGH}$	—	−100	−50	μA
τ_1	Delay times (see Fig.10)		7	8,5	10	μs
τ_2		see Fig.6	$\tau_1 - 15\%$ or 6,5	—	$\tau_1 + 5\%$ or 10	μs
τ_3			7	8,5	10	μs
τ_4			$\tau_3 - 10\%$ or 7	—	$\tau_3 + 10\%$ or 10	μs
	LO output (pin 17)					
V_{LO}	Output voltage		—	—	$V_p - 0,5$	V
$ Z_{\text{LO}} $	Output impedance		—	95	—	k Ω
I_{LO}	Output leakage current	$S/\overline{\text{RD}} = \text{LOW}$	−10	−0,1	0	μA
I_{LO}	Maximum output current	$S/\overline{\text{RD}} = \text{HIGH Z}$	−8	−4	−2	mA
	LM input (pin 18)					
V_{LM}	Input voltage	closed loop	185	205	225	mV
I_{LM}	Input bias current		−2	—	—	μA
	Laser supply					
	Transconductance					
G_{LDC}	For DC (note 11)	$S/\overline{\text{RD}} = \text{HIGH Z}$	—	0,5	—	A/V
G_{LDC}		$S/\overline{\text{RD}} = \text{LOW}$	—	0	—	A/V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
τ_{LO}	For AC (note 12) delay time		—	*	—	ns

* Value to be fixed.

** X = don't care.

Notes to the characteristics

- Voltage output signal V_{O1} measured at $f_{HFin} = 700$ kHz; $I_{HFin(p-p)} = 7$ μ A; $V_{GCHF} = 2,4$ V.
Voltage output signal V_{O2} measured at $f_{HFin} = 100$ kHz; $I_{HFin(p-p)} = 7$ μ A; $V_{GCHF} = 2,4$ V.
- Voltage output signal V_{O1} measured at $f_{HFin} = 1$ MHz; $I_{HFin(p-p)} = 7$ μ A; $V_{GCHF} = 2,4$ V.
Voltage output signal V_{O2} measured at $f_{HFin} = 100$ kHz; $I_{HFin(p-p)} = 7$ μ A; $V_{GCHF} = 2,4$ V.
- Phase of input/output signal, group delay and flatness measured at $I_{HFin(p-p)} = 1$ μ A; $V_{GCHF} = 4$ V.

$$\text{Group delay } \tau = \frac{d\phi}{d\omega}; \Delta f \approx 50 \text{ kHz.}$$

Flatness: $\Delta\tau = \tau_{\max} - \tau_{\min}$.

- HF part output voltage for closed loop conditions; $f_{HFin} = 500$ kHz.
- HF part output voltage for closed loop conditions; $f_{HFin} = 0,1$ to 1 MHz.
 M_1 is the measured value of V_{O1} .

$$6. \quad P_1 \text{ is the measured value of } \frac{I_{Re1}(1)}{I_{D1}(1) + I_{D2}(1)} \cdot \frac{I_{D1}(2) + I_{D2}(2)}{I_{Re1}(2)}$$

Where: (1) are the current levels at $f_i = 25$ kHz.

(2) are the current levels at $f_i = 1$ kHz.

Measurement taken at $V_{GCLF} = 3,5$ V.

$$7. \quad P_2 \text{ is the measured value of } \frac{I_{Re2}(1)}{I_{D3}(1) + I_{D4}(1)} \cdot \frac{I_{D3}(2) + I_{D4}(2)}{I_{Re2}(2)}$$

Where: (1) are the current levels at $f_i = 25$ kHz.

(2) are the current levels at $f_i = 1$ kHz.

Measurement taken at $V_{GCLF} = 3,5$ V.

$$8. \quad S_6 \text{ is the measured value of } S_1 \cdot \frac{I_{DT}}{4} - 1, 1 \quad I_{BgC}$$

Measurement taken at $V_{GCLF} = 3,5$ V.

- LF part reference current I_{ref} and low-pass filter output voltage for closed loop conditions.
Measurement taken at $I_{DT} > I_{DT3}$; $\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETP2}$.

$$10. \quad \text{FE output current measured at } V_{GCLF} = 3, 5 \text{ V and } Si/\overline{RD} = \text{HIGH } Z; I_{ST} = \frac{V_{FOC \text{ START}}}{R_{FOC \text{ START}}}$$

- Laser supply transconductance for DC

$$G_{LDC} = \frac{\Delta I_{LO}}{\Delta V_{LM}} (0 < -I_{LO} < 2 \text{ mA})$$

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12. Laser supply transconductance for AC

$$G_{LAC} = G_{LO} \cdot \frac{1}{1 + S \cdot \tau_{LO}}$$

Where: S is the laplace operator in the frequency domain.

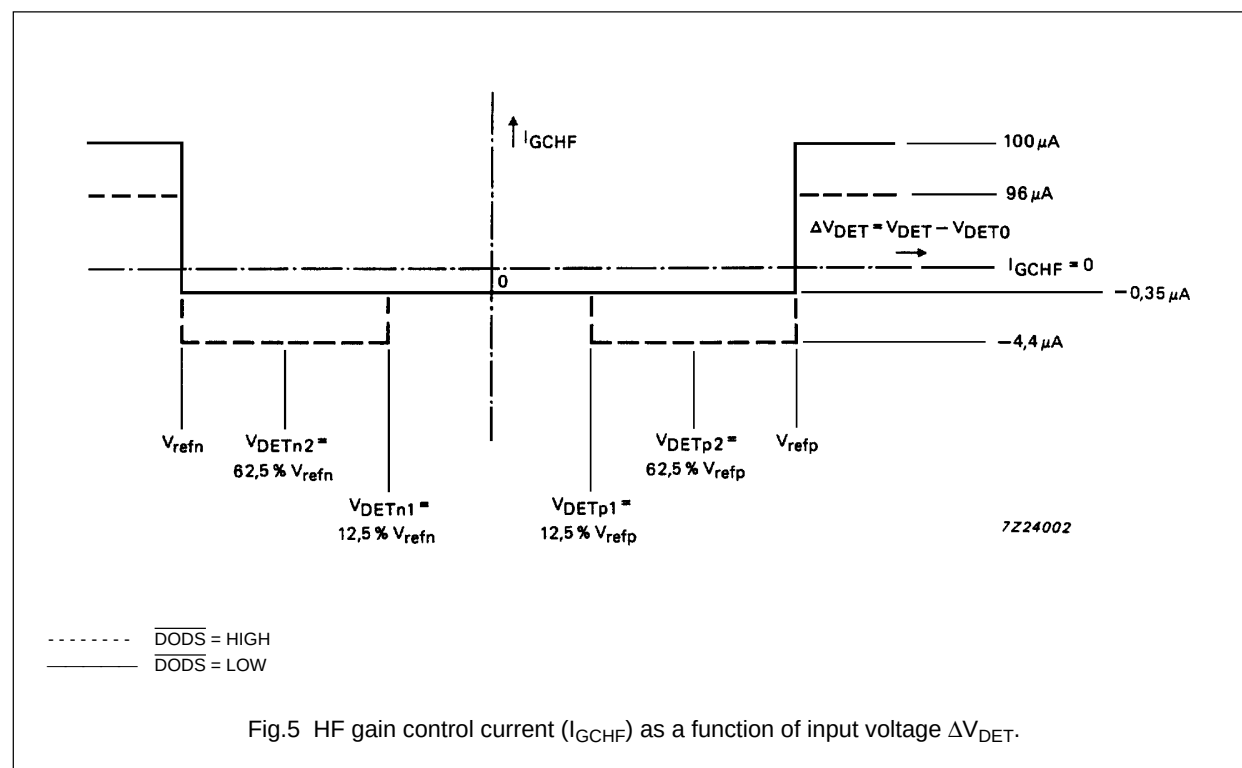


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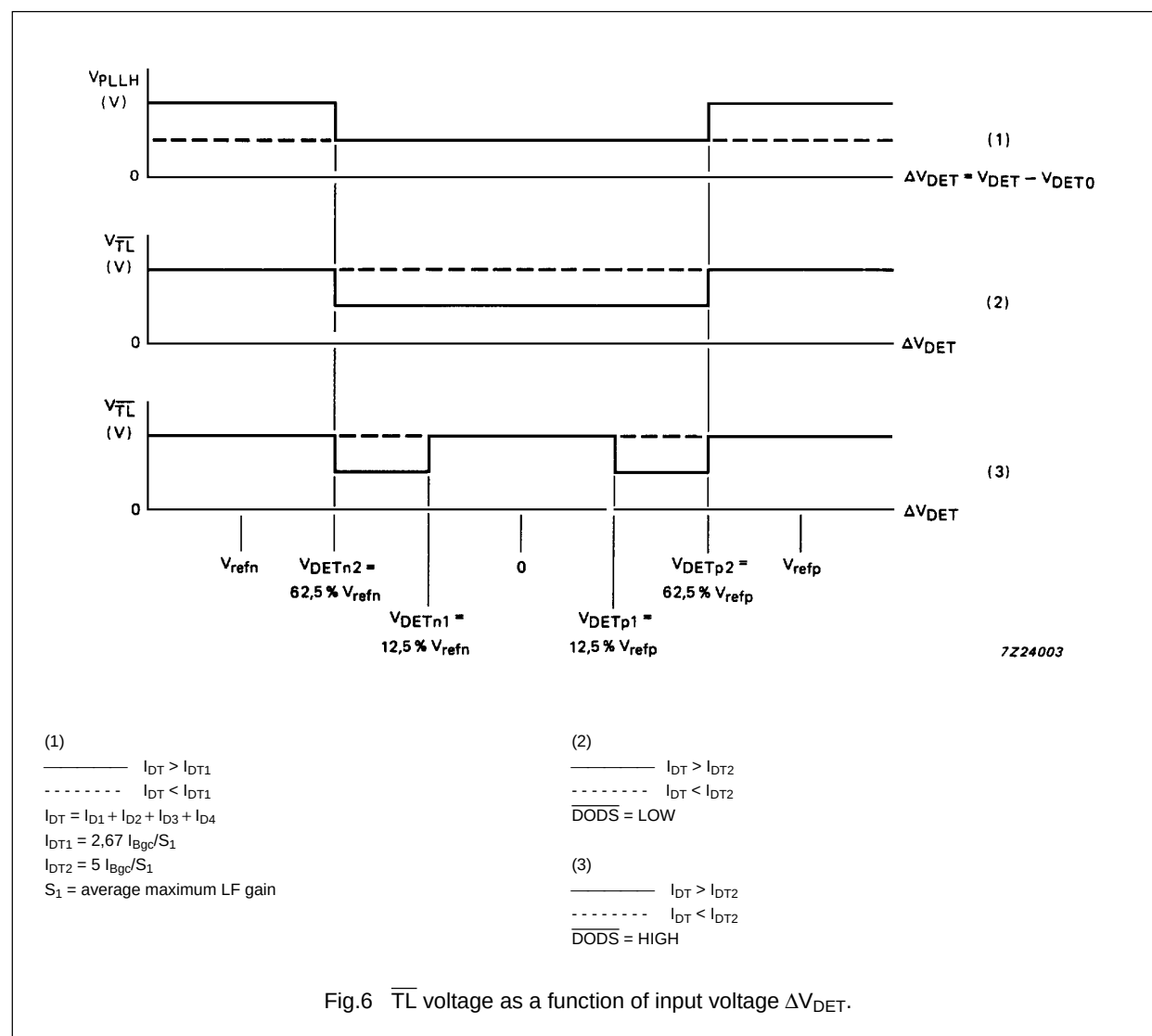


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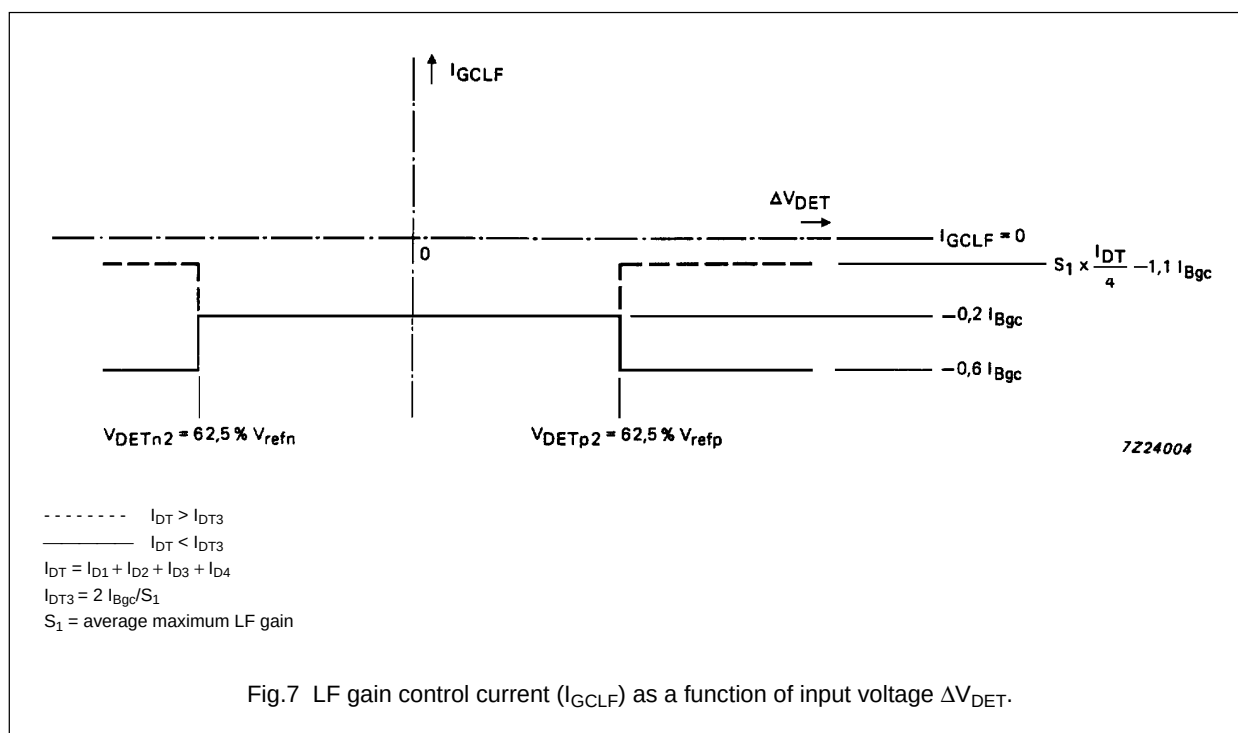


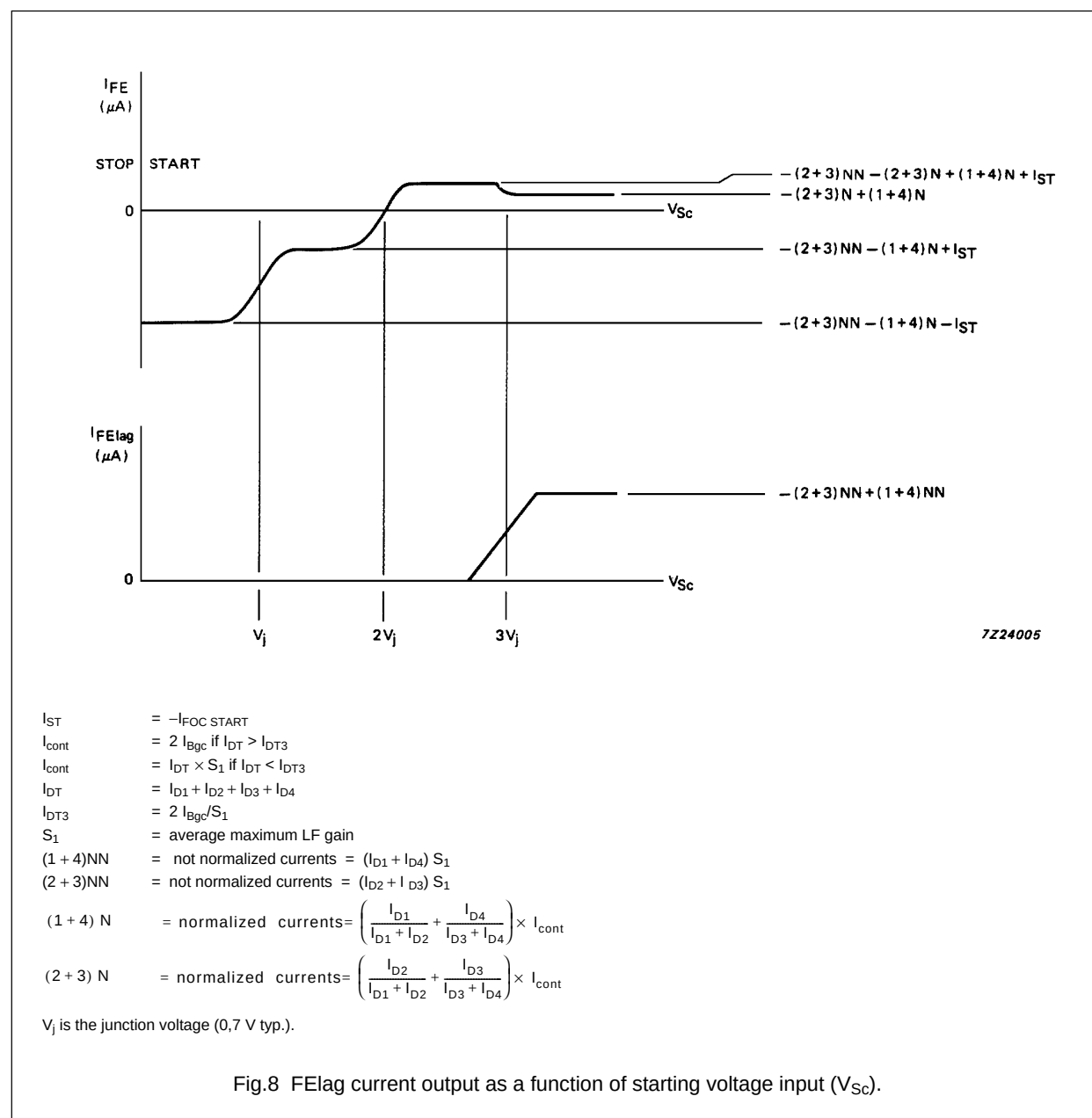
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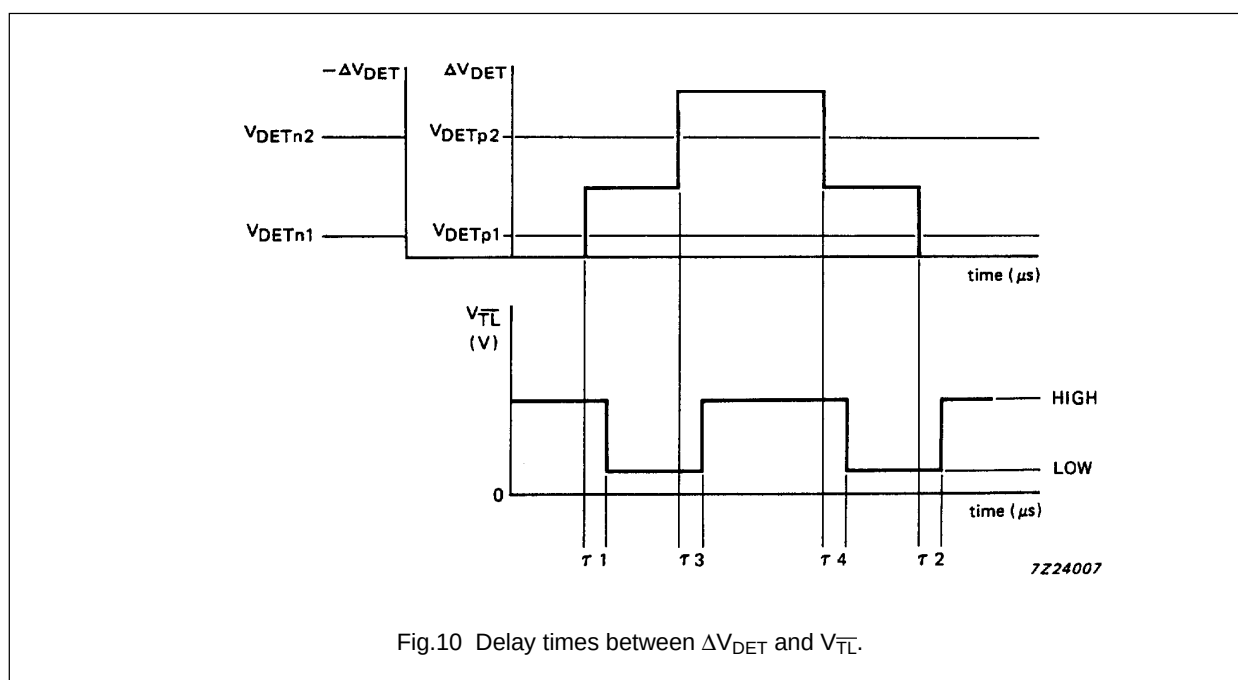
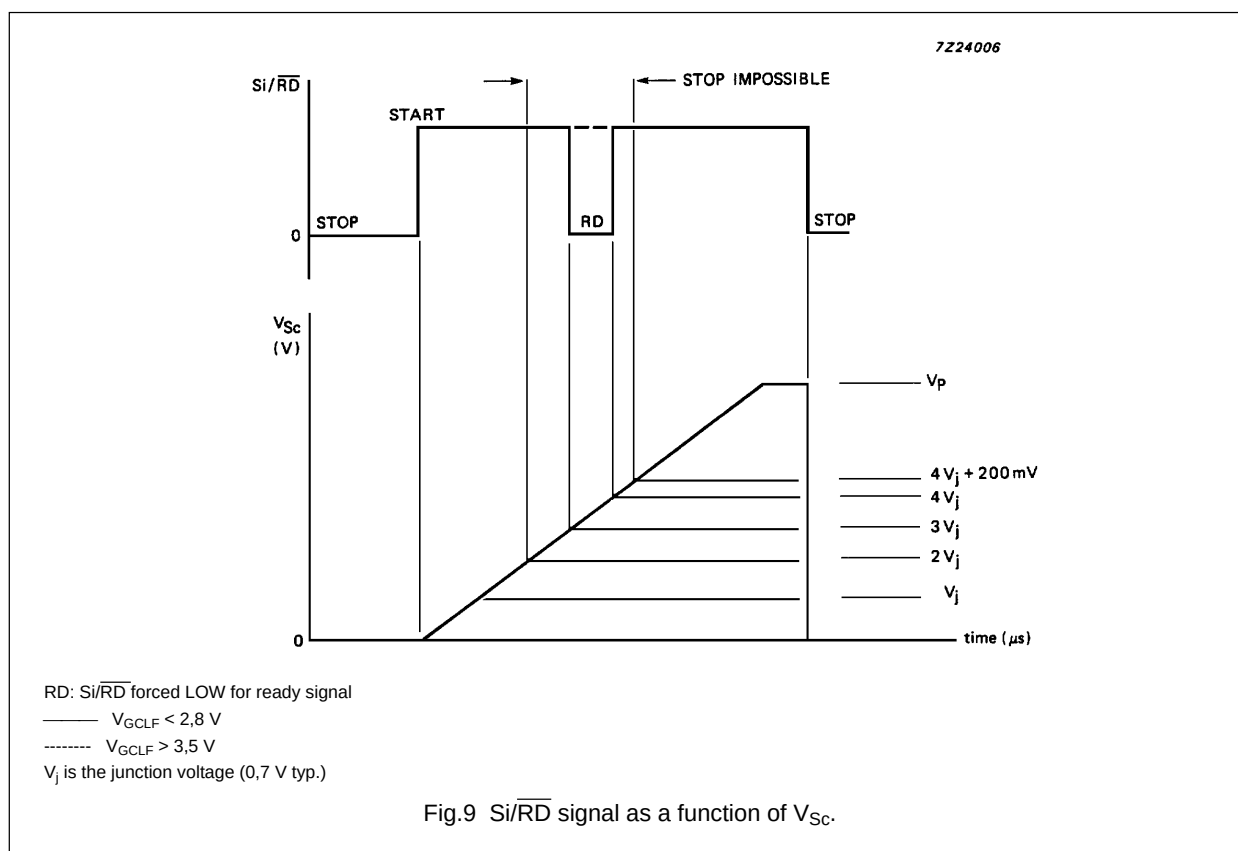


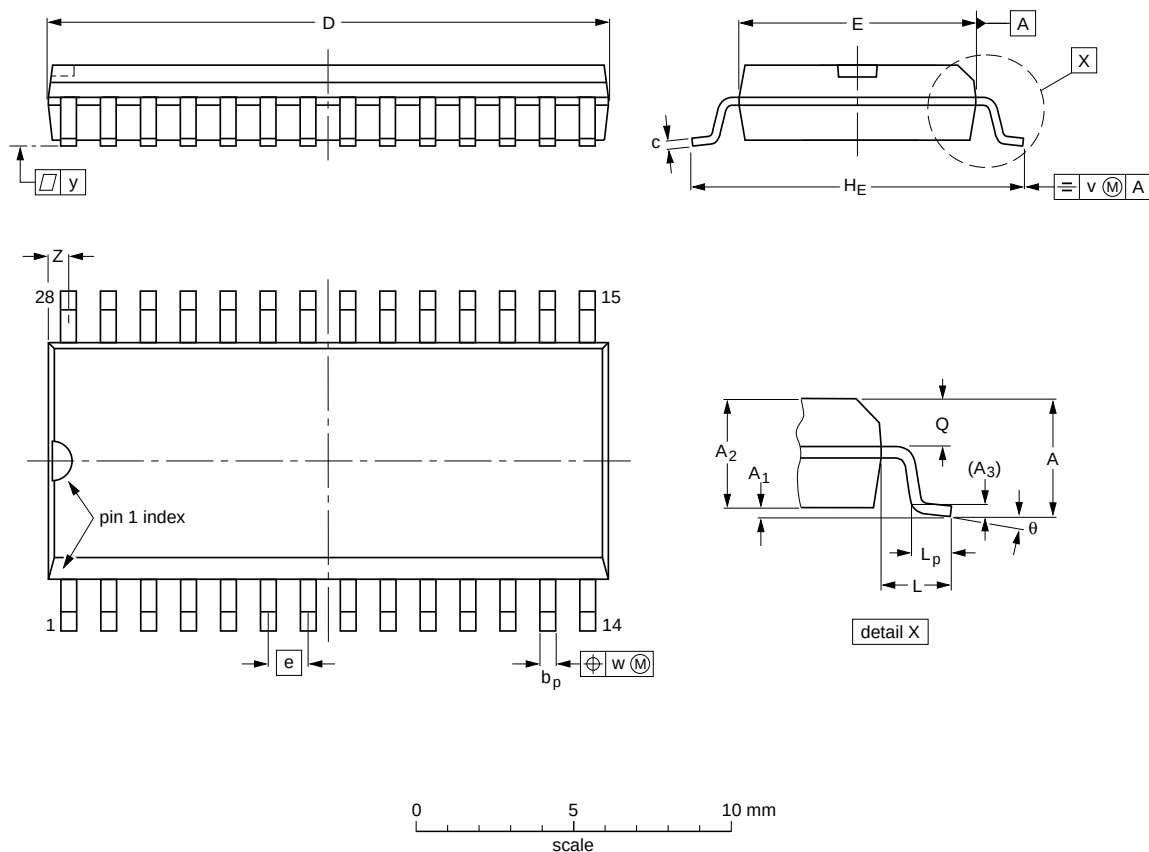
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PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm

SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				91-08-13 95-01-24

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.