DATA SHEET

TDA8754
Triple high speed ADC for LCD drive

Objective specification
File under Integrated Circuits, IC02

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Philips
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Triple high speed ADC for LCD drive TDA8754

FEATURES

- Triple 8-bit Analog-to-Digital Converter (ADC)
- Sampling rate up to 170 MHz
- IC controllable via a serial interface, which can be either I^{2}C-bus or 3-wire, selected via a TTL input pin
- IC analog input 0.5 to 1.1 V (peak-to-peak value) to have full-scale ADC input
- Clamps for programming a clamp level through a clamping code between −63 and +64 by steps of 1 LSB
- Controllable gain stages: gain controlled independently on the 3 channels via the serial interface to have a full-scale resolution to 1%
- Low gain variation at different temperatures
- Analog bandwidth of 400 MHz
- Controllable PLL via the serial interface generates the ADC clock. It can be locked on line frequencies from 15 kHz up to 280 kHz.
- Integrated PLL divider
- Integrated clamp pulse and H and V LCD control pulses generation (independently adjustable in position and duration). Also a data enable signal can be generated, independently adjustable in position and duration with respect to HSYNC.
- The pixel clock is available at half the clock frequency
- Programmable phase clock adjustment cells
- Internal voltage regulators
- TTL compatible digital inputs
- 3.3 V CMOS compatible digital outputs
- Outputs: one port output up to 140 MHz or 2-port demultiplexed outputs on the full speed range. Operating mode selectable through the serial interface.
- Chip enable: high-impedance ADC output
- Power-down mode.

GENERAL DESCRIPTION

The TDA8754 is a triple 8-bit ADC with controllable gain and clamps for the digitizing of large bandwidth R, G, B signals. Clamp level, gain, and all the other settings are controlled via a serial interface (either I^{2}C-bus or 3-wire, selected through a logic input). The gain is optimized for stability versus temperature variations.

The IC also includes a PLL that generates the ADC clock which can be locked to the horizontal line frequency. The PLL jitter is minimized for high resolution PC graphics applications. An external clock can also be used to clock the ADC.

The clamp pulse is generated on-chip, it can be adjusted in position (with respect to HSYNC) and duration through the serial interface.

The horizontal and vertical control pulses for the LCD can be adjusted in duration through the serial interface. Also a data enable signal can be generated, independently adjustable in position (with respect to HSYNC) and duration through the serial interface.

Outputs: one port output up to 140 MHz or demultiplexed 2-port outputs on the full speed range. Operating mode selectable through the serial interface.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8754H	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage for R, G, B channels		4.75	5.0	5.25	V
V_{DD}	logic supply voltage for I^2C-bus and 3-wire interface		3.0	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
$V_{CC(O)}$	output stages supply voltage for R, G, B channels		3.0	3.3	3.6	V
$V_{CCA(PLL)}$	analog PLL supply voltage		4.75	5.0	5.25	V
$V_{CC(O)(PLL)}$	output PLL supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current for R, G, B channels		–	tbf	–	mA
I_{DD}	logic supply current for I^2C-bus and 3-wire interface		–	tbf	–	mA
I_{CCD}	digital supply current		–	tbf	–	mA
$I_{CC(O)}$	output stages supply current for R, G, B channels		–	tbf	–	mA
$I_{CCA(PLL)}$	analog PLL supply current		–	tbf	–	mA
$I_{CC(O)(PLL)}$	output PLL supply current		–	tbf	–	mA
INL	DC integral non-linearity		–	±1	±1.5	LSB
DNL	DC differential non-linearity		–	±0.5	±0.8	LSB
ΔG_{amp}	gain stability versus temperature	V_{ref} = 2.5 V with 100 ppm/K variation	–	–	200	ppm/K
t_{set}	setting time of the block ADC + AGC	input signal setting time <1 ns; setting to 1%; f_i = 85 MHz	–	2.5	3.5	ns
$f_{clk(max)}$	maximum conversion rate		170	–	–	MHz
f_{ref}	PLL reference clock frequency		15	–	120	kHz
f_{PLL}	output clock frequency		12	–	170	MHz
$j_{PLL(rms)}$	maximum PLL phase jitter (RMS value)		–	0.2	–	ns
D/D_{PLL}	PLL divider ratio		512	–	4095	
P_{tot}	total power consumption	f_{clk} = 170 MHz; ramp input	–	tbf	1.2	W

BLOCK DIAGRAM

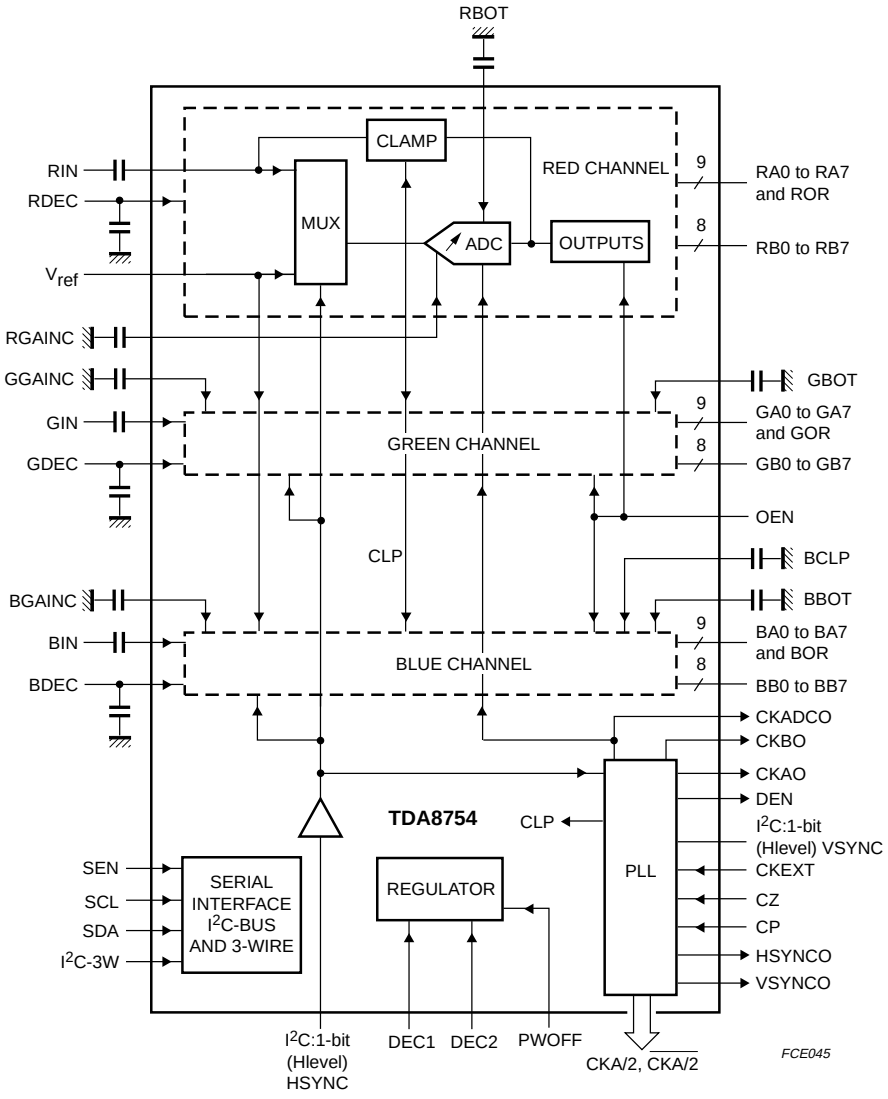
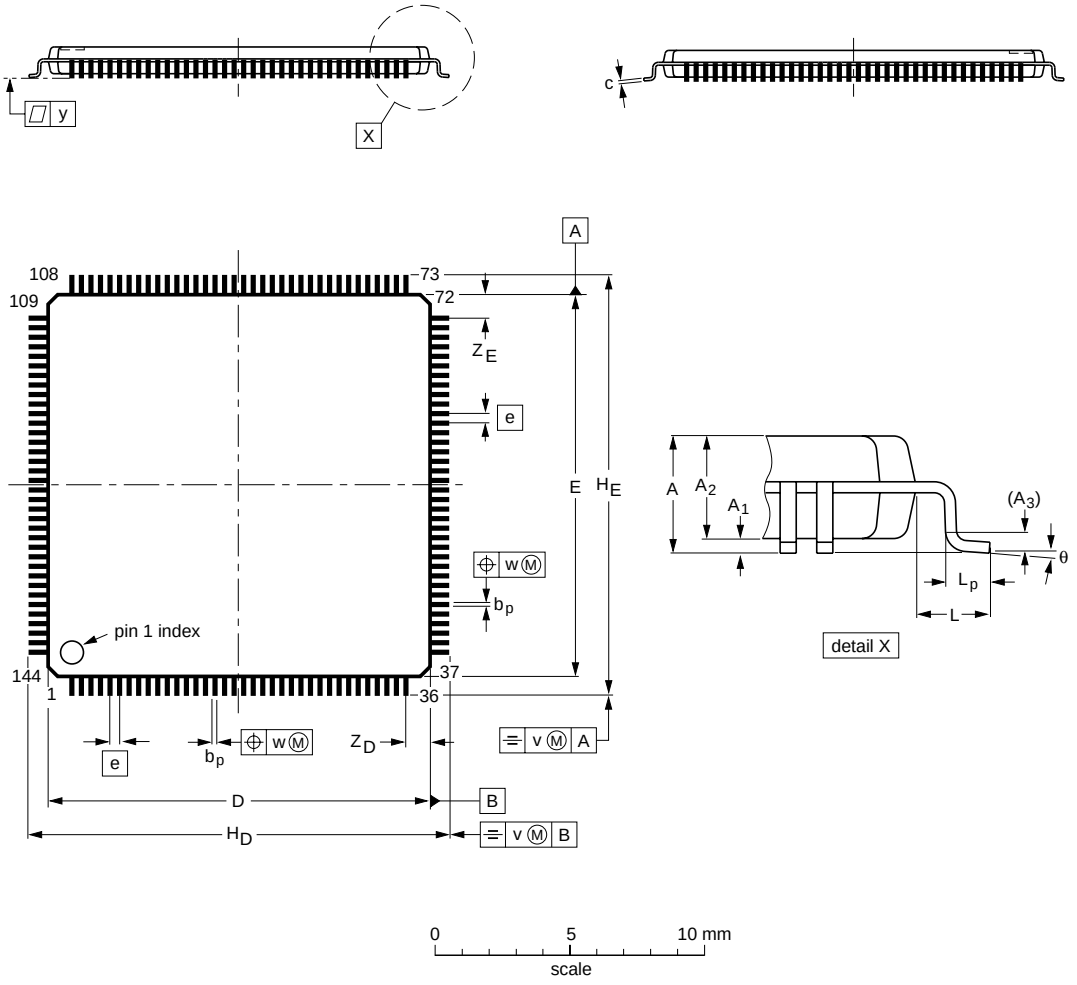


Fig.1 Block diagram.

PACKAGE OUTLINE

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.50	22.15 21.85	22.15 21.85	1.0	0.75 0.45	0.2	0.1	0.1	1.40 1.10	1.40 1.10	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT486-1						97-08-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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