

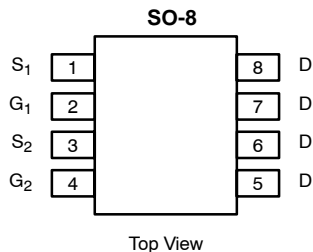


## Complementary MOSFET Half-Bridge (N- and P-Channel)

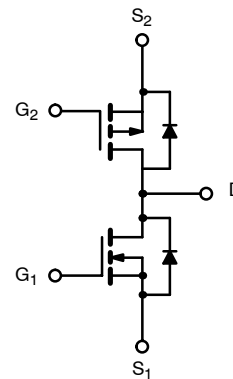
PRODUCT SUMMARY			
	V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
N-Channel	20	0.020 @ V <sub>GS</sub> = 4.5 V	9.1
		0.030 @ V <sub>GS</sub> = 2.5 V	7.5
P-Channel	-20	0.060 @ V <sub>GS</sub> = -4.5 V	-5.3
		0.100 @ V <sub>GS</sub> = -2.5 V	-4.1

### FEATURES

- TrenchFET® Power MOSFET



Ordering Information: Si4500BDY  
Si4500BDY-T1 (with Tape and Reel)  
Si4500BDY—E3 (Lead (Pb)-Free)  
Si4500BDY-T1—E3 (Lead (Pb)-Free with Tape and Reel)



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		10 sec.	Steady State	10 sec.	Steady State		
Drain-Source Voltage	V <sub>DS</sub>	20		-20		V	
Gate-Source Voltage	V <sub>GS</sub>	± 12		± 12			
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a, b</sup>	T <sub>A</sub> = 25°C	9.1	6.6	-5.3	-3.8	A	
	T <sub>A</sub> = 70°C	7.3	5.3	-4.9	-3.1		
Pulsed Drain Current	I <sub>DM</sub>	30		-20			
Continuous Source Current (Diode Conduction) <sup>a, b</sup>	I <sub>S</sub>	2.1	1.1	-2.1	-1.1		
Maximum Power Dissipation <sup>a, b</sup>	T <sub>A</sub> = 25°C	2.5	1.3	2.5	1.3	W	
	T <sub>A</sub> = 70°C	1.6	0.8	1.6	0.8		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150				°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ	Max	Typ	Max		
Maximum Junction-to-Ambient <sup>a</sup>	t ≤ 10 sec	40	50	41	50	°C/W	
	Steady-State	75	95	75	95		
Maximum Junction-to-Foot (Drain)	Steady-State	20	22	23	26		

**Notes**

- a. Surface Mounted on FR4 Board.  
b. t ≤ 10 sec

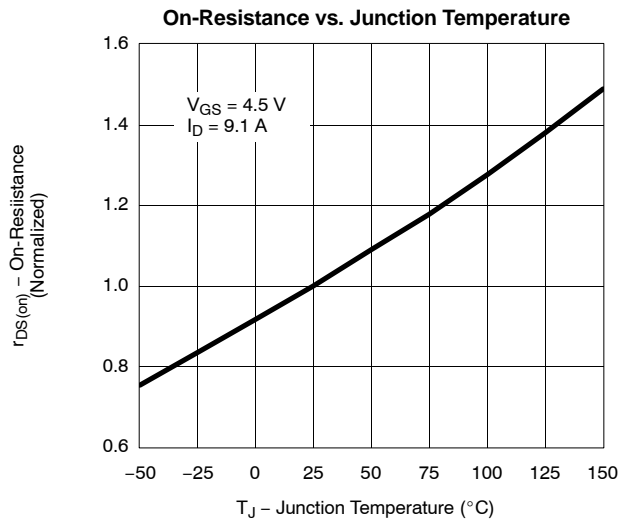
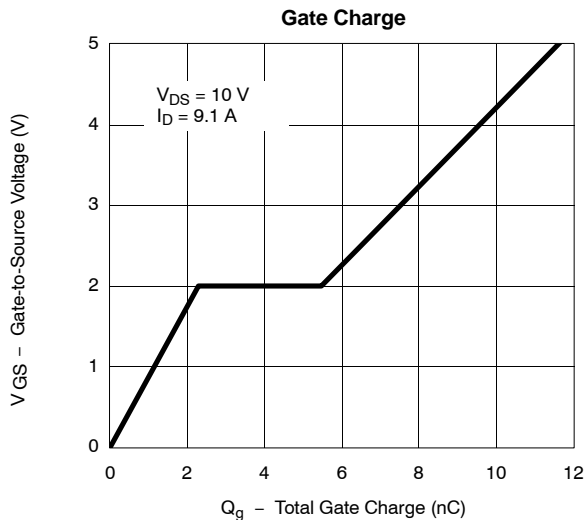
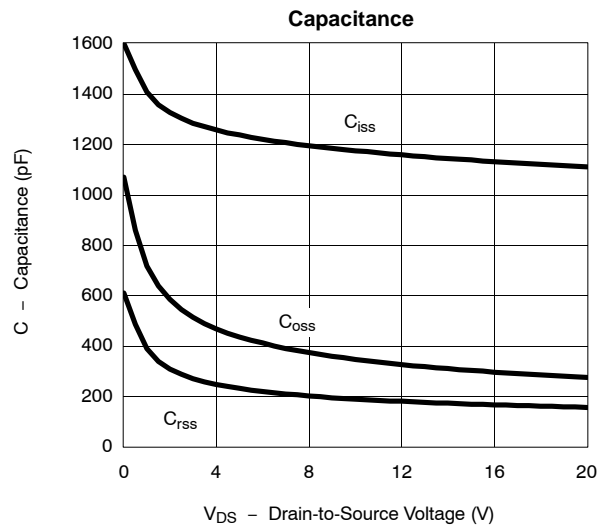
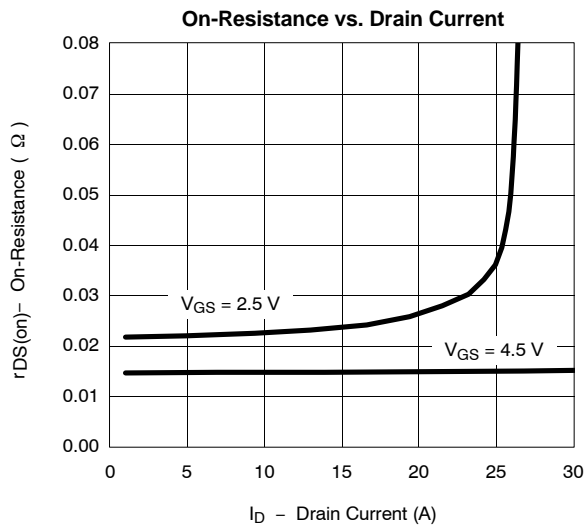
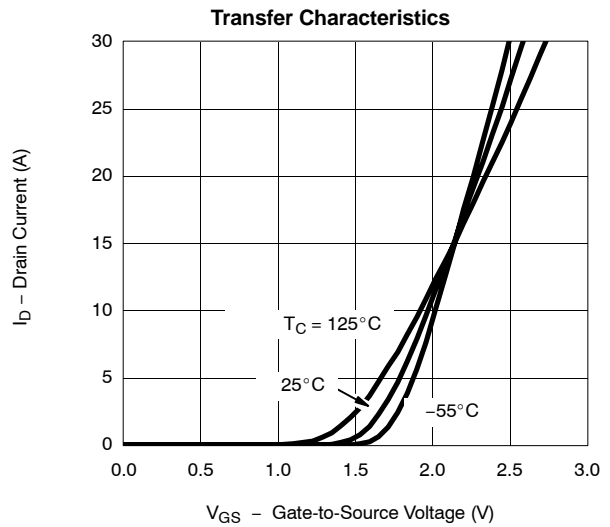
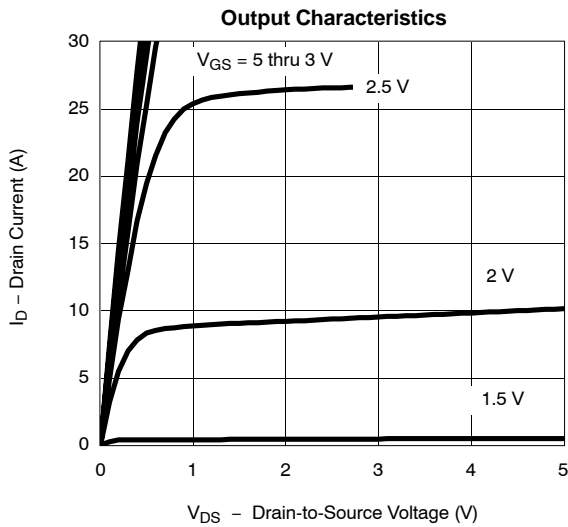
SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit	
<b>Static</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	0.6		1.5	V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-0.6		-1.5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V	N-Ch			±100	nA
			P-Ch			±100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	N-Ch			1	μA
		V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V	P-Ch			-1	
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	N-Ch			5	
		V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	P-Ch			-5	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	30			A
		V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -4.5 V	P-Ch	-20			
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9.1 A	N-Ch		0.016	0.020	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -5.3 A	P-Ch		0.048	0.060	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 3.3 A	N-Ch		0.024	0.030	
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1 A	P-Ch		0.082	0.100	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 9.1 A	N-Ch		29		S
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -5.3 A	P-Ch		11		
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.1 A, V <sub>GS</sub> = 0 V	N-Ch		0.8	1.2	V
		I <sub>S</sub> = -2.1 A, V <sub>GS</sub> = 0 V	P-Ch		-0.8	-1.2	
<b>Dynamic<sup>a</sup></b>							
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9.1 A P-Channel V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -5.3 A	N-Ch		11	17	nC
Gate-Source Charge	Q <sub>gs</sub>		N-Ch		6.0	9	
			P-Ch		2.5		
Gate-Drain Charge	Q <sub>gd</sub>		N-Ch		3.2		
		P-Ch		1.6			
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 6 Ω P-Channel V <sub>DD</sub> = -10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 6 Ω	N-Ch		35	50	ns
Rise Time	t <sub>r</sub>		N-Ch		20	30	
			P-Ch		50	80	
Turn-Off Delay Time	t <sub>d(off)</sub>		N-Ch		35	60	
			P-Ch		31	50	
Fall Time	t <sub>f</sub>		N-Ch		55	85	
			P-Ch		15	30	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		I <sub>F</sub> = 2.1 A, di/dt = 100 A/μs	N-Ch		30	
		I <sub>F</sub> = -2.1 A, di/dt = 100 A/μs	P-Ch		25	50	

## Notes

- a. Guaranteed by design, not subject to production testing.  
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

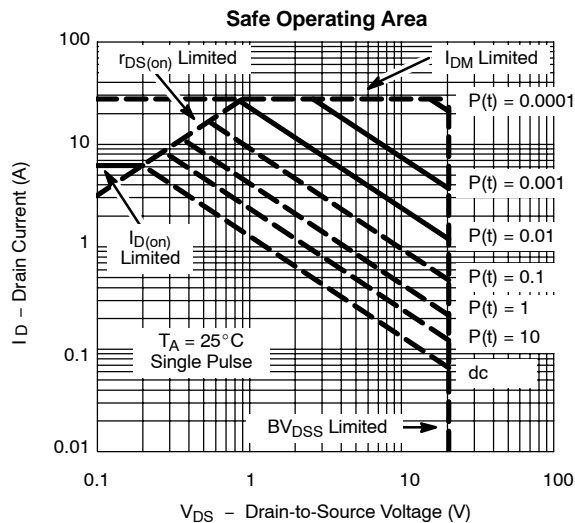
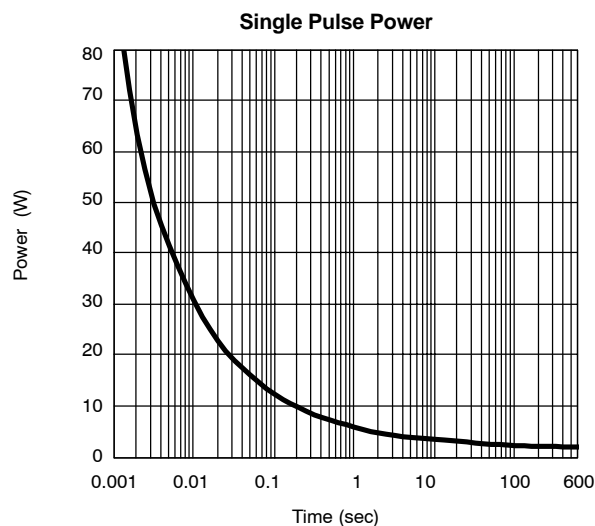
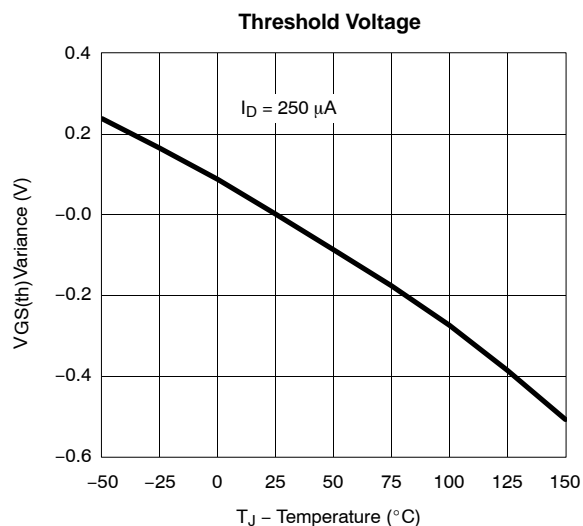
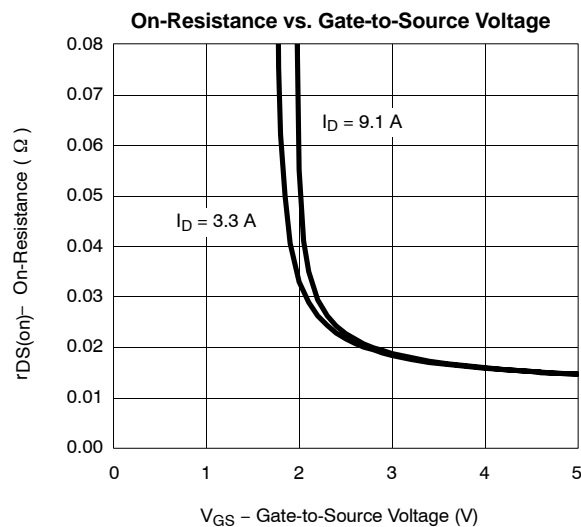
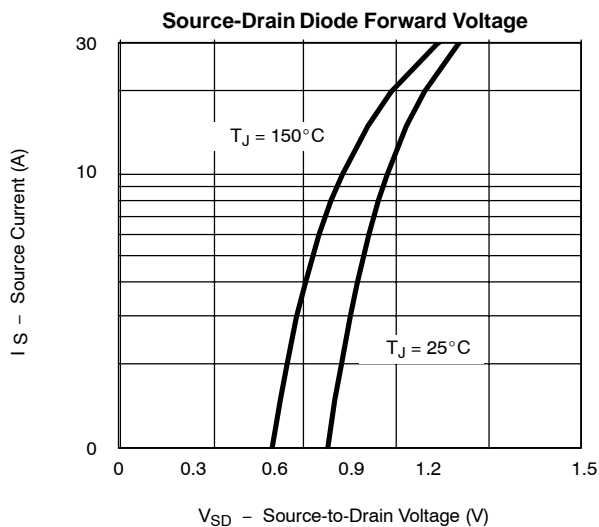


**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) N-CHANNEL**



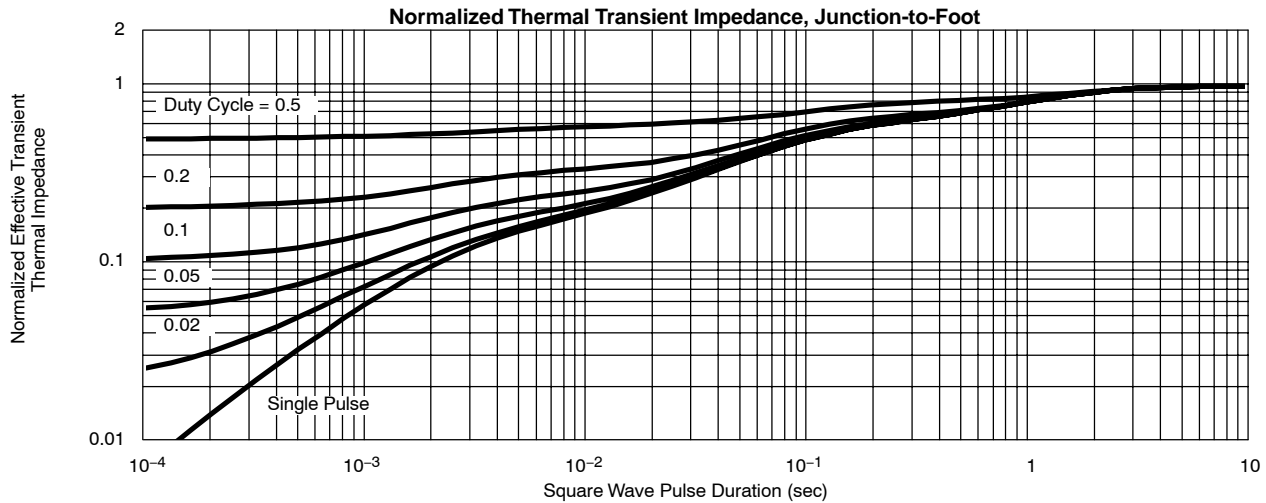
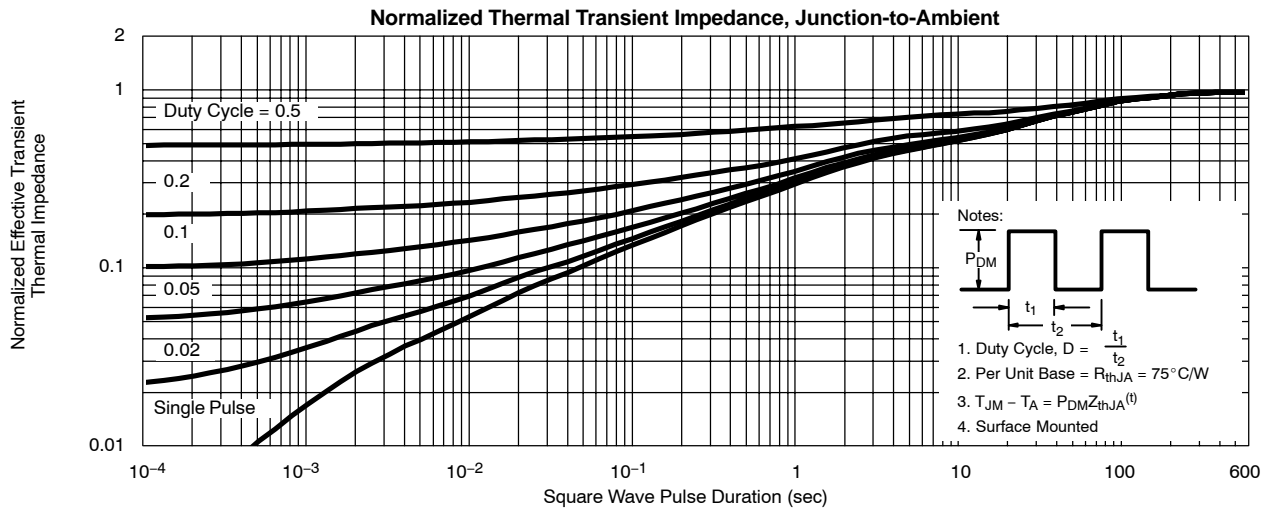
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

**N-CHANNEL**

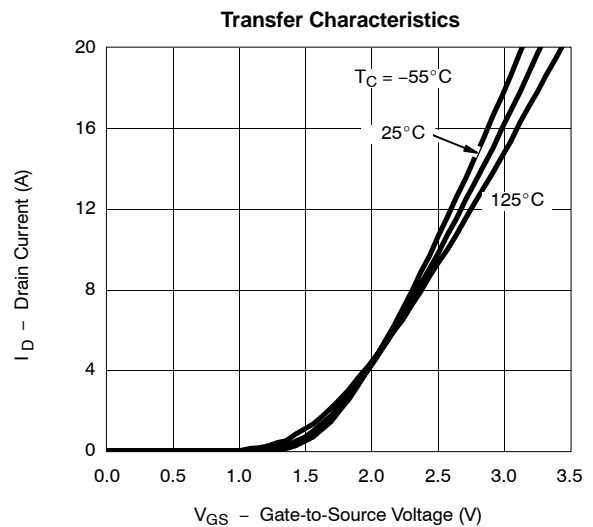
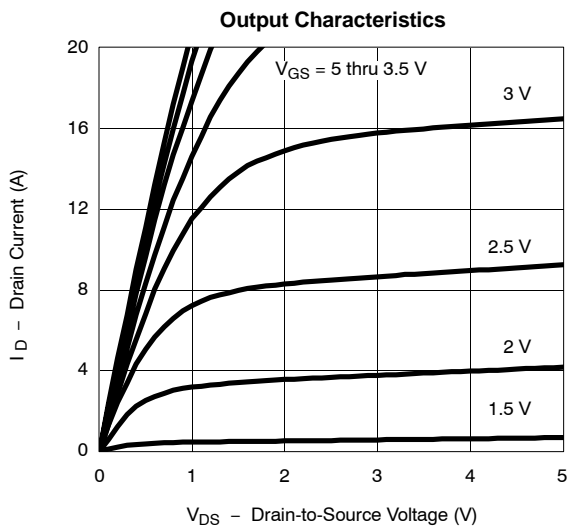




**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) N-CHANNEL**



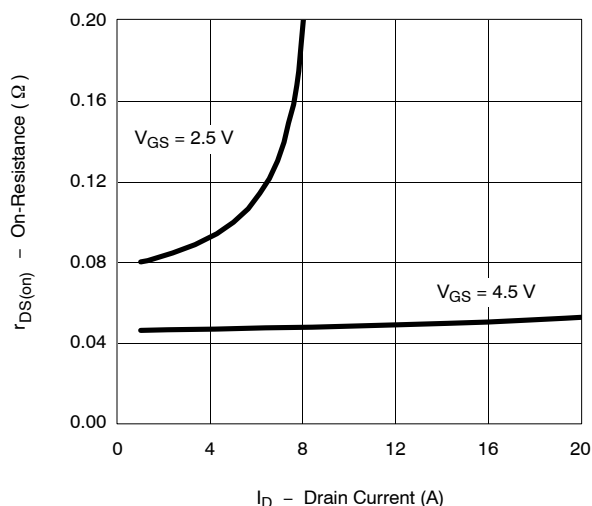
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) P-CHANNEL**



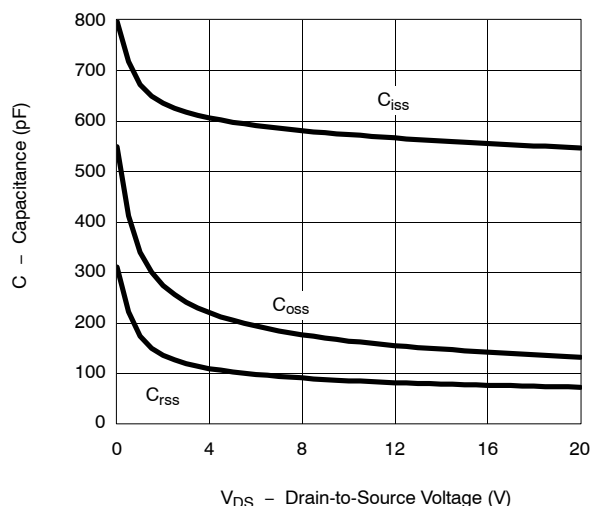
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

**P-CHANNEL**

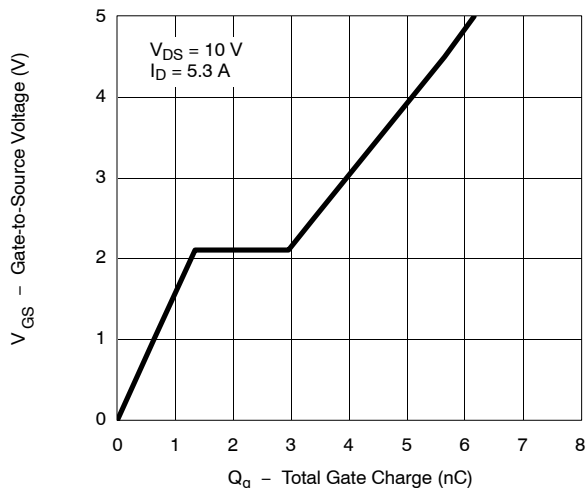
**On-Resistance vs. Drain Current**



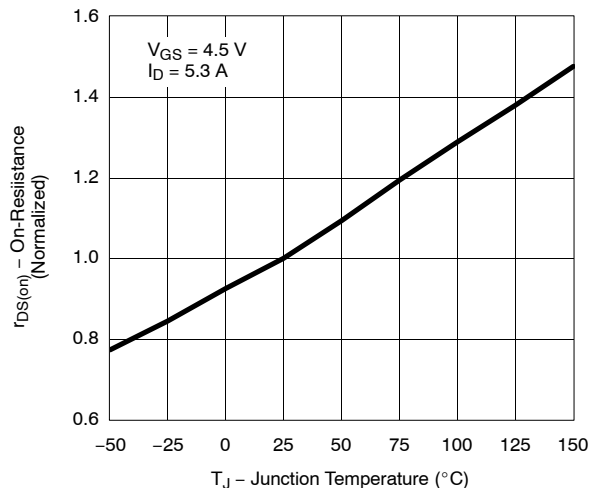
**Capacitance**



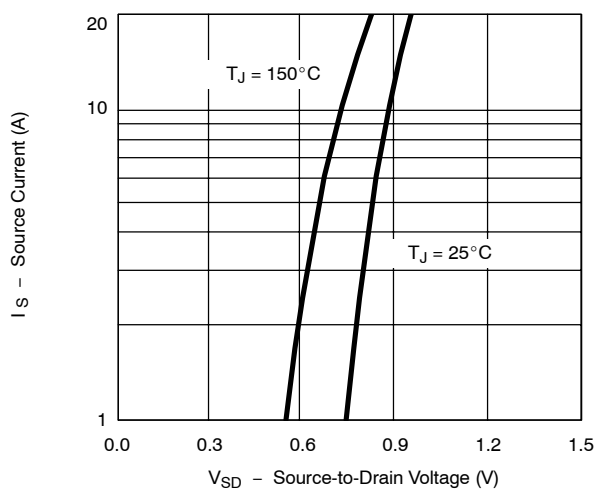
**Gate Charge**



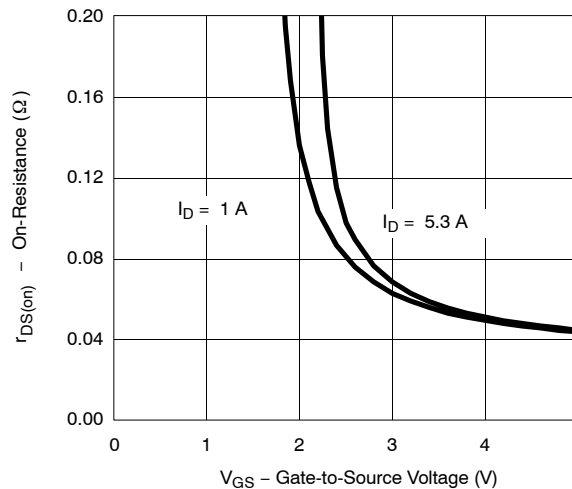
**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**

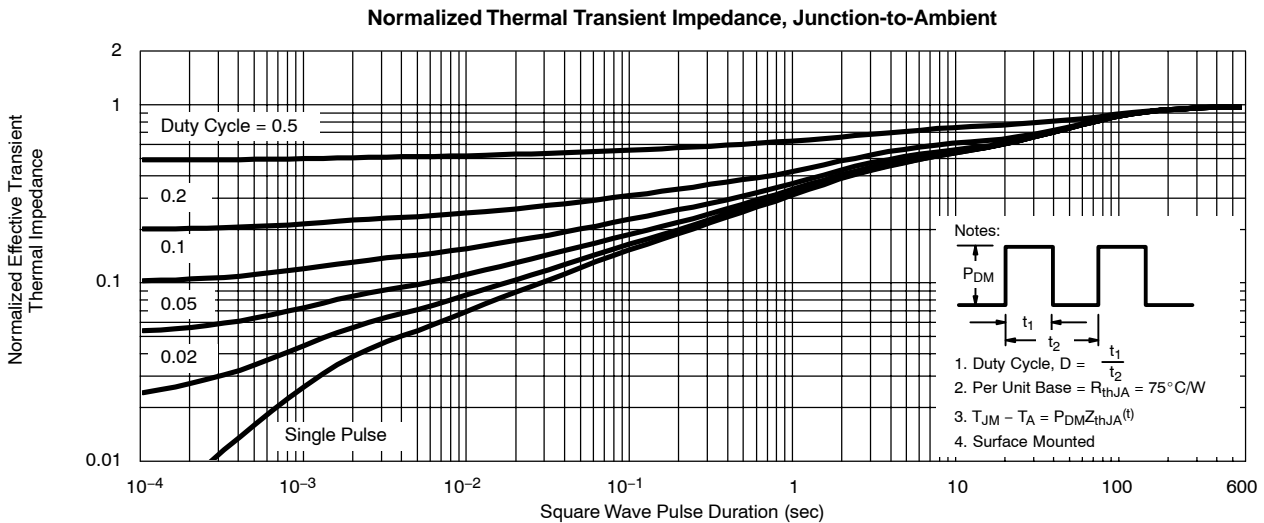
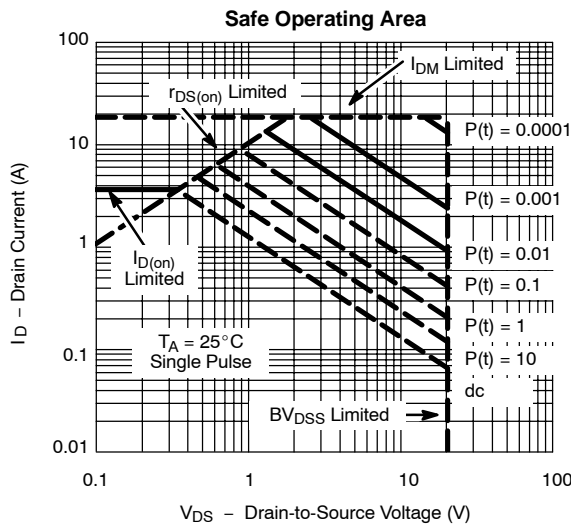
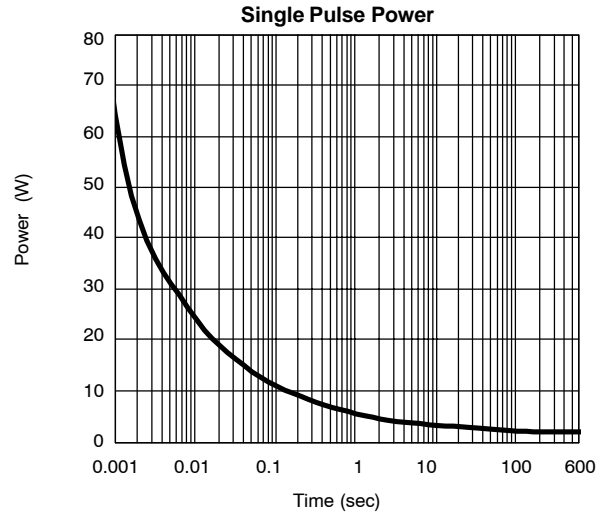
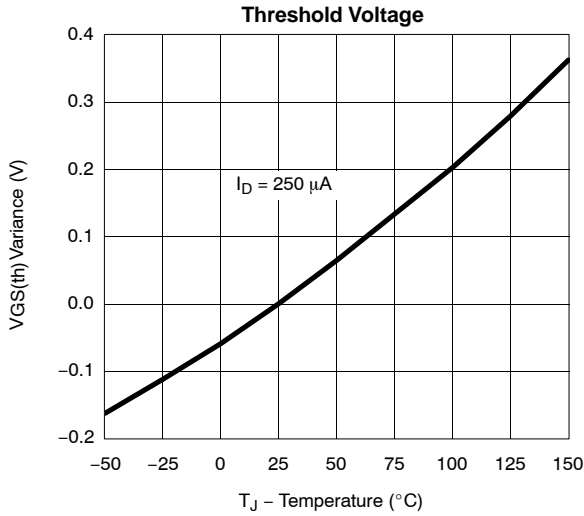


**On-Resistance vs. Gate-to-Source Voltage**





**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

**P-CHANNEL**

