MCP6002

1 MHz Bandwidth Low Power Op Amp

Features

- 1 MHz bandwidth (typ.)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8 V to 5.5 V
- Supply Current: I_Q = 108 µA (typ.)
- 90° Phase Margin
- Industrial Temperature Range: -40°C to +85°C
- Available in Dual Package

Applications

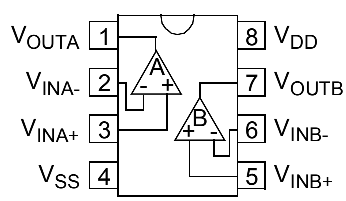
- Portable Equipment
- Photodiode Pre-amps
- Analog Filters
- Notebooks and PDAs
- Battery Powered Systems

Available Tools

Spice Macromodels (at www.microchip.com)
FilterLab® Software (at www.microchip.com)

Package Types

PDIP, SOIC, MSOP

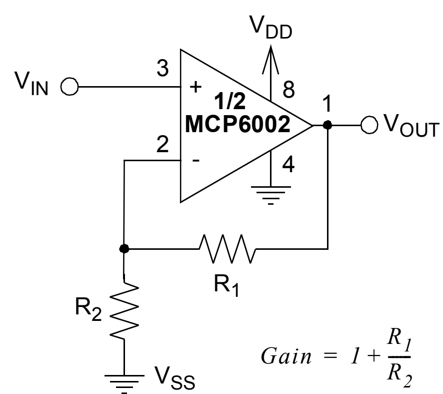


Description

The Microchip Technology Inc. MCP6002 operational amplifier is targeted towards general purpose applications. The Dual MCP6002 has 1 MHz bandwidth and 90° phase margin (typ.). It also maintains 45° phase margin (typ.) with 500 pF capacitive load. This device operates from a single supply voltage as low as 1.8 V, while drawing 108 µA (typ.) quiescent current. In addition, MCP6002 supports rail-to-rail input and output swing, with a common mode input voltage range of V_{DD} + 300 mV to V_{SS} - 300 mV. This operational amplifier is designed with Microchip's advanced CMOS process.

This device is specified from -40°C to +85°C with a power supply range of 1.8 V to 5.5 V.

Typical Application



Non-Inverting Amplifier

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} - V_{SS} ....7.0 V
All Inputs and Outputs .... V_{SS} -0.3 V to V_{DD} +0.3 V
Difference Input Voltage .... |V_{DD} - V_{SS}|
Output Short Circuit Current ....continuous
Current at Input Pins ....±2 mA
Current at Output and Supply Pins ....±30 mA
Storage Temperature ....-65°C to +150°C
Junction Temp. (T_J) ....+150°C
ESD Protection On All Pins (HBM/MM) .... ≥ 4 kV/200 V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{INA+}/V_{INB+}	Non-inverting Inputs
V_{INA-}/V_{INB-}	Inverting Inputs
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
V_{OUTA}/V_{OUTB}	Outputs

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = +1.8 V to +5.5 V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and V_{OUT} ~ V_{DD}/2.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-7	—	7	mV	V_{CM} = V_{SS}
Input Offset Voltage Drift with Temperature	$\Delta V_{OS}/\Delta T$	—	±2	—	µV/°C	T_A= -40°C to +85°C, V_{CM} = V_{SS}
Power Supply Rejection	PSRR	—	86	—	dB	V_{CM} = V_{SS}
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1	—	pA	
Input Bias Current	I_B	—	19	—	pA	T_A = +85°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common Mode						
Common-Mode Input Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common-Mode Rejection Ratio	CMRR	60	76	—	dB	V_{CM} = -0.3 V to 5.3 V, V_{DD} = 5 V
Open Loop Gain						
DC Open Loop Gain (large signal)	A_{OL}	88	112	—	dB	V_{OUT} = 0.3 V to V_{DD} - 0.3 V, V_{CM} = V_{SS}
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 5.5 V
Output Short Circuit Current	I_{SC}	—	±23	—	mA	V_{DD} = 5.5 V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	50	108	170	µA	I_O = 0, V_{DD} = 5.5 V, V_{CM} = 5 V

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
AC Response						
Gain Bandwidth Product	GBWP	—	1	—	MHz	
Phase Margin at Unity Gain	PH	—	90	—	degrees	G = +1
Slew Rate	SR	—	0.6	—	V/µs	
Noise						
Input Noise Voltage	E_n	—	6	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_n	—	28	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_n	—	0.6	—	fA/√Hz	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8 V to +5.5 V, and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	

Note: The MCP6002 operates over this extended temperature range, but with reduced performance. In any case, T_J must not exceed the Maximum Junction Temperature (150°C).

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

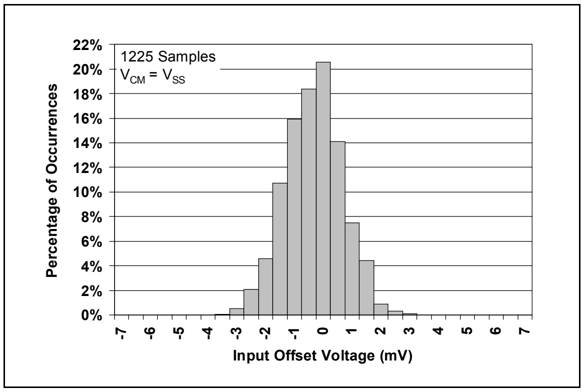


FIGURE 2-1: *Histogram of Input Offset Voltage with V_{CM} = V_{SS}.*

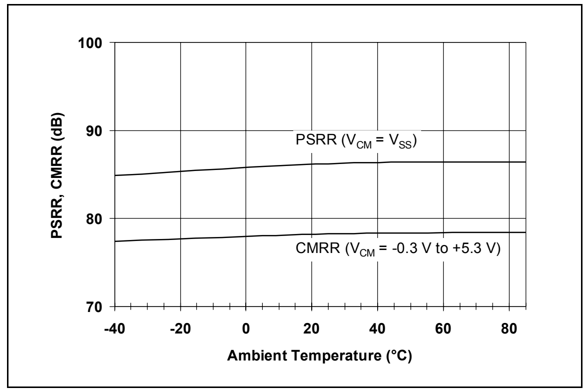


FIGURE 2-4: *Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Temperature.*

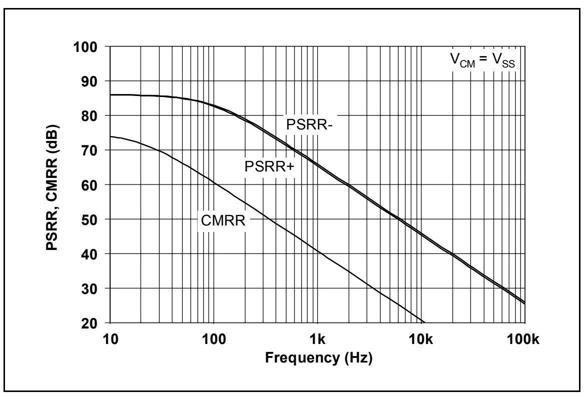


FIGURE 2-2: *Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Frequency.*

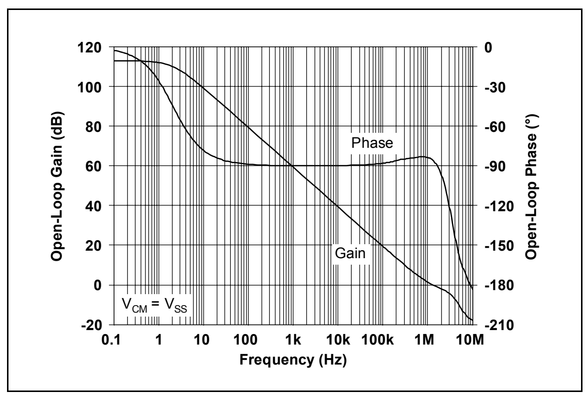


FIGURE 2-5: *Open Loop Gain, Phase vs. Frequency.*

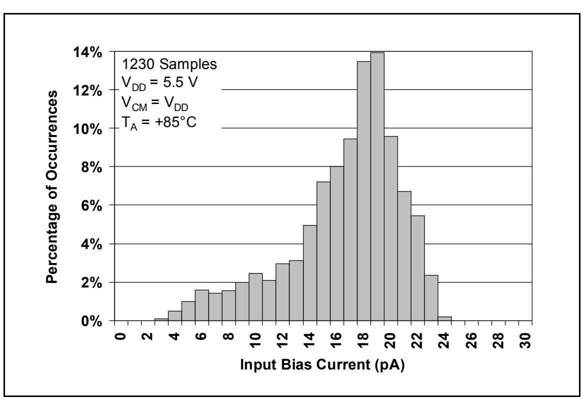


FIGURE 2-3: *Input Bias Current Histogram with Temperature = 85°C.*

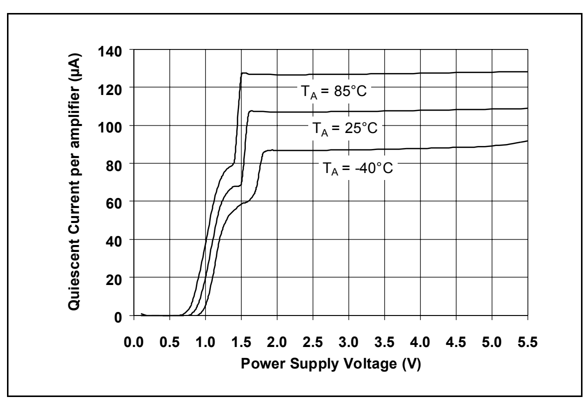


FIGURE 2-6: *Quiescent Current vs. Power Supply Voltage vs. Temperature.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

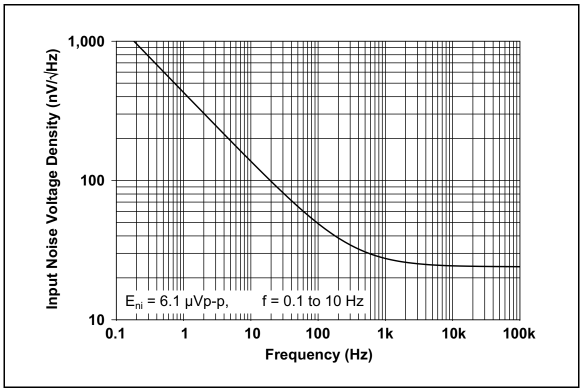


FIGURE 2-7: *Input Noise Voltage Density vs. Frequency.*

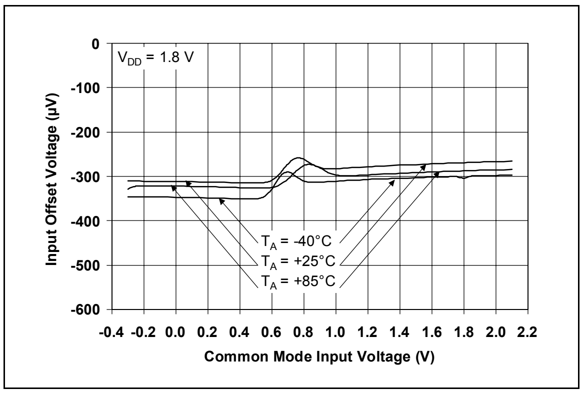


FIGURE 2-8: *Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with V_{DD} = 1.8 V.*

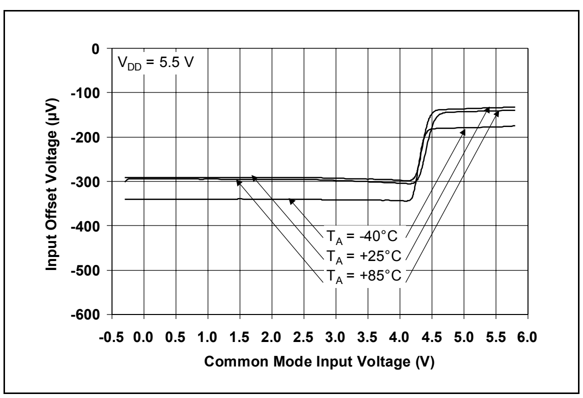


FIGURE 2-9: *Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with V_{DD} = 5.5 V.*

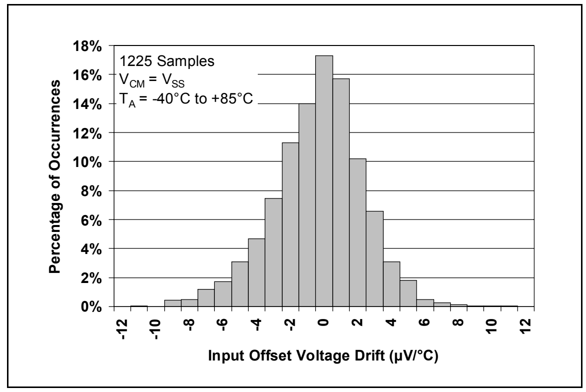


FIGURE 2-10: *Histogram of Input Offset Voltage Drift with V_{CM} = V_{SS}.*

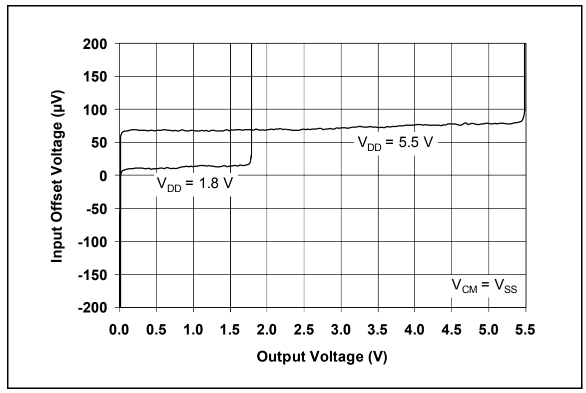


FIGURE 2-11: *Input Offset Voltage vs. Output Voltage vs. Power Supply Voltage.*

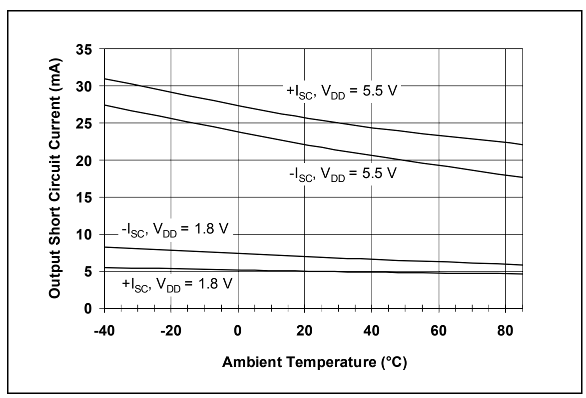


FIGURE 2-12: *Output Short Circuit Current vs. Temperature vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0 V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \sim V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$, and C_L = 60 pF.

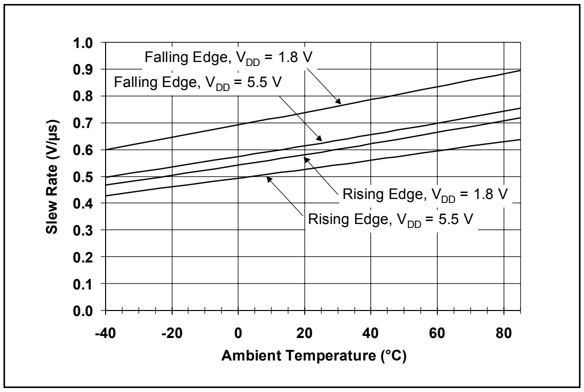


FIGURE 2-13: *Slew Rate vs. Temperature vs. Power Supply Voltage.*

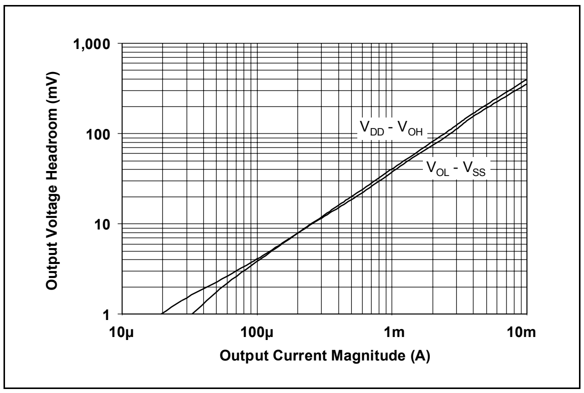


FIGURE 2-14: *Output Voltage Headroom vs. Output Current.*

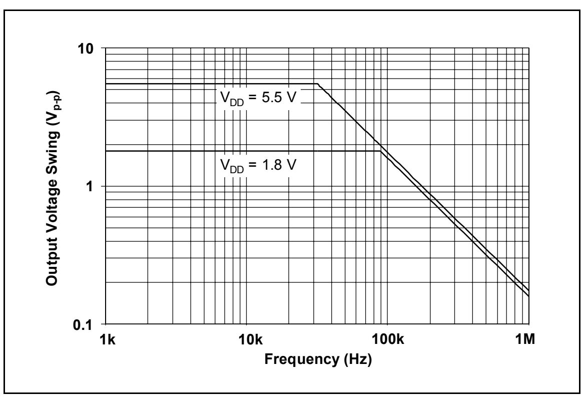


FIGURE 2-15: *Output Voltage Swing vs. Frequency vs. Power Supply Voltage.*

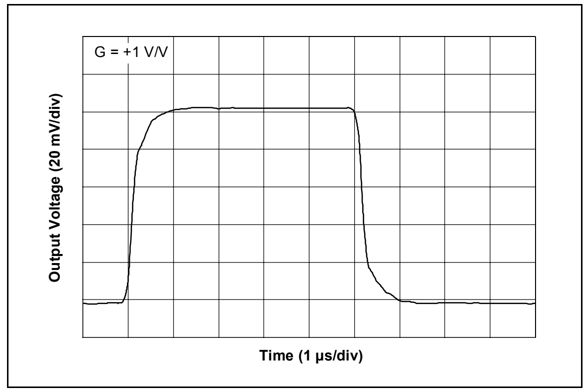


FIGURE 2-16: *Small Signal Non-Inverting Pulse Response.*

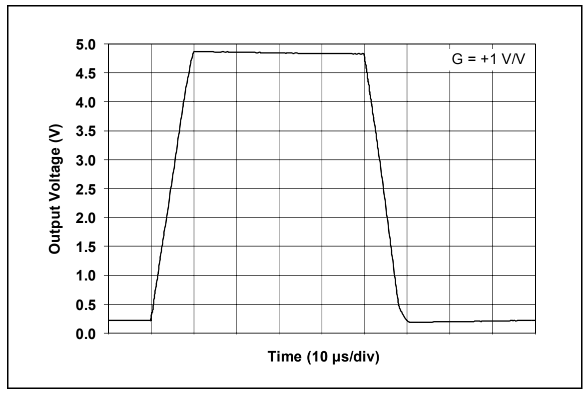


FIGURE 2-17: *Large Signal Non-Inverting Pulse Response.*

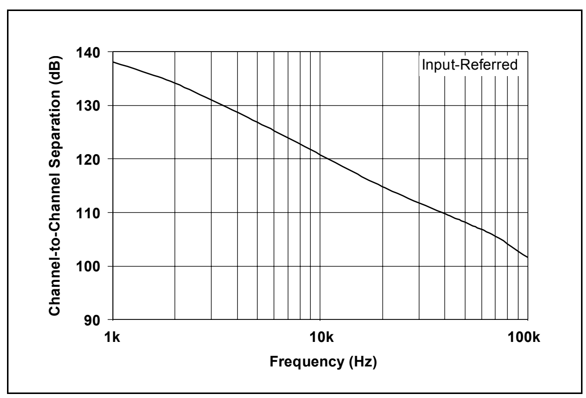


FIGURE 2-18: *Channel-to-Channel Separation vs. Frequency.*

3.0 APPLICATION INFORMATION

The MCP6002 is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low cost, low power and general purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6002 ideal for battery powered applications. This device has high phase margin which makes it stable for larger capacitive load applications.

3.1 Rail-to-Rail Input

The input stage of the MCP6002 uses two differential input stages in parallel; one operates at low common mode input voltage (V_{CM}) and the other at high V_{CM}. With this topology, the MCP6002 operates with V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS}. The Input Offset Voltage is measured at $V_{CM} = V_{SS}$ - 300 mV and V_{DD} + 300 mV to ensure proper operation.

3.2 Rail-to-Rail Output

The output voltage range of the MCP6002 is V_{DD} - 25 mV (min.) and V_{SS} + 25 mV (max.) when R_L = 10 kΩ is connected to $V_{DD}/2$ and V_{DD} = 5.5 V. Refer to Figure 2-14 for more information.

3.3 Phase Reversal and Input Voltage

The MCP6002 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 3-1 shows an input voltage exceeding both supplies without any phase reversal.

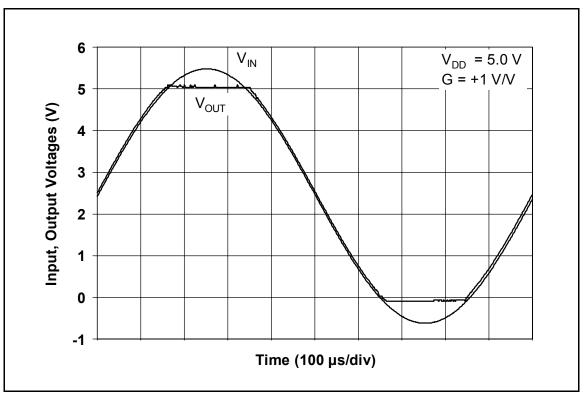
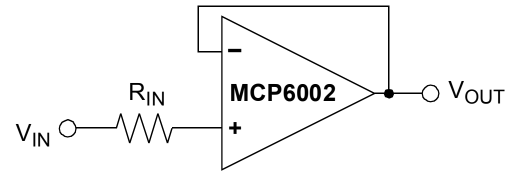


FIGURE 3-1: *The MCP6002 Shows No Phase Reversal.*

The maximum operating V_{CM} that can be applied to the inputs is V_{SS} - 300 mV (min.) and V_{DD} + 300 mV (max.). Input voltages that exceed this absolute maximum rating can cause excessive current to flow into or out of the input pins. Current beyond ±2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor as shown in Figure 3-2.



$$R_{IN} \geq \frac{(Maximum\ expected\ V_{IN}) - V_{DD}}{2\ mA}$$

$$R_{IN} \geq \frac{V_{SS} - (Minimum\ expected\ V_{IN})}{2\ mA}$$

FIGURE 3-2: *Input Current Limiting Resistor (R_{IN}).*

3.4 Capacitive Load and Stability

Capacitive loads can cause stability problems with voltage feedback op amps. A buffer configuration (G = +1) is the most sensitive to capacitive loads. Figure 3-3 shows how increasing the load capacitance will decrease the phase margin and reduce the bandwidth. A phase margin above 60° is best, but 45° is still usable.

The MCP6002 has a phase margin of 90° under the specified conditions in the AC characteristics table. The MCP6002 maintains greater than 60° phase margin (typ.), with 200 pF capacitive load. It also maintains stability at 45° phase margin (typ.), with 500 pF capacitive load, as shown in Figure 3-3.

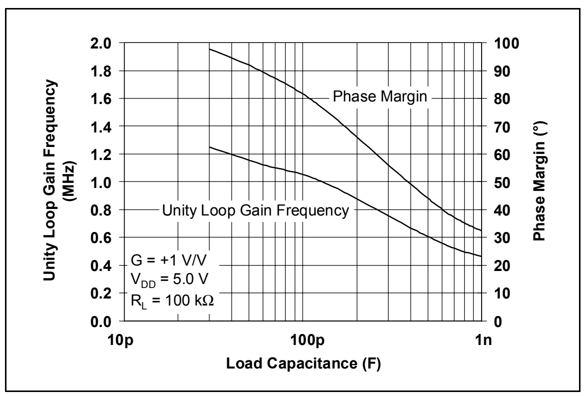


FIGURE 3-3: *Gain Bandwidth Product, Phase Margin vs. Load Capacitance with Unity Gain.*

If the MCP6002 is required to drive large capacitive loads (C_L > 500 pF), then a series resistor (R_{ISO} in Figure 3-4) at the output of the amplifier improves the phase margin. This resistor makes the output load resistive at higher frequencies. The bandwidth reduction caused by the capacitive load, however, is not changed. To select R_{ISO}, use the SPICE macro model starting with 1 kΩ and adjust this resistor until the frequency response shows low peaking.

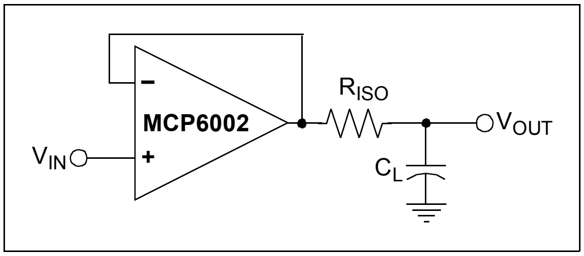


FIGURE 3-4: Amplifier Circuit for Heavy Capacitive Loads.

3.5 Application Circuits

3.5.1 UNITY GAIN BUFFER

The rail-to-rail input and output capability of the MCP6002 is ideal for unity gain buffer applications. The low quiescent current and wide bandwidth makes the MCP6002 suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 3-5.

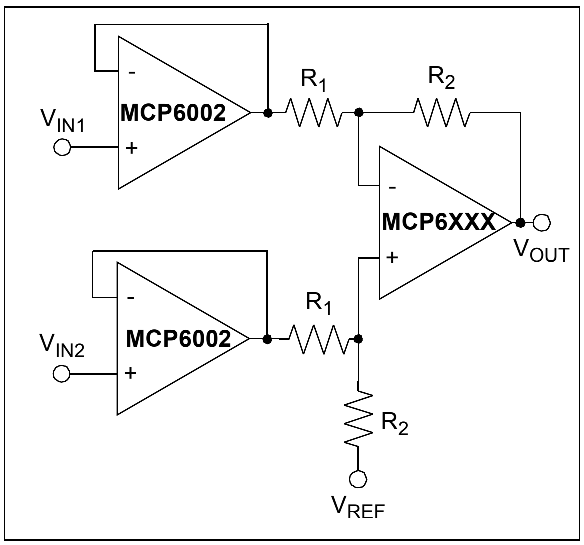


FIGURE 3-5: Instrumentation Amplifier with Unity Gain Buffer Inputs.

3.5.2 ACTIVE LOW PASS FILTER

The MCP6002 is suitable for active low pass filter applications, as shown in Figure 3-6. It is possible to have a filter cutoff frequency as high as 1/10th of the op amp bandwidth, or 100 kHz at unity gain. The low input bias current also makes it possible for the designer to use larger resistor values and smaller capacitor values. However, as the resistances increase, the noise generated also increases. In addition, parasitic capacitances and the large value resistors could modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

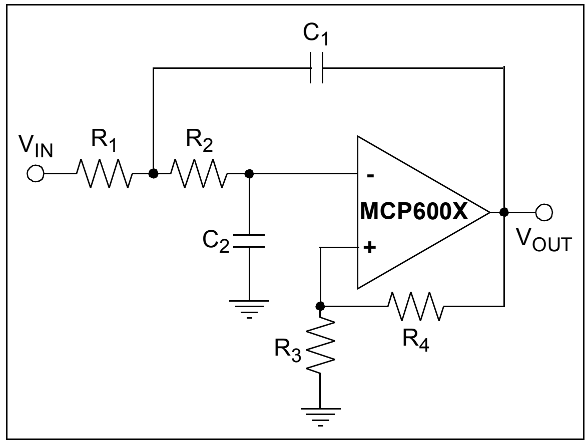


FIGURE 3-6: Active Low Pass Filter.

The component values in Figure 3-6 can be selected using Microchip's FilterLab®, which is a software tool that simplifies active filter design. This tool provides schematic diagrams of filter circuits (up to the 8th order) with resistor and capacitor values, and displays the frequency response.

FilterLab can be downloaded, free of charge, from the Microchip website (www.microchip.com).

3.5.3 PEAK DETECTOR

The MCP6002 has high input impedance, rail-to-rail input and output, and low input bias current, which makes this device suitable for a peak detector application. Figure 3-7 shows a peak detector circuit with Clear and Sample switches. The peak detection cycle uses a clock (CLK), as shown in Figure 3-7.

At the rising edge of CLK, Sample Switch closes to begin sampling. The peak voltage stored on C_1 is sampled to C_2 for a sample time defined by t_{SAMP}. At the end of the sample time (falling edge of Sample Signal), Clear Signal goes high and closes the Clear Switch. When the Clear Switch closes, C_1 depletes through R for a time defined by t_{CLEAR}. At the end of the clear time (falling edge of Clear Signal), op amp A begins to store the peak value of V_{IN} on C_1 for a time defined by t_{DETECT}.

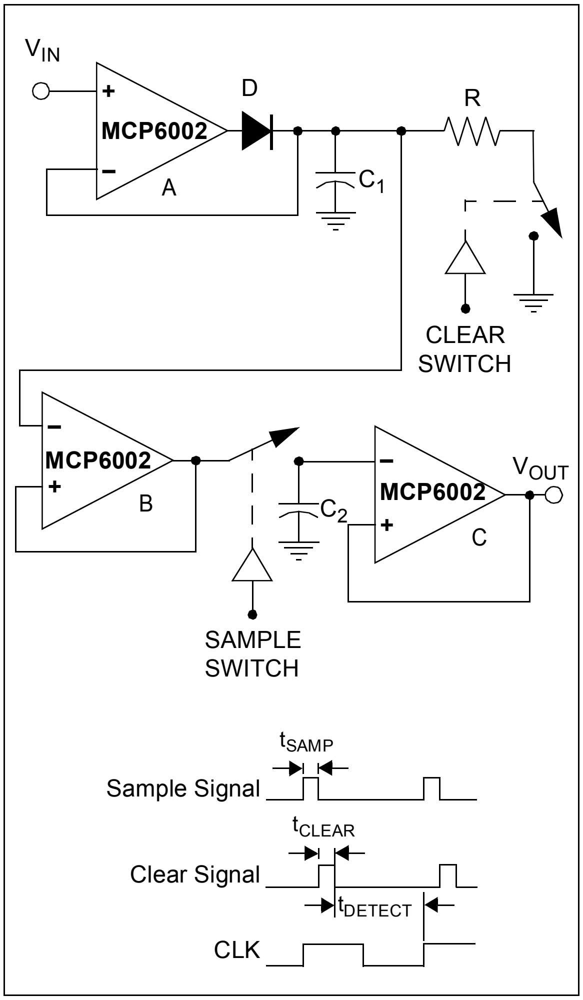


FIGURE 3-7: *Peak Detector with Clear and Sample CMOS Analog Switches.*

3.5.4 RELAXATION OSCILLATOR

This general purpose amplifier (MCP6002) fits well in a relaxation oscillator circuit, as shown in Figure 3-8. The oscillation frequency is set by R and C. The R_1 and R_2 resistors are used to set the high and low switching voltages, as shown in the timing diagram of Figure 3-8.

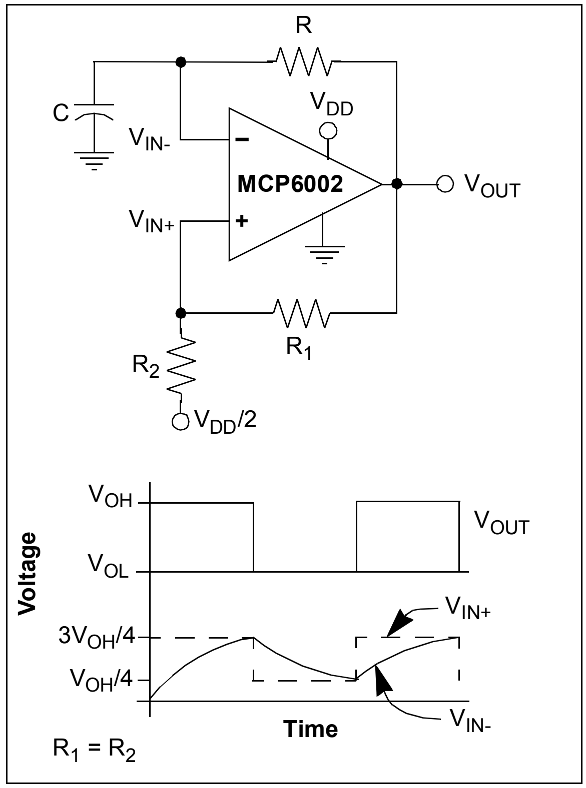


FIGURE 3-8: *Relaxation Oscillator.*

3.5.5 OPTICAL DETECTOR AMPLIFIER

Figure 3-9 shows the MCP6002 op amp used as a transimpedance amplifier in a photo detector circuit. The photo detector looks like a capacitive current source. The resistor, R_1, converts the input signal to the output voltage, V_{OUT}. The capacitor, C_1, stabilizes this circuit and produces a low pass response.

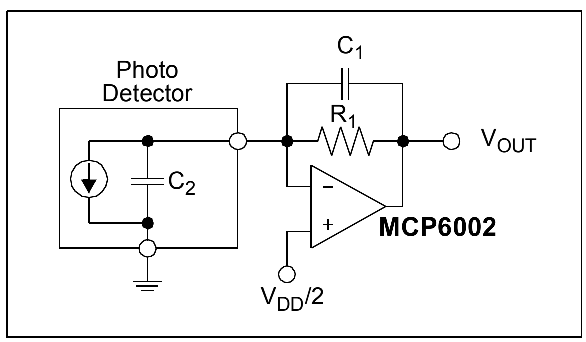


FIGURE 3-9: *Transimpedance Amplifier for an Optical Detector.*

4.0 SPICE MACRO MODEL

The Spice macro model for the MCP6002 simulates the typical amplifier performance of: offset voltage, DC power supply rejection, input capacitance, DC common mode rejection, open loop gain over frequency, phase margin, output swing, DC power supply current, power supply current change with supply voltage, input common mode range, output voltage range vs. load and input voltage noise.

The listing for this macro model is shown on the next page. The most recent revision of the model can be downloaded from Microchip's web site at www.microchip.com.

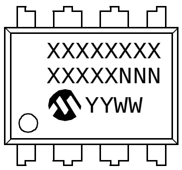
```
.SUBCKT MCP6002 1 2 3 4 5
*               | | | | |
*               | | | | Output
*               | | | Negative Supply
*               | | Positive Supply
*               | Inverting Input
*               Non-inverting Input
*
* Macromodel for the MCP6002 (dual)
*
* Revision History:
*   REV A: 06-21-02 created KEB
*
* Recommendations:
*   Use PSPICE (or SPICE 2G6; other simulators may require translation)
*   For a quick, effective design, use a combination of: data sheet
*     specs, bench testing, and simulations with this macromodel
*   For high impedance circuits, set GMIN=100F in the .OPTIONS
*     statement
*
* Included:
*   Typical performance at room temperature (25 degrees C)
*   DC, AC, Transient, and Noise analyses.
*   Most specs, including: offsets, DC PSRR, DC CMRR, input impedance,
*     open loop gain, voltage ranges, supply current, ... , etc.
*
* Not Included:
*   Variation in specs vs. Power Supply Voltage
*   Distortion (detailed non-linear behavior)
*   Temperature analysis
*   Process variation
*   Behavior outside normal operating region
*
* Input Stage
V10  3 10 -0.3
R10 10 11 8K
R11 10 12 8K
C11 11 12 0.2P
C12  1  0 6P
E12  1 14 POLY(4) 20 0 21 0 26 0 27 0   1M 21 21 1 1
I12 14  0 1.5P
M12 11 14 15 15 NMI L=2U W=42U
C13 14  2 3P
M14 12  2 15 15 NMI L=2U W=42U
I14  2  0 0.5P
C14  2  0 6P
I15 15  4 50U
V16 16  4 0.30
D16 16 15 DL
V13  3 13 0.00
D13 14 13 DL
```

```
*
* Noise Sources
I20 21 20 423U
D20 20  0 DN1
D21  0 21 DN1
*
* PSRR and CMRR
G26  0 26 POLY(1) 3 4   110U -20U
R26 26  0 1
G27  0 27 POLY(2) 1 3 2 4   -440U 80U 80U
R27 27  0 1
*
* Open Loop Gain, Slew Rate
G30  0 30 POLY(1) 12 11   0 1K
R30 30  0 1
E31 31  0 POLY(1) 3 4   57.2 8.33
D31 30 31 DL
E32  0 32 POLY(1) 3 4   74.0 8.00
D32 32 30 DL
G33  0 33 POLY(1) 30 0   0 447
R33 33  0 1
C33 33  0 76.15M
G34  0 34 POLY(1) 33 0   0 1
R34 34  0 1
C34 34  0 50N
G35  0 35 POLY(2) 34 0 33 34   0 1 2.70
R35 35  0 1
*
* Output Stage
G40  0 40 POLY(1) 47 5   0 2
D41 40 41 DL
R41 41  0 1K
D42 42 40 DL
R42 42  0 1K
G43  3  0 POLY(1) 41 0   50U  1M
G44  0  4 POLY(1) 42 0   50U -1M
E45 45  0 POLY(2) 3 0 41 0   -20M 1 -40M
D45 47 45 DLS
E46 46  0 POLY(2) 4 0 42 0    20M 1 -40M
D46 46 47 DLS
G47  0 47 POLY(3) 3 0 4 0 35 0   0 1M 1M 2M
R47 47  0 500
R48 47  5 0.5
C48  5  0 2P
*
* Models
.MODEL NMI NMOS
.MODEL DL   D N=1   IS=1F
.MODEL DLS  D N=1M  IS=1F
.MODEL DN1  D IS=1F KF=1E-16 AF=1
*
.ENDS MCP6002
```

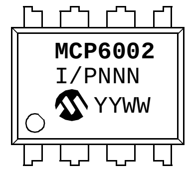
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

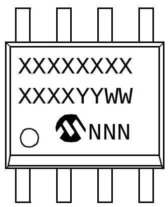
8-Lead PDIP (300 mil)



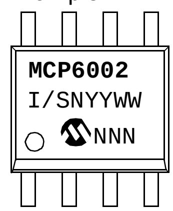
Example:



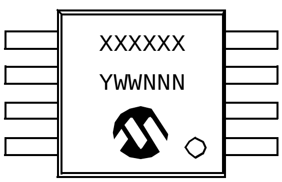
8-Lead SOIC (150 mil)



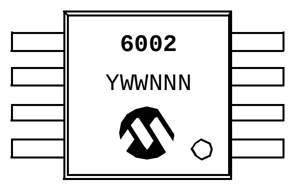
Example:



8-Lead MSOP



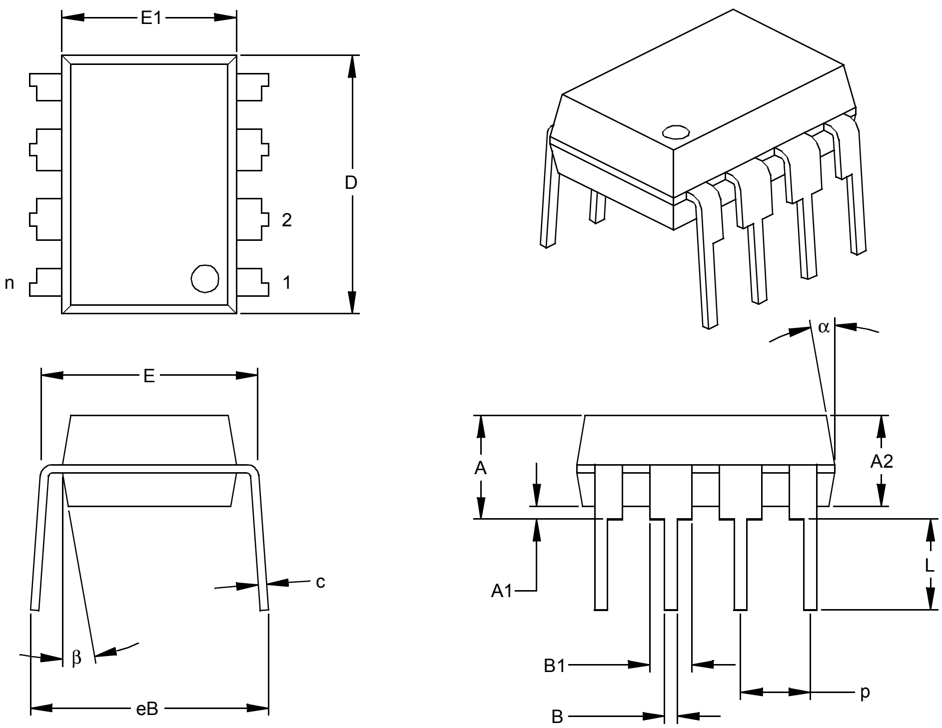
Example:



Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

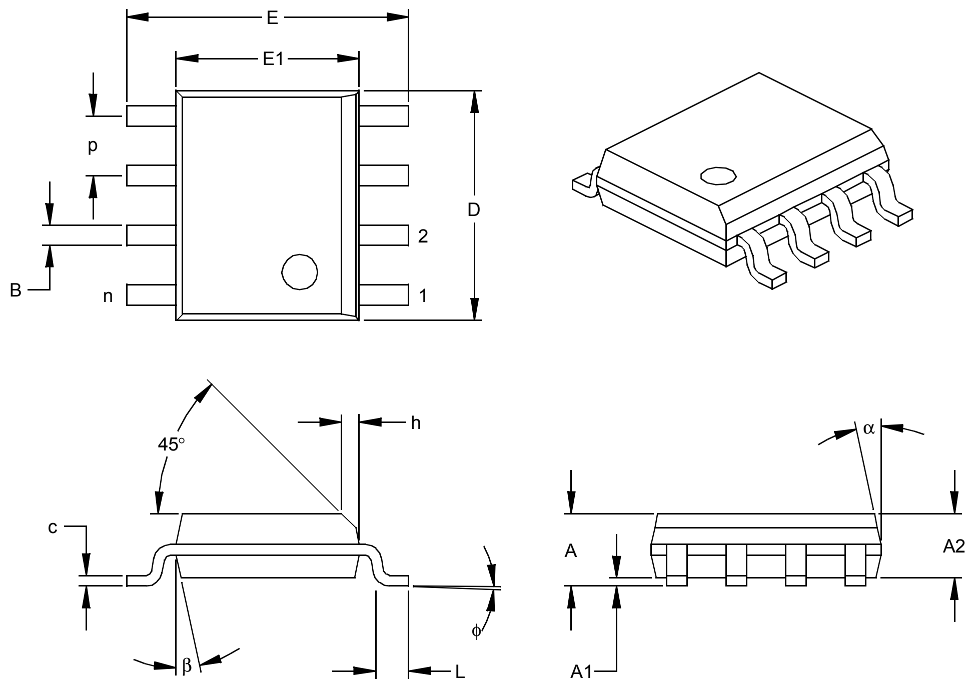


	Units	INCHES*			MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

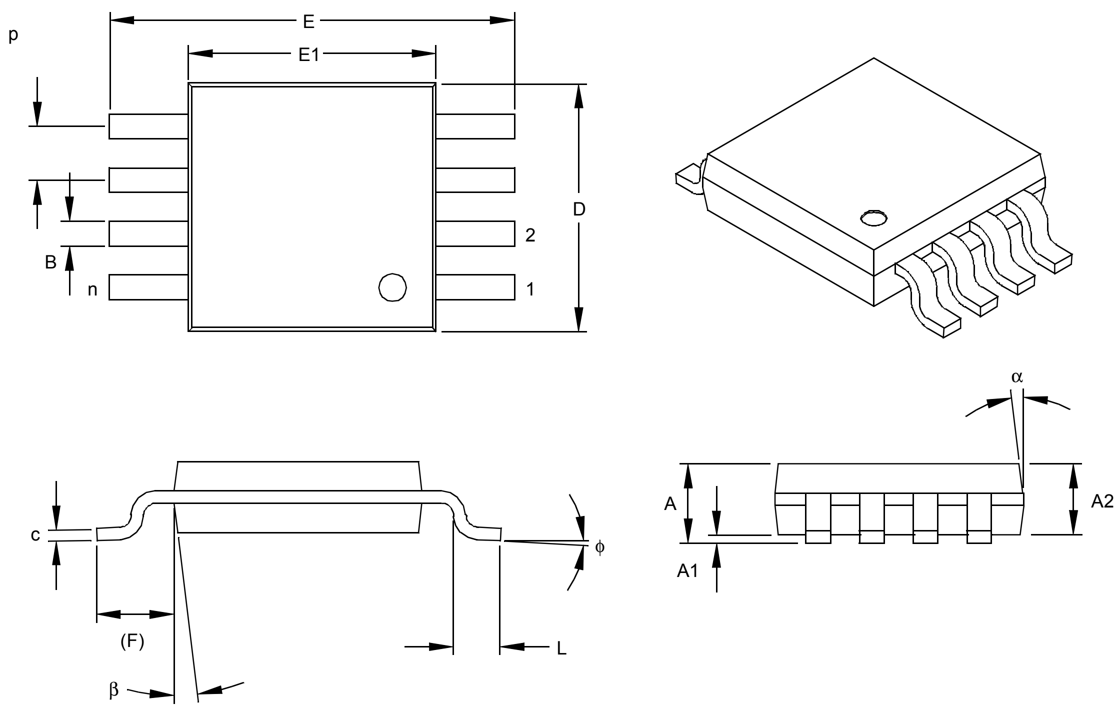


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p		.026			0.65	
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	.5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

*Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed. 010" (0.254mm) per side.

Drawing No. C04-111

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013001

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP6002: 1 MHz, Low Power Op Amp MCP6002T:1 MHz, Low Power Op Amp
Temperature Range:	I = -40°C to +85°C
Package:	MS = Plastic MSOP, 8-lead P = Plastic DIP (300 mil Body), 8-lead SN = Plastic SOIC, (150 mil Body), 8-lead

Examples:

a) MCP6002-I/MS: 8LD MSOP Industrial

b) MCP6002-I/P: 8 LD PDIP Industrial

c) MCP6002-I/SN: 8LD SOIC Industrial

d) MCP6002T-I/MS: 8LD MSOP Industrial, Tape and Reel

e) MCP6002T-I/SN: 8LD SOIC Industrial, Tape and Reel

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