

1 MHz Bandwidth Low Power Op Amp

Features

- Available in SC-70-5 and SOT-23-5 packages
- 1 MHz Gain Bandwidth Product (typ.)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 5.5V
- Supply Current: $I_Q = 100 \mu\text{A}$ (typ.)
- 90° Phase Margin (typ.)
- Industrial Temperature Range: -40°C to +85°C
- Available in Single, Dual and Quad Packages

Applications

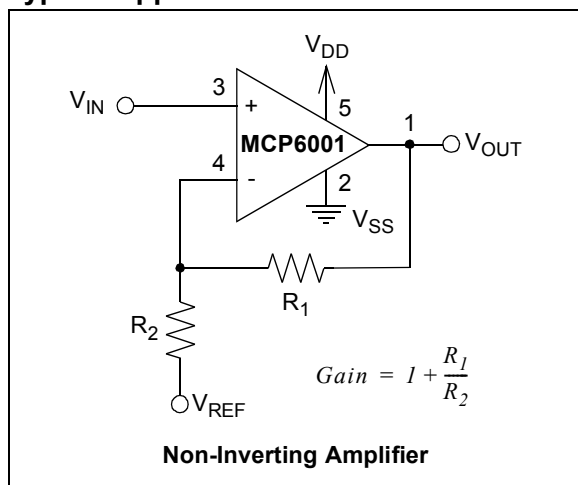
- Portable Equipment
- Photodiode Pre-amps
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Available Tools

Spice Macromodels (at www.microchip.com)

FilterLab[®] Software (at www.microchip.com)

Typical Application

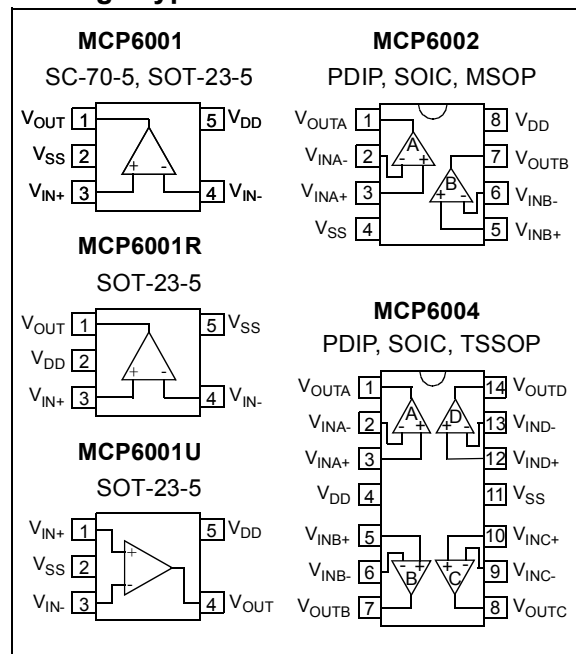


Description

The Microchip Technology Inc. MCP6001/2/4 family of operational amplifiers (op amps) is specifically designed for general-purpose applications. This family has a 1 MHz gain bandwidth product and 90° phase margin (typ.). It also maintains 45° phase margin (typ.) with 500 pF capacitive load. This family operates from a single supply voltage as low as 1.8V, while drawing 100 μA (typ.) quiescent current. In addition, the MCP6001/2/4 supports rail-to-rail input and output swing, with a common mode input voltage range of $V_{DD} + 300 \text{ mV}$ to $V_{SS} - 300 \text{ mV}$. This family of operational amplifiers is designed with Microchip's advanced CMOS process.

The MCP6001/2/4 family is specified from -40°C to +85°C, with a power supply range of 1.8V to 5.5V.

Package Types



MCP6001/2/4

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$	7.0V
All Inputs and Outputs	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage	$ V_{DD} - V_{SS} $
Output Short Circuit Current	continuous
Current at Input Pins	± 2 mA
Current at Output and Supply Pins	± 30 mA
Storage Temperature	-65°C to $+150^{\circ}\text{C}$
Junction Temp. (T_J)	$+150^{\circ}\text{C}$
ESD Protection On All Pins (HBM/MM)	≥ 4 kV/200V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
$V_{IN+}/V_{INA+}/V_{INB+}/V_{INC+}/V_{IND+}$	Non-inverting Inputs
$V_{IN-}/V_{INA-}/V_{INB-}/V_{INC-}/V_{IND-}$	Inverting Inputs
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
$V_{OUT}/V_{OUTA}/V_{OUTB}/V_{OUTC}/V_{OUTD}$	Outputs

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = 25^{\circ}\text{C}$, $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$, and $V_{OUT} \sim V_{DD}/2$.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-7.0	—	+7.0	mV	$V_{CM} = V_{SS}$
Input Offset Voltage Drift with Temperature	$\Delta V_{OS}/\Delta T$	—	± 2.0	—	$\mu\text{V}/^{\circ}\text{C}$	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CM} = V_{SS}$
Power Supply Rejection	PSRR	—	86	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current	I_B	—	± 1.0	—	pA	
Input Bias Current	I_B	—	19	—	pA	$T_A = +85^{\circ}\text{C}$
Input Offset Current	I_{OS}	—	± 1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	$10^{13} 6$	—	ΩpF	
Differential Input Impedance	Z_{DIFF}	—	$10^{13} 3$	—	ΩpF	
Common Mode						
Common Mode Input Range	V_{CMR}	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	
Common Mode Rejection Ratio	CMRR	60	76	—	dB	$V_{CM} = -0.3\text{V}$ to 5.3V , $V_{DD} = 5\text{V}$
Open Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	88	112	—	dB	$V_{OUT} = 0.3\text{V}$ to $V_{DD} - 0.3\text{V}$, $V_{CM} = V_{SS}$
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	$V_{SS} + 25$	—	$V_{DD} - 25$	mV	$V_{DD} = 5.5\text{V}$
Output Short-Circuit Current	I_{SC}	—	± 23	—	mA	$V_{DD} = 5.5\text{V}$
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	50	100	170	μA	$I_O = 0$, $V_{DD} = 5.5\text{V}$, $V_{CM} = 5\text{V}$

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = 25^\circ\text{C}$, $V_{DD} = +5.0\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \sim V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$, and $C_L = 60\text{ pF}$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin at Unity Gain	PH	—	90	—	degrees	G = +1
Slew Rate	SR	—	0.6	—	V/ μs	
Noise						
Input Noise Voltage	E_{ni}	—	6.0	—	$\mu\text{Vp-p}$	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	28	—	nV/ $\sqrt{\text{Hz}}$	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/ $\sqrt{\text{Hz}}$	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$, and $V_{SS} = \text{GND}$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	$^\circ\text{C}$	
Operating Temperature Range	T_A	-40	—	+125	$^\circ\text{C}$	(Note)
Storage Temperature Range	T_A	-65	—	+150	$^\circ\text{C}$	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	$^\circ\text{C/W}$	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	$^\circ\text{C/W}$	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	$^\circ\text{C/W}$	
Thermal Resistance, 8L-SOIC (150 mil)	θ_{JA}	—	163	—	$^\circ\text{C/W}$	
Thermal Resistance, 8L-SOIC (208 mil)	θ_{JA}	—	118	—	$^\circ\text{C/W}$	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	$^\circ\text{C/W}$	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	$^\circ\text{C/W}$	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	$^\circ\text{C/W}$	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	$^\circ\text{C/W}$	

Note: The MCP6001/2/4 operates over this extended temperature range, but with reduced performance. In any case, the Junction Temperature (T_J) must not exceed the Absolute Maximum specification of $+150^\circ\text{C}$.

MCP6001/2/4

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = 25^\circ\text{C}$, $V_{DD} = +5.0\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \sim V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$, and $C_L = 60\text{ pF}$.

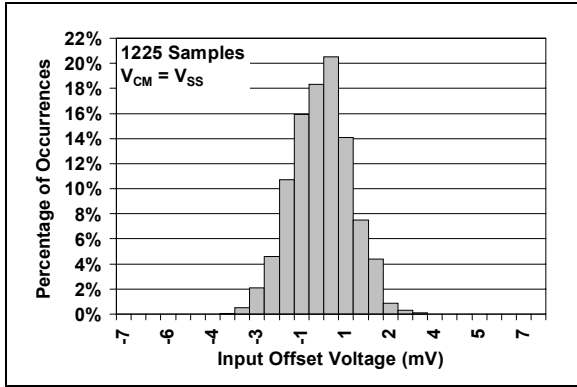


FIGURE 2-1: Histogram of Input Offset Voltage with $V_{CM} = V_{SS}$.

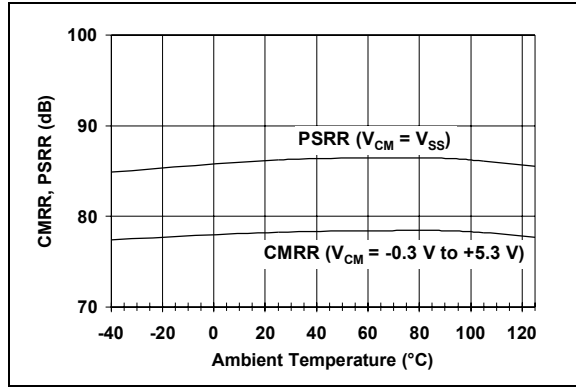


FIGURE 2-4: Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Temperature.

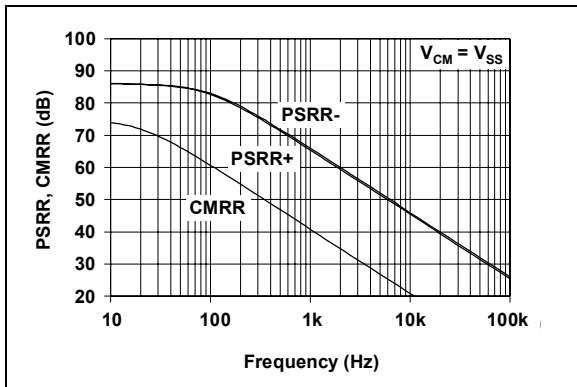


FIGURE 2-2: Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Frequency.

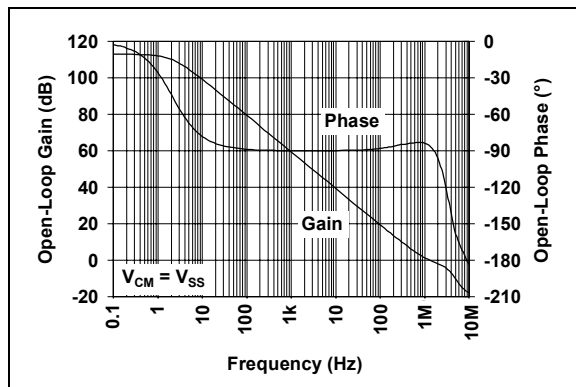


FIGURE 2-5: Open-Loop Gain, Phase vs. Frequency.

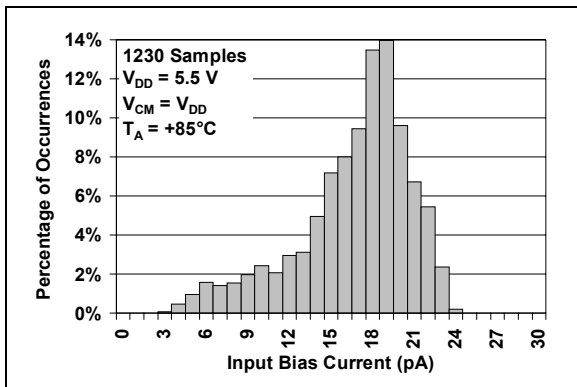


FIGURE 2-3: Input Bias Current Histogram with Temperature = 85°C .

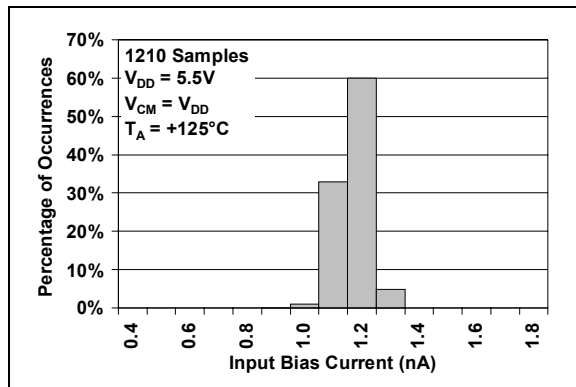


FIGURE 2-6: Input Bias Current Histogram with Temperature = 125°C .

Note: Unless otherwise indicated, $T_A = 25^\circ\text{C}$, $V_{DD} = +5.0\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \sim V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$, and $C_L = 60\text{ pF}$.

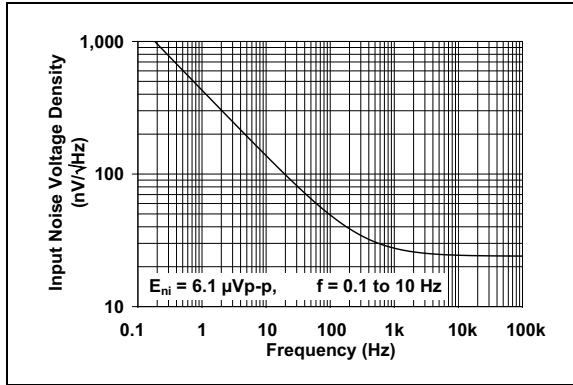


FIGURE 2-7: Input Noise Voltage Density vs. Frequency.

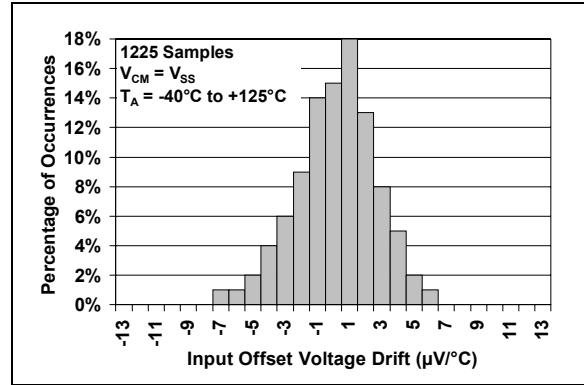


FIGURE 2-10: Histogram of Input Offset Voltage Drift with $V_{CM} = V_{SS}$.

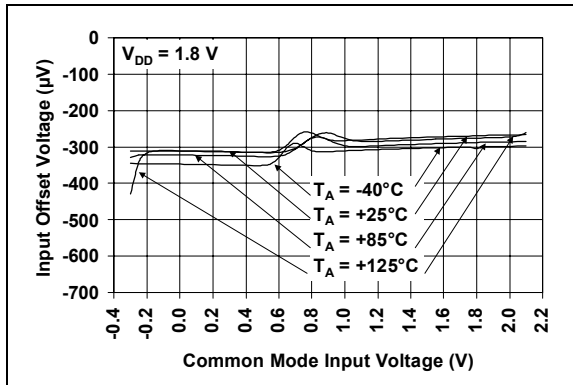


FIGURE 2-8: Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with $V_{DD} = 1.8\text{V}$.

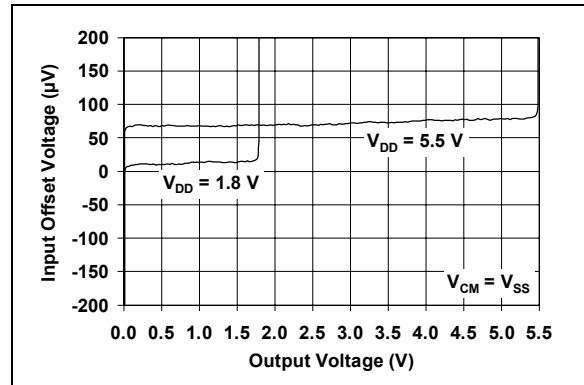


FIGURE 2-11: Input Offset Voltage vs. Output Voltage vs. Power Supply Voltage.

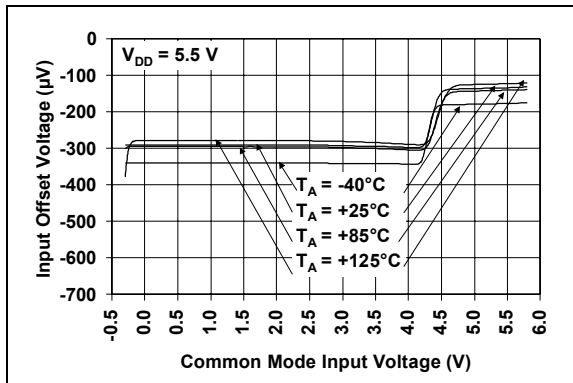


FIGURE 2-9: Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with $V_{DD} = 5.5\text{V}$.

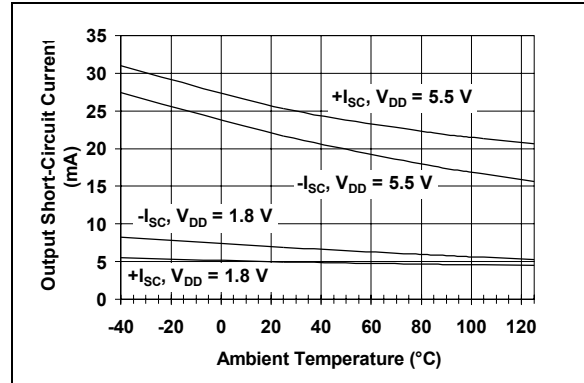


FIGURE 2-12: Output Short-Circuit Current vs. Temperature vs. Power Supply Voltage.

MCP6001/2/4

Note: Unless otherwise indicated, $T_A = 25^\circ\text{C}$, $V_{DD} = +5.0\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \sim V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$, and $C_L = 60\text{ pF}$.

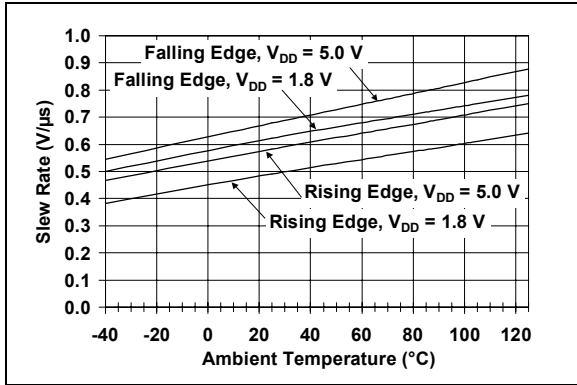


FIGURE 2-13: Slew Rate vs. Temperature vs. Power Supply Voltage.

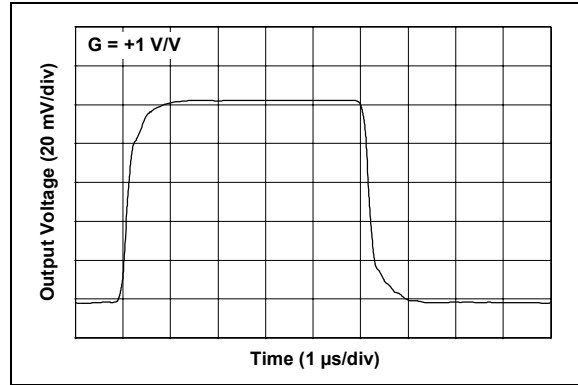


FIGURE 2-16: Small Signal Non-Inverting Pulse Response.

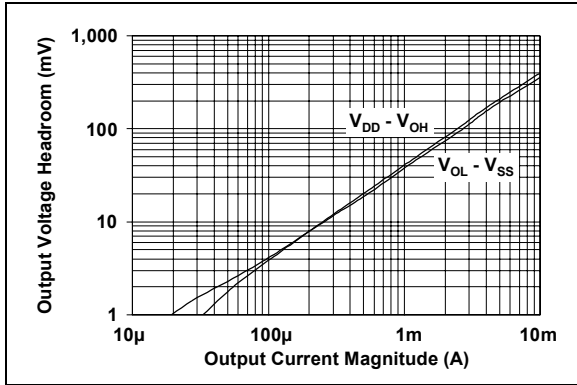


FIGURE 2-14: Output Voltage Headroom vs. Output Current Magnitude.

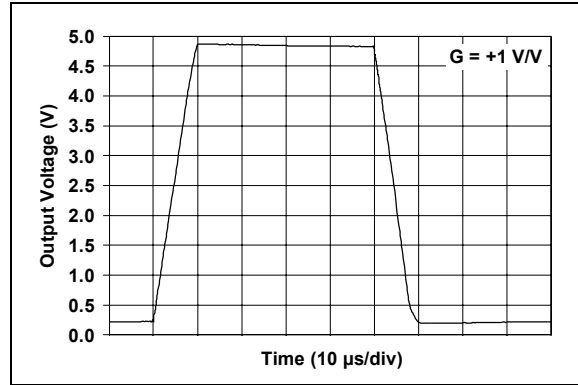


FIGURE 2-17: Large Signal Non-Inverting Pulse Response.

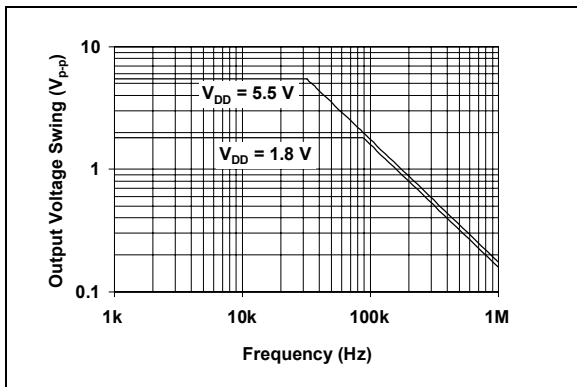


FIGURE 2-15: Output Voltage Swing vs. Frequency vs. Power Supply Voltage.

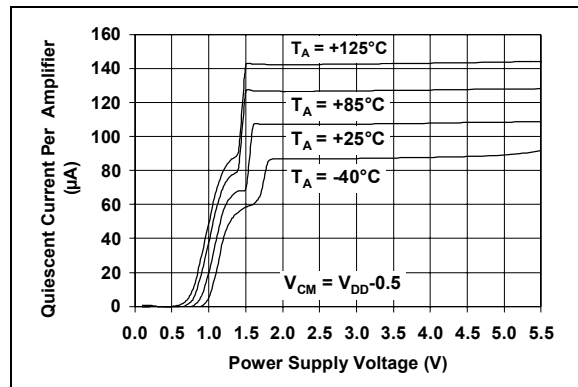


FIGURE 2-18: Quiescent Current vs. Power Supply Voltage vs. Temperature.

3.0 APPLICATION INFORMATION

The MCP6001/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low cost, low power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6001/2/4 ideal for battery-powered applications. This device has high phase margin which makes it stable for larger capacitive load applications.

3.1 Rail-to-Rail Input

The input stage of the MCP6001/2/4 op amp uses two differential input stages in parallel; one operates at low common mode input voltage (V_{CM}) and the other at high V_{CM} . With this topology, the device operates with V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS} . The Input Offset Voltage is measured at $V_{CM} = V_{SS} - 300$ mV and $V_{DD} + 300$ mV to ensure proper operation.

3.2 Rail-to-Rail Output

The output voltage range of the MCP6001/2/4 op amp is $V_{DD} - 25$ mV (min.) and $V_{SS} + 25$ mV (max.) when $R_L = 10$ k Ω is connected to $V_{DD}/2$ and $V_{DD} = 5.5$ V. Refer to Figure 2-14 for more information.

3.3 Phase Reversal and Input Voltage

The MCP6001/2/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 3-1 shows the input voltage exceeding the supply voltage without any phase reversal. This graph is created with a non-inverting circuit configuration in a gain of +2 V/V.

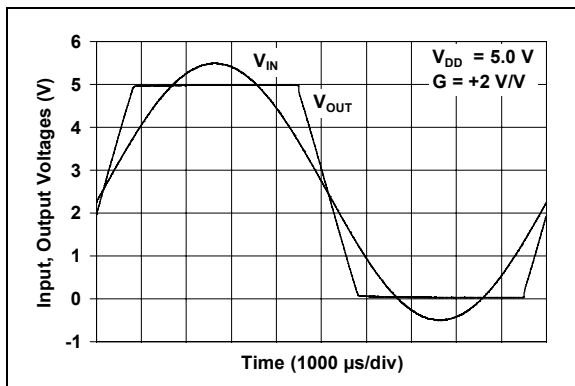


FIGURE 3-1: The MCP6001/2/4 Shows No Phase Reversal.

The maximum operating V_{CM} that can be applied to the inputs is $V_{SS} - 300$ mV (min.) and $V_{DD} + 300$ mV (max.). Input voltages that exceed this absolute maximum rating can cause excessive current to flow into or out of the input pins. Current beyond ± 2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor, as shown in Figure 3-2.

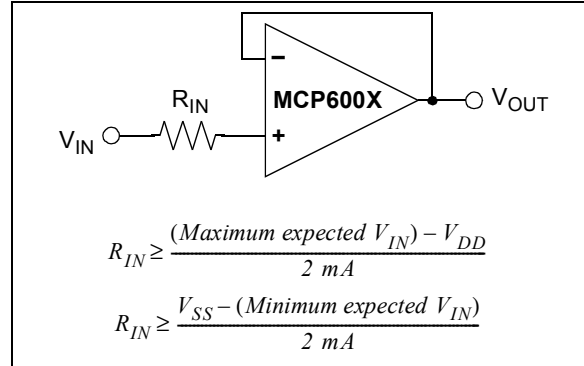


FIGURE 3-2: Input Current Limiting Resistor (R_{IN}).

3.4 Capacitive Load and Stability

Capacitive loads can cause stability problems with voltage feedback op amps. A buffer configuration ($G = +1$) is the most sensitive to capacitive loads. Figure 3-3 shows how increasing the load capacitance will decrease the phase margin and reduce the bandwidth. A phase margin of 60° has minimum overshoot, however, a 45° has over 25% overshoot on the step response.

The MCP6001/2/4 op amp has a phase margin of 90° (typ.) under the specified conditions in the AC electrical specifications table. The device maintains greater than 60° phase margin (typ.), with 200 pF capacitive load. The device also maintains stability at 45° phase margin (typ.), with 500 pF capacitive load, as shown in Figure 3-3.

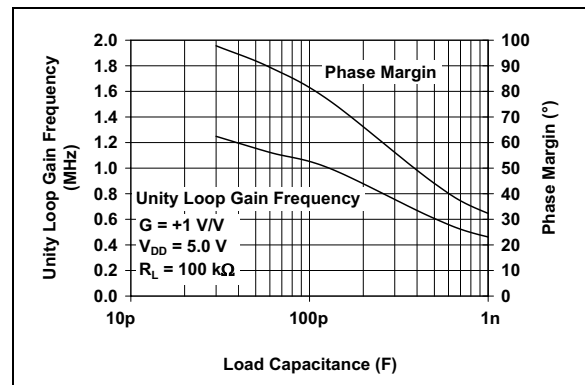


FIGURE 3-3: Gain Bandwidth Product, Phase Margin vs. Load Capacitance with Unity Gain.

When the MCP6001/2/4 op amp is required to drive large capacitive loads, a series resistor (R_{ISO}) at the output of the amplifier improves the phase margin. This resistor makes the output load resistive at higher frequencies. However, the bandwidth reduction caused by the capacitive load is not changed. To select R_{ISO} , use the SPICE macro model starting with 1 k Ω and adjust the resistor until the frequency response shows low peaking.

MCP6001/2/4

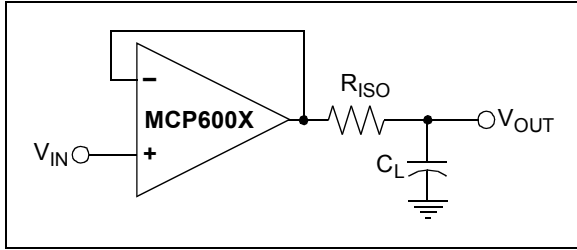


FIGURE 3-4: Amplifier Circuit for Heavy Capacitive Loads.

3.5 Application Circuits

3.5.1 UNITY GAIN BUFFER

The rail-to-rail input and output capability of the MCP6001/2/4 op amp is ideal for unity gain buffer applications. The low quiescent current and wide bandwidth makes the device suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 3-5.

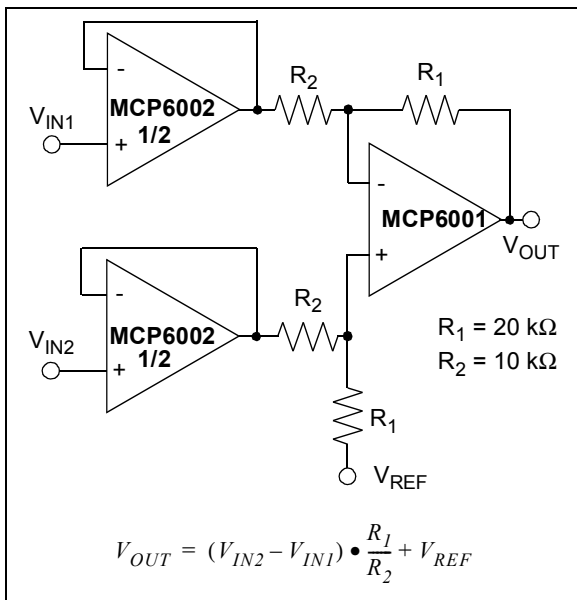


FIGURE 3-5: Instrumentation Amplifier with Unity Gain Buffer Inputs.

3.5.2 ACTIVE LOW-PASS FILTER

The MCP6001/2/4 op amp's low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistances increase, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

It is possible to have a filter cutoff frequency as high as 1/10th of the op amp bandwidth, or 100 kHz. Figure 3-6 shows a second-order butterworth filter with 100 kHz cutoff frequency and a gain of +1 V/V.

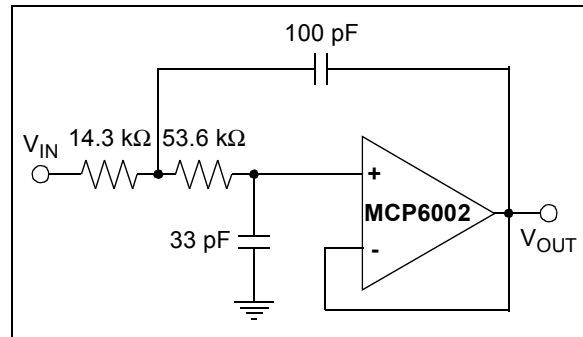


FIGURE 3-6: Active Second Order Low Pass Filter.

The component values in Figure 3-6 are selected using Microchip's FilterLab[®] software, which is a tool that simplifies active filter design. This tool provides schematic diagrams of filter circuits (up to the 8th order) with resistor and capacitor values, and displays the frequency response.

FilterLab software can be downloaded, free of charge, from the Microchip web site (www.microchip.com).

3.5.3 PEAK DETECTOR

The MCP6001/2/4 op amp has a high input impedance, rail-to-rail input and output and low input bias current, which makes this device suitable for a peak detector application. Figure 3-7 shows a peak detector circuit with clear and sample switches. The peak-detection cycle uses a clock (CLK), as shown in Figure 3-7.

At the rising edge of CLK, Sample Switch closes to begin sampling. The peak voltage stored on C_1 is sampled to C_2 for a sample time defined by t_{SAMP} . At the end of the sample time (falling edge of Sample Signal), Clear Signal goes high and closes the Clear Switch. When the Clear Switch closes, C_1 discharges through R_1 for a time defined by t_{CLEAR} . At the end of the clear time (falling edge of Clear Signal), op amp A begins to store the peak value of V_{IN} on C_1 for a time defined by t_{DETECT} .

In order to define the t_{SAMP} and t_{CLEAR} , it is necessary to determine the capacitor charging and discharging period. The capacitor charging time is limited by the amplifier source current, while the discharging time (τ) is defined using R_1 ($\tau = R_1 * C_1$). t_{DETECT} is the time that the input signal is sampled on C_1 , and is dependent on the input voltage change frequency.

The op amp output current limit, and the size of the storage capacitors (both C_1 and C_2), could create slewing limitations as the input voltage (V_{IN}) increases. Current through a capacitor is dependent on the size of the capacitor and the rate of voltage change. From this

relationship, the rate of voltage change or the slew rate can be determined. For example, with op amp short-circuit current of $I_{SC} = 25\text{mA}$ and load capacitor of $C_1 = 0.1\ \mu\text{F}$, then:

EQUATION

$$I_{SC} = C_1 \times \frac{dV_{C1}}{dt}$$

$$\frac{dV_{C1}}{dt} = \frac{I_{SC}}{C_1}$$

$$= \frac{25\text{mA}}{0.1\ \mu\text{F}}$$

$$\frac{dV_{C1}}{dt} = \frac{250\text{mV}}{\mu\text{s}}$$

This voltage change rate is less than the MCP6001/2/4 slew rate of $600\text{mV}/\mu\text{s}$. When the input voltage swings below the voltage across C_1 , D_1 becomes reverse-biased, which opens the feedback loop and rails the amplifier. When the input voltage increases, the amplifier recovers at its slew rate. Based on the rate of voltage change shown in the above equation, it takes an extended period of time to charge a $0.1\ \mu\text{F}$ capacitor. The capacitors need to be selected so that the circuit is not limited by the amplifier slew rate. Therefore, the capacitors should be less than $40\ \mu\text{F}$ and a stabilizing resistor (R_{ISO}) needs to be properly selected. Refer to Section 3.4, "Capacitive Load and Stability", for op amp stability.

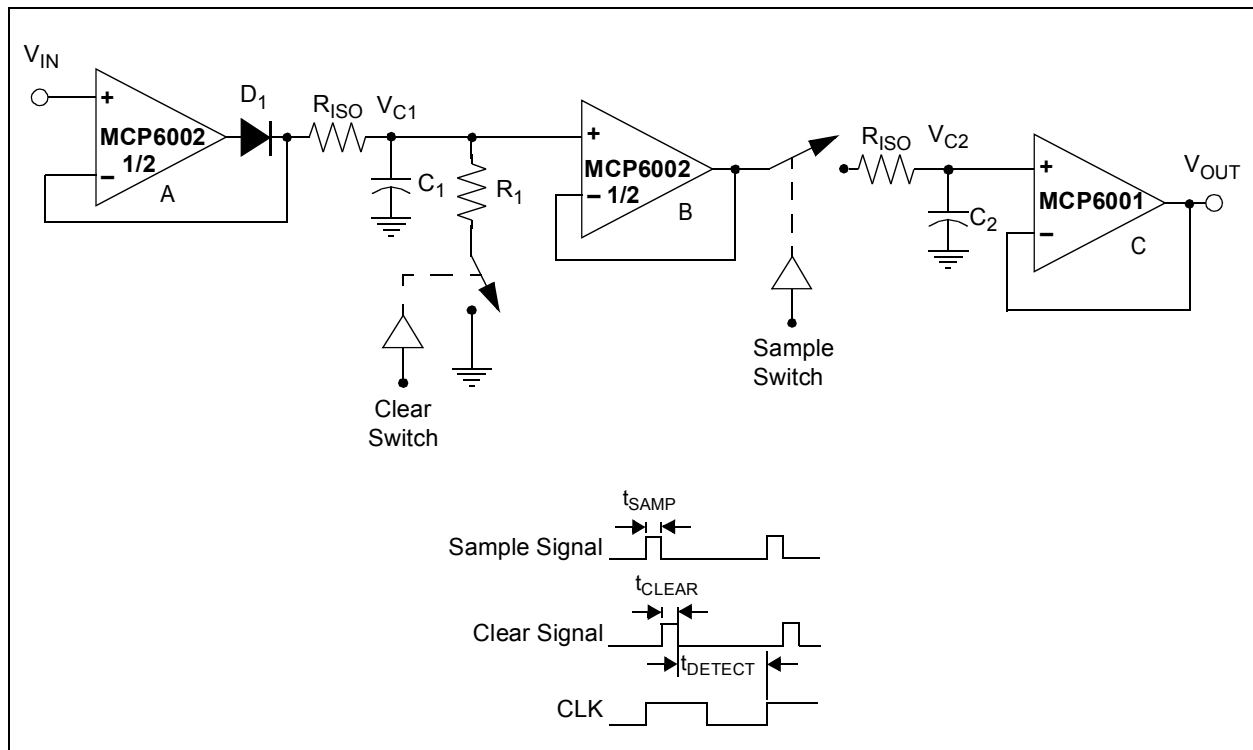


FIGURE 3-7: Peak Detector with Clear and Sample CMOS Analog Switches.

MCP6001/2/4

4.0 SPICE MACRO MODEL

The Spice macro model for the MCP6001/2/4 op amp simulates the typical amplifier performance of: offset voltage, DC power supply rejection, input capacitance, DC common mode rejection, open-loop gain over frequency, phase margin, output swing, DC power supply current, power supply current change with supply voltage, input common mode range, output voltage range vs. load and input voltage noise.

The listing for this macro model is shown on the next page. The most recent revision of the model can be downloaded from Microchip's web site at www.microchip.com.

Software License Agreement

The software supplied herewith by Microchip Technology Incorporated (the "Company") is intended and supplied to you, the Company's customer, for use solely and exclusively on Microchip products manufactured by the company.

The software is owned by the Company and/or its supplier, and is protected under applicable copyright laws. All rights are reserved. Any use in violation of the foregoing restrictions may subject the user to criminal sanctions under applicable laws, as well as to civil liability for the breach of the terms and conditions of this license.

THIS SOFTWARE IS PROVIDED IN AN "AS IS" CONDITION. NO WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE APPLY TO THIS SOFTWARE. THE COMPANY SHALL NOT, IN ANY CIRCUMSTANCES, BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, FOR ANY REASON WHATSOEVER.

```
.SUBCKT MCP6001 1 2 3 4 5
*      | | | | |
*      | | | | Output
*      | | | Negative Supply
*      | | Positive Supply
*      | Inverting Input
*      Non-inverting Input
*
* Macromodel for the MCP6001/2/4 op amp family:
*   MCP6001 (single)
*   MCP6002 (dual)
*   MCP6004 (quad)
*
* Revision History:
*   REV A: 21-Jun-02, KEB (created model)
*   REV B: 16-Jul-02, KEB (improved output stage)
*
* Recommendations:
*   Use PSPICE (or SPICE 2G6; other simulators may require translation)
*   For a quick, effective design, use a combination of: data sheet
*   specs, bench testing, and simulations with this macromodel
*   For high impedance circuits, set GMIN=100F in the .OPTIONS
*   statement
*
* Supported:
*   Typical performance at room temperature (25 degrees C)
*   DC, AC, Transient, and Noise analyses.
*   Most specs, including: offsets, DC PSRR, DC CMRR, input impedance,
*   open loop gain, voltage ranges, supply current, ... , etc.
*
* Not Supported:
*   Variation in specs vs. Power Supply Voltage
*   Distortion (detailed non-linear behavior)
*   Temperature analysis
*   Process variation
*   Behavior outside normal operating region
*
* Input Stage
V10 3 10 -300M
R10 10 11 6.90K
R11 10 12 6.90K
C11 11 12 115E-15
C12 1 0 6.00P
E12 1 14 POLY(4) 20 0 21 0 26 0 27 0 1.00M 20.1 20.1 1 1
I12 14 0 1.50P
M12 11 14 15 15 NMI L=2.00U W=42.0U
C13 14 2 3.00P
M14 12 2 15 15 NMI L=2.00U W=42.0U
I14 2 0 500E-15
C14 2 0 6.00P
I15 15 4 50.0U
```

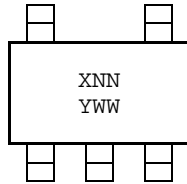
MCP6001/2/4

```
V16 16 4 300M
D16 16 15 DL
V13 3 13 50M
D13 14 13 DL
*
* Noise, PSRR, and CMRR
I20 21 20 423U
D20 20 0 DN1
D21 0 21 DN1
G26 0 26 POLY(1) 3 4 110U -20.0U
R26 26 0 1
G27 0 27 POLY(2) 1 3 2 4 -440U 80.0U 80.0U
R27 27 0 1
*
* Open Loop Gain, Slew Rate
G30 0 30 POLY(1) 12 11 0 1.00K
R30 30 0 1
E31 31 0 POLY(1) 3 4 104 -2.33
D31 30 31 DL
E32 0 32 POLY(1) 3 4 140 -6.07
D32 32 30 DL
G33 0 33 POLY(1) 30 0 0 447
R33 33 0 1
C33 33 0 77.1M
G34 0 34 POLY(1) 33 0 0 1.00
R34 34 0 1.00
C34 34 0 50.2N
G35 0 35 POLY(2) 34 0 33 34 0 1.00 3.00
R35 35 0 1.00
*
* Output Stage
G50 0 50 POLY(1) 57 5 0 2.00
D51 50 51 DL
R51 51 0 1K
D52 52 50 DL
R52 52 0 1K
G53 3 0 POLY(1) 51 0 50.0U 1M
G54 0 4 POLY(1) 52 0 50.0U -1M
E55 55 0 POLY(2) 3 0 51 0 -10M 1 -40.0M
D55 57 55 DLS
E56 56 0 POLY(2) 4 0 52 0 10M 1 -40.0M
D56 56 57 DLS
G57 0 57 POLY(3) 3 0 4 0 35 0 0 1.00M 1.00M 2.00M
R57 57 0 500
R58 57 5 500M
C58 5 0 2.00P
*
* Models
.MODEL NMI NMOS
.MODEL DL D N=1 IS=1F
.MODEL DLS D N=10M IS=1F
.MODEL DN1 D IS=1F KF=146E-18 AF=1
*
.ENDS MCP6001
```

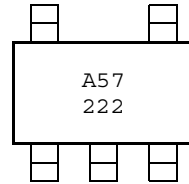
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

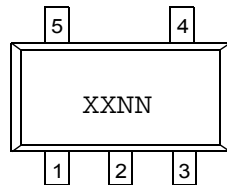
5-Lead SC-70 (MCP6001)



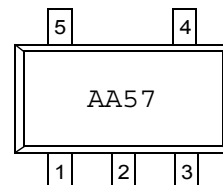
Example:



5-Lead SOT-23 (MCP6001)

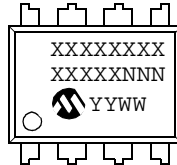


Example:

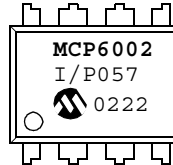


MCP6001 = AANN
MCP6001R = ADNN
MCP6001U = AFNN

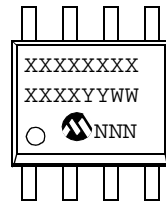
8-Lead PDIP (300 mil)



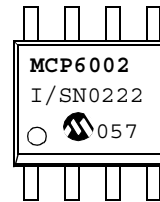
Example:



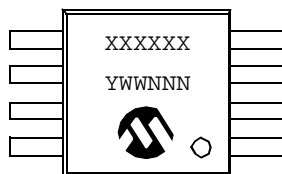
8-Lead SOIC (150 mil)



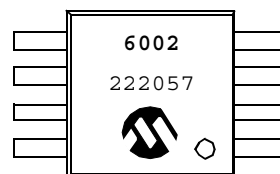
Example:



8-Lead MSOP



Example:



Legend: XX...X Customer specific information*
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code

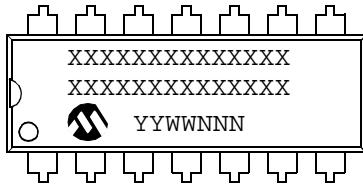
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

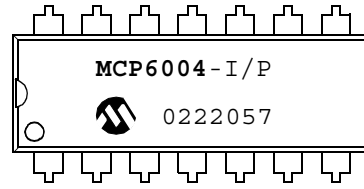
MCP6001/2/4

Package Marking Information (Continued)

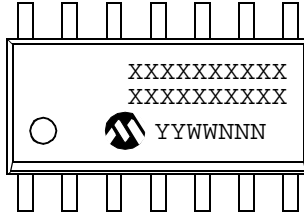
14-Lead PDIP (300 mil) (MCP6004)



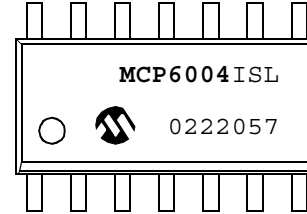
Example:



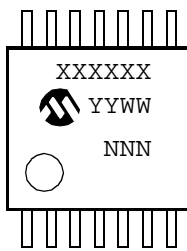
14-Lead SOIC (150 mil) (MCP6004)



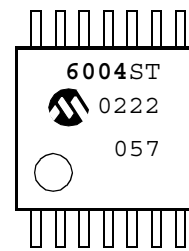
Example:



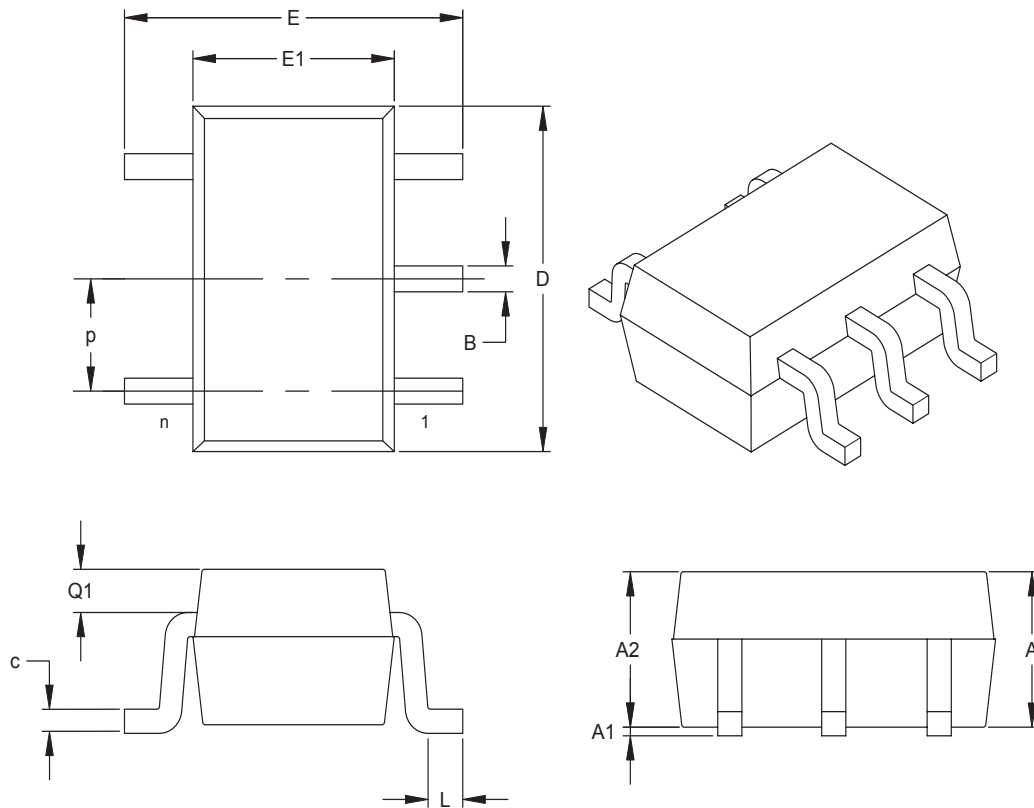
14-Lead TSSOP (MCP6004)



Example:



5-Lead Plastic Package (SC-70)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	5			5		
Pitch	p	.026 (BSC)			0.65 (BSC)		
Overall Height	A	.031		.043	0.80		1.10
Molded Package Thickness	A2	.031		.039	0.80		1.00
Standoff	A1	.000		.004	0.00		0.10
Overall Width	E	.071		.094	1.80		2.40
Molded Package Width	E1	.045		.053	1.15		1.35
Overall Length	D	.071		.087	1.80		2.20
Foot Length	L	.004		.012	0.10		0.30
Top of Molded Pkg to Lead Shoulder	Q1	.004		.016	0.10		0.40
Lead Thickness	c	.004		.007	0.10		0.18
Lead Width	B	.006		.012	0.15		0.30

*Controlling Parameter

Notes:

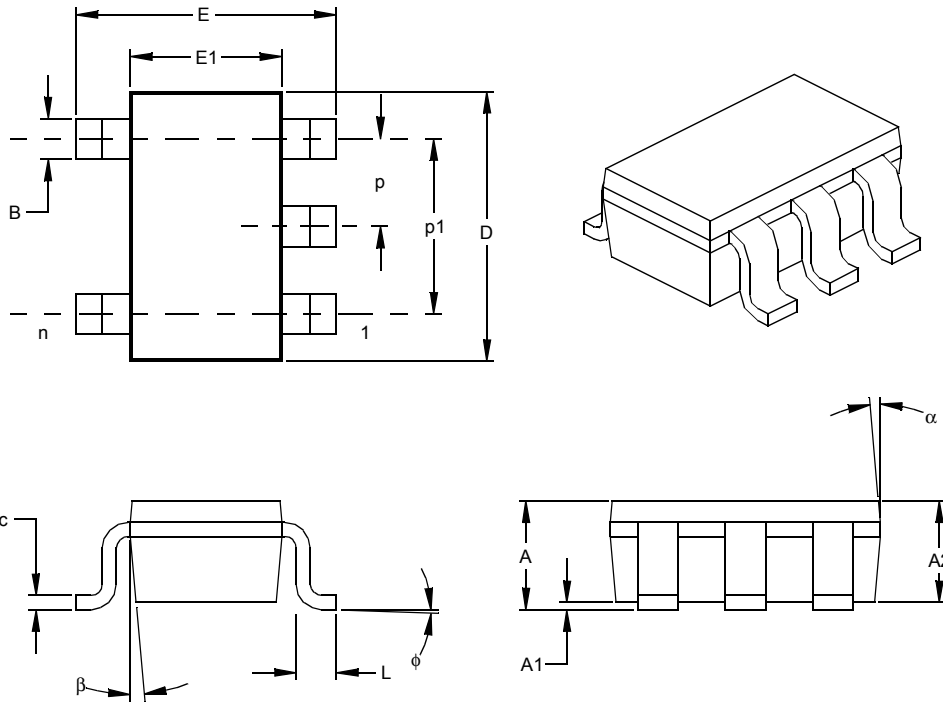
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (EIAJ) Standard: SC-70

Drawing No. C04-061

MCP6001/2/4

5-Lead Plastic Small Outline Transistor (OT) (SOT23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
 § Significant Characteristic

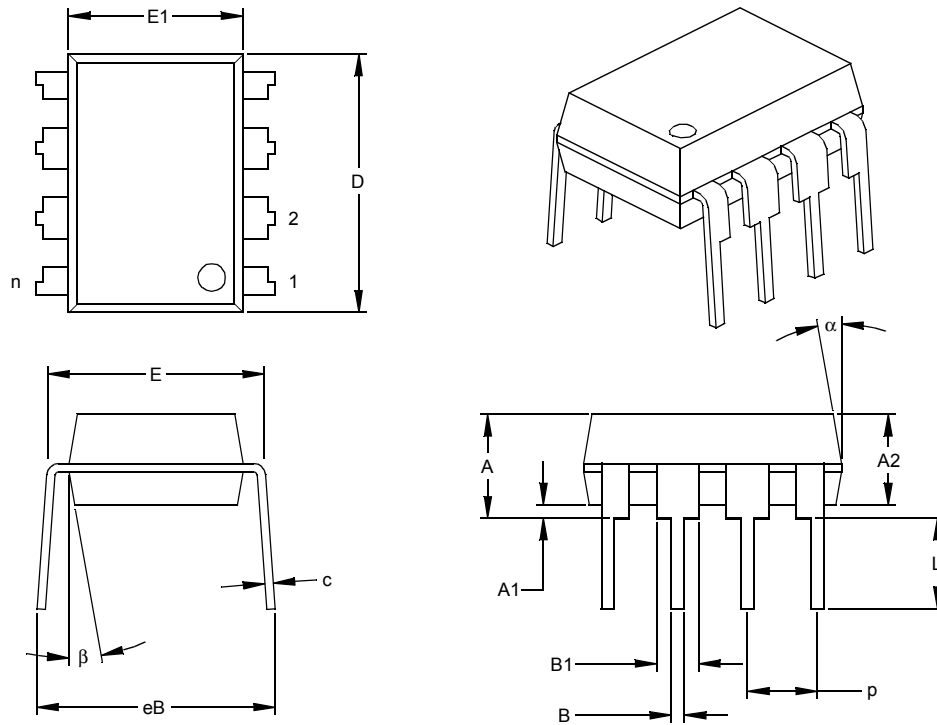
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-178

Drawing No. C04-091

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



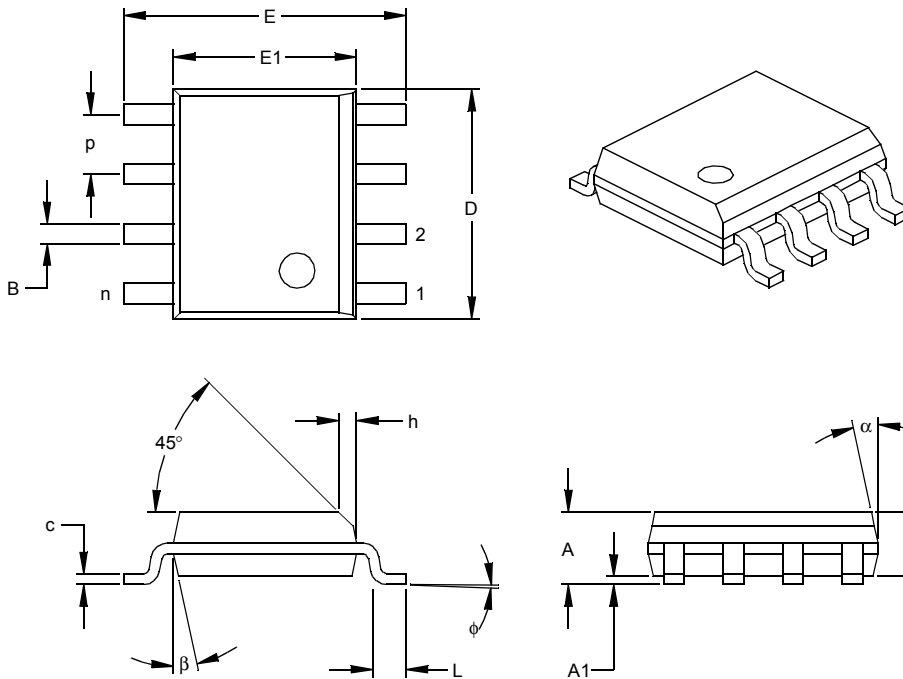
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
 § Significant Characteristic

Notes:
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
 JEDEC Equivalent: MS-001
 Drawing No. C04-018

MCP6001/2/4

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

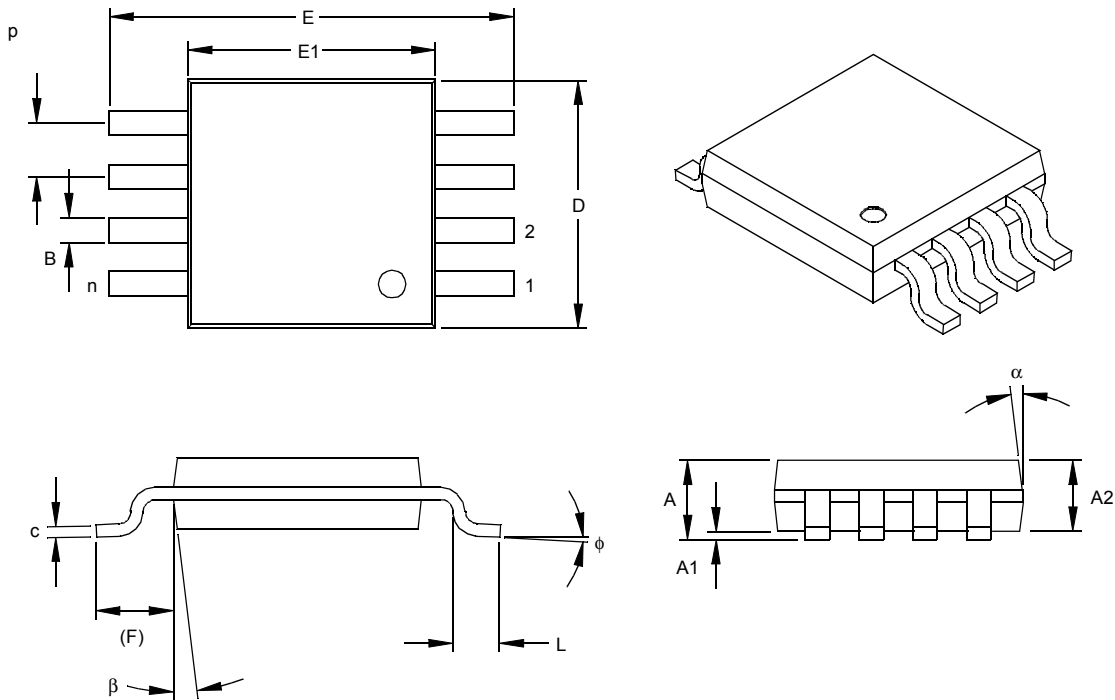


Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
 § Significant Characteristic

Notes:
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
 JEDEC Equivalent: MS-012
 Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p	.026			0.65		
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

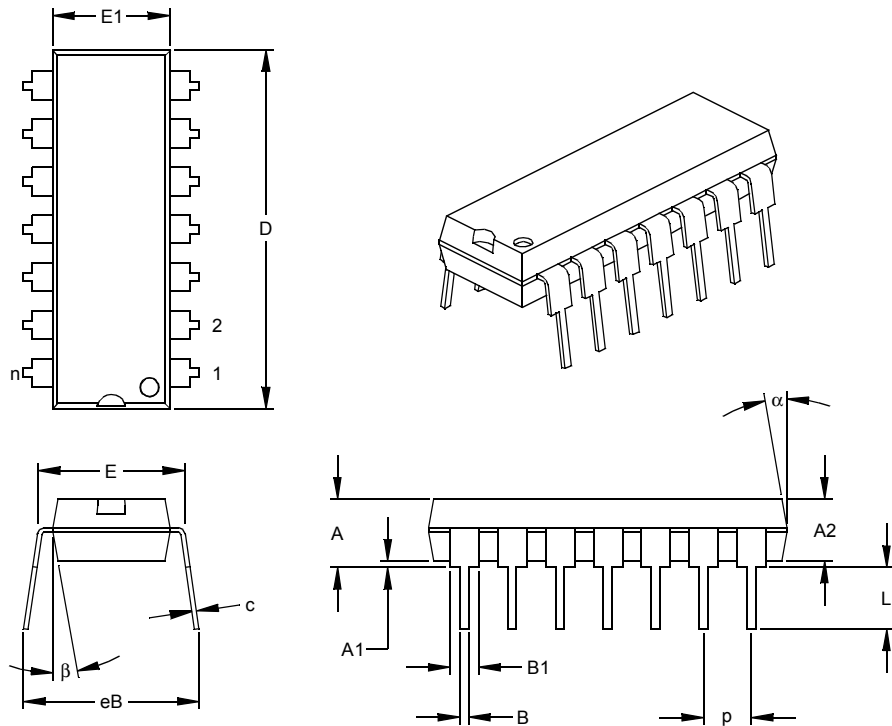
*Controlling Parameter
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
 Drawing No. C04-111

MCP6001/2/4

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

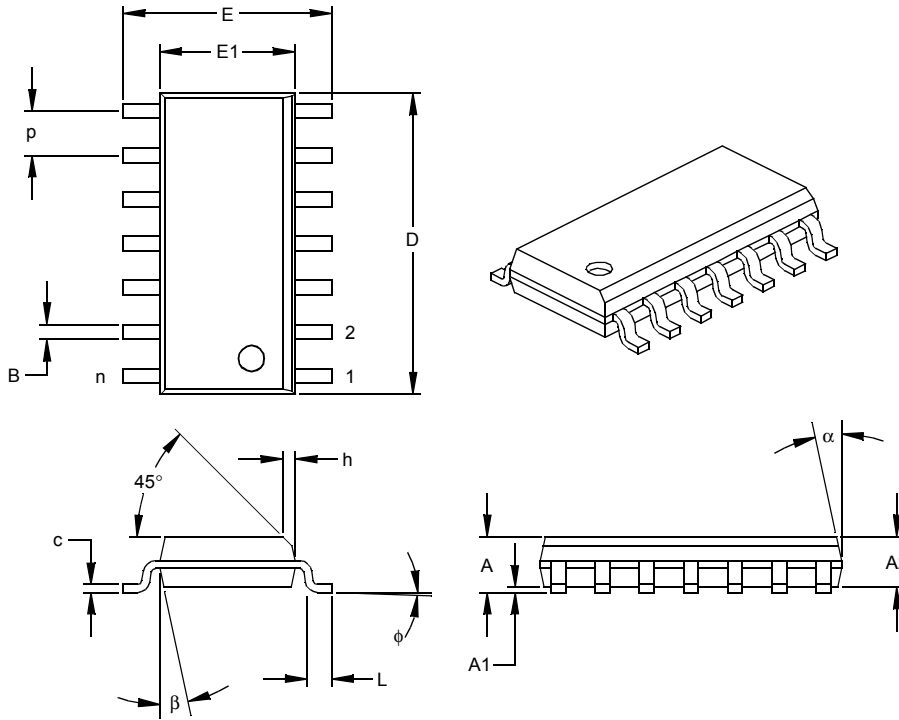
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
 § Significant Characteristic

Notes:

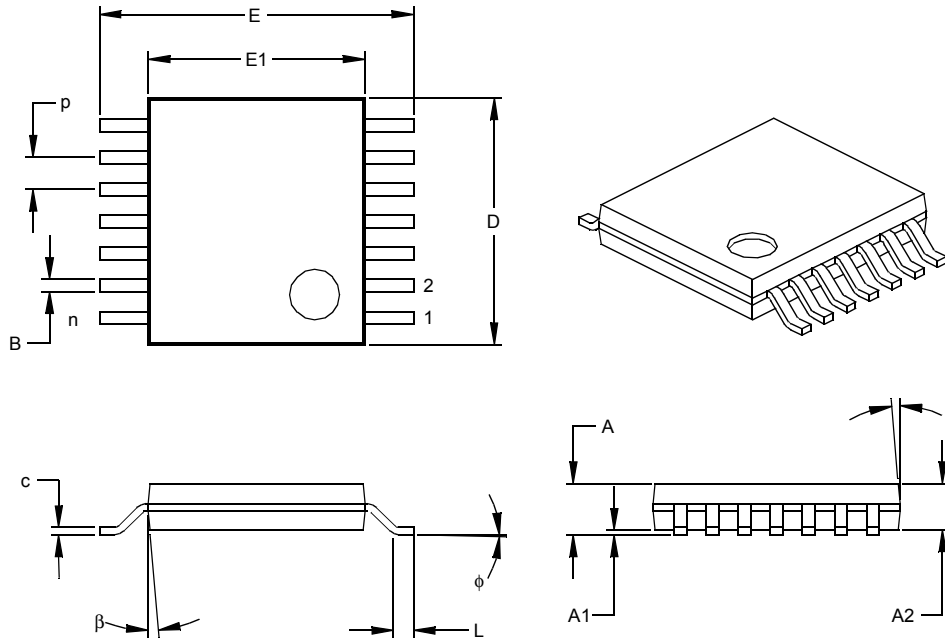
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-065

MCP6001/2/4

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-087

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>
Device	Temperature Range	Package
Device:	MCP6001T:	1 MHz Bandwidth, Low Power Op Amp (Tape and Reel)(SC-70, SOT-23)
	MCP6001RT:	1 MHz Bandwidth, Low Power Op Amp (Tape and Reel)(SOT-23)
	MCP6001UT:	1 MHz Bandwidth, Low Power Op Amp (Tape and Reel)(SOT-23)
	MCP6002:	1 MHz Bandwidth, Low Power Op Amp
	MCP6002T:	1 MHz Bandwidth, Low Power Op Amp (Tape and Reel)(SOIC, MSOP)
	MCP6004:	1 MHz Bandwidth, Low Power Op Amp
	MCP6004T:	1 MHz, Bandwidth Low Power Op Amp (Tape and Reel)(SOIC, MSOP)
Temperature Range:	I	= -40°C to +85°C
Package:	LT	= Plastic Package (SC-70), 5-lead (MCP6001 only)
	OT	= Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6001, MCP6001R, MCP6001U)
	MS	= Plastic MSOP, 8-lead
	P	= Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN	= Plastic SOIC, (150 mil Body), 8-lead
	SL	= Plastic SOIC (150 mil Body), 14-lead
	ST	= Plastic TSSOP (4.4mm Body), 14-lead

Examples:

a) MCP6001T-I/LT: 5LD SC-70, Tape and Reel.
 b) MCP6001T-I/OT: 5LD SOT-23, Tape and Reel.
 c) MCP6001RT-I/OT: 5LD SOT-23, Tape and Reel.
 d) MCP6001UT-I/OT: 5LD SOT-23, Tape and Reel.

a) MCP6002-I/MS: 8LD MSOP.
 b) MCP6002-I/P: 8LD PDIP.
 c) MCP6002-I/SN: 8LD SOIC.
 d) MCP6002T-I/MS: 8LD MSOP, Tape and Reel.
 e) MCP6002T-I/SN: 8LD SOIC, Tape and Reel.

a) MCP6004-I/P: 14LD PDIP.
 b) MCP6004-I/SL: 14LD SOIC.
 c) MCP6004-I/ST: 14LD TSSOP.
 d) MCP6004T-I/SL: 14LD SOIC Tape and Reel.
 e) MCP6004T-I/ST: 14LD TSSOP Tape and Reel.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

MCP6001/2/4

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, KEELOQ, MPLAB, PIC, PICmicro, PICSTART and PRO MATE are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


FilterLab, microID, MXDEV, MXLAB, PICMASTER, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

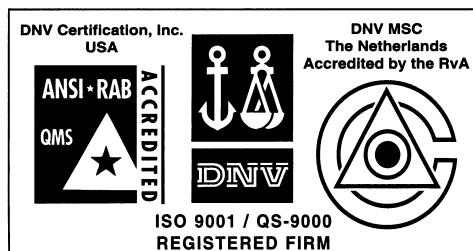
dsPIC, dsPICDEM.net, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICC, PICDEM, PICDEM.net, rFPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



MICROCHIP

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Rocky Mountain

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-4338

Atlanta

3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034 Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Hong Kong SAR

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380 Fax: 86-755-82966626

China - Qingdao

Rm. B503, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Microchip Technology (Barbados) Inc.,
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria

Microchip Technology Austria GmbH
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Microchip Ltd.
505 Eskdale Road
Winkersley Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

12/05/02