# TDA8025

## IC card interface

Rev. 01 — 6 April 2009 Product data sheet



## 1. General description

The TDA8025 is a cost-effective analog interface for asynchronous smart cards operating at 3 V, 1.8 V or optionally, 1.2 V. Using few external components, the TDA8025 provides integrated supply, protection and control functions for a range of applications.

## 2. Features

- Integrated circuit smart card interface
- 3 V, 1.8 V or 1.2 V smart card supply
- Low power consumption in inactive mode
- Three protected, half duplex, bidirectional buffered input/output lines (C4, C7 and C8)
- $V_{CC}$ regulation:
  - 3 V, 1.8 V or optionally 1.2 V at ± 5 % using one 220 nF and one 470 nF low ESR multilayer ceramic capacitor.
  - Current pulse handling for pulses of 40 nAs at $V_{CC}$ = 3 V, 15 nAs at $V_{CC}$ = 1.8 V or $V_{CC}$ = 1.2 V up to 20 MHz
- Thermal and short-circuit protection for all card contacts
- Automatic activation and deactivation sequences triggered by short-circuit, card take-off, overheating, falling $V_{DD(INTF)}$ and $V_{DD(INTREGD)}$
- Enhanced card-side ElectroStatic Discharge (ESD) protection of > 6 kV
- Clock signal using the internal oscillator or an external crystal (≤ 26 MHz) connected to pin XTAL1
- Card clock generation up to 20 MHz with synchronous frequency changes of $f_{xtal}$, $\frac{1}{2}$ $f_{xtal}$, $\frac{1}{4}$ $f_{xtal}$ or $\frac{1}{8}$ $f_{xtal}$ using pins CLKDIV1 and CLKDIV2
- Non-inverted control of pin RST using pin RSTIN
- NDS certified
- Supply supervisors during power on and off:
  - $V_{DD(INTREGD)}$ using a fixed threshold
  - $V_{DD(INTF)}$ using resistor bridge threshold adjustment
- Built-in debouncing on card presence contacts (typically 4.5 ms)
- Multiplexed status signal using pin OFFN

## 3. Applications

- Pay TV
- Electronic payment
- Identification
- Bank card readers

# 4. Quick reference data



**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $V_{DDI(REG)}$ | regulator input supply voltage | pin CONFIG = ground | | 3.6 | 5 | 5.5 | V |
| | | pin CONFIG = $V_{DDI(REG)}$; regulator is bypassed | | 3 | 3.3 | 3.6 | V |
| $V_{DD(INTF)}$ | interface supply voltage | pin CONFIG = ground | [1] | 1.6 | 3.0 | 3.3 | V |
| | | pin CONFIG = $V_{DDI(REG)}$ and $V_{DD(INTF)}$ not connected to $V_{DDI(REG)}$ and $V_{DD(INTREGD)}$ | | 1.6 | 3.0 | $V_{DDI(REG)}$ + 0.3 | V |
| | | pin CONFIG = $V_{DDI(REG)}$ with $V_{DD(INTF)}$ connected to $V_{DDI(REG)}$ and $V_{DD(INTREGD)}$ | | 3 | 3.3 | 3.6 | V |
| $I_{DDI(REG)}$ | regulator input supply current | inactive mode | | | | | |
| | | $V_{DDI(REG)}$ = 5 V; $f_{xtal}$ = stopped | | - | - | 300 | µA |
| | | $V_{DDI(REG)}$ = 5 V; $f_{xtal}$ = 10 MHz; $f_{CLK} = \frac{1}{8} f_{XTAL}$ | | - | - | 2.5 | mA |
| | | active mode | | | | | |
| | | $V_{CC}$ = 3 V; $I_{CC}$ = 65 mA | | - | - | 85 | mA |
| | | $V_{CC}$ = 1.8 V; $I_{CC}$ = 65 mA | | - | - | 85 | mA |
| | | $V_{CC}$ = 1.2 V; $I_{CC}$ = 30 mA | | - | - | 50 | mA |
| **Card supply voltage** | | | | | | | |
| $V_{CC}$ | supply voltage | including ripple | | | | | |
| | | inactive mode | | | | | |
| | | no load | | –0.1 | - | +0.1 | V |
| | | $I_{CC}$ = 1 mA | | –0.1 | - | +0.3 | V |
| | | active mode | | | | | |
| | | 3 V card: | | | | | |
| | | $I_{CC}$ < 65 mA DC | | 2.85 | 3.05 | 3.15 | V |
| | | single current pulse –100 mA; 2 µs | | 2.76 | 3.05 | 3.20 | V |
| | | current pulses of 40 nAs at $I_{CC}$ < 200 mA; t < 400 ns | | 2.76 | 3.05 | 3.20 | V |
| | | 1.8 V card: | | | | | |
| | | $I_{CC}$ < 65 mA DC | | 1.71 | 1.83 | 1.89 | V |
| | | single current pulse –100 mA; 2 µs | | 1.66 | 1.83 | 1.94 | V |
| | | current pulses of 15 nAs with $I_{CC}$ < 200 mA; t < 400 ns | | 1.66 | 1.83 | 1.94 | V |
| | | 1.2 V card: | | | | | |
| | | $I_{CC}$ < 30 mA DC | | 1.1 | 1.2 | 1.3 | V |
| | | single current pulse –100 mA; 2 µs | | 1.1 | 1.2 | 1.3 | V |
| | | current pulses of 15 nAs with $I_{CC}$ < 200 mA; t < 400 ns | | 1.10 | 1.2 | 1.3 | V |
| $V_{ripple(p-p)}$ | peak-to-peak ripple voltage | pin $V_{CC}$; 20 kHz to 200 MHz | | - | - | 350 | mV |

**Table 1. Quick reference data** *...continued*



| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | supply current | 0 V to 3 V | | - | - | 65 | mA |
| | | 0 V to 1.8 V | | - | - | 65 | mA |
| | | 0 V to 1.2 V | | - | - | 30 | mA |
| SR | slew rate | up or down | | 0.02 | 0.14 | 0.26 | V/µs |
| **General** | | | | | | | |
| $t_{deact}$ | deactivation time | total sequence | [2] | 35 | 80 | 100 | µs |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –25 °C to +85 °C | | - | - | 0.56 | W |
| $T_{amb}$ | ambient temperature | | | –25 | - | +85 | °C |

[1] To enable the microcontroller to provide the required maximum voltage input level on XTAL1, $V_{DD(INTF)}$ must not exceed $V_{DD(INTREGD)}$ + 0.3 V. See Section 8.1 on page 7 for specific limitations on the maximum $V_{DD(INTF)}$ voltage and Table 8 on page 23 for the limits of XTAL1.

[2] See Figure 12 on page 18.

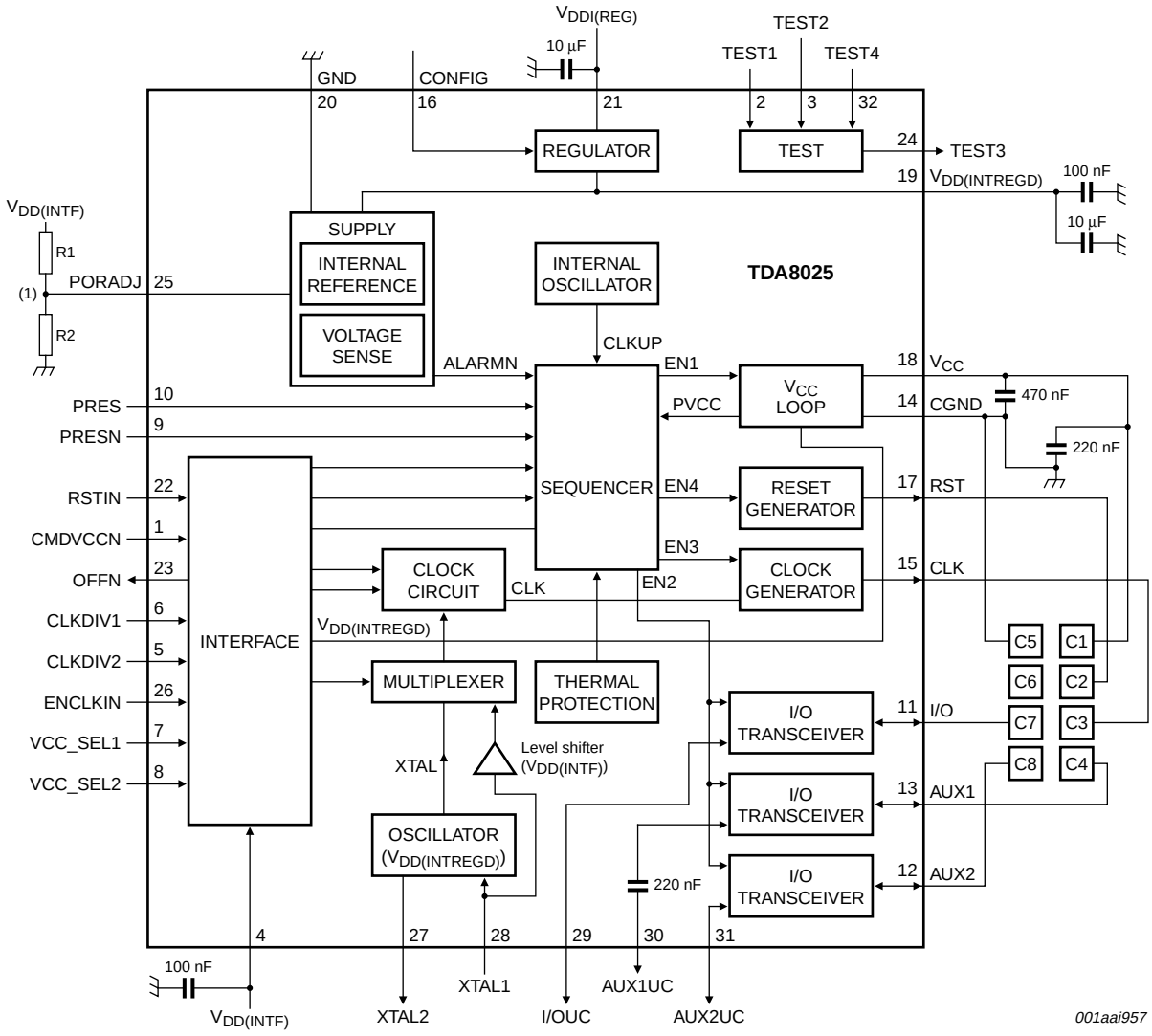
# 5. Ordering information

**Table 2. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TDA8025HN | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm | SOT617-1 |

## 6. Block diagram






(1) Optional external resistor bridge. If this bridge is not needed, connect pin PORADJ to $V_{DD(INTF)}$.

**Fig 1. Block diagram**

# 7. Pinning information



## 7.1 Pinning

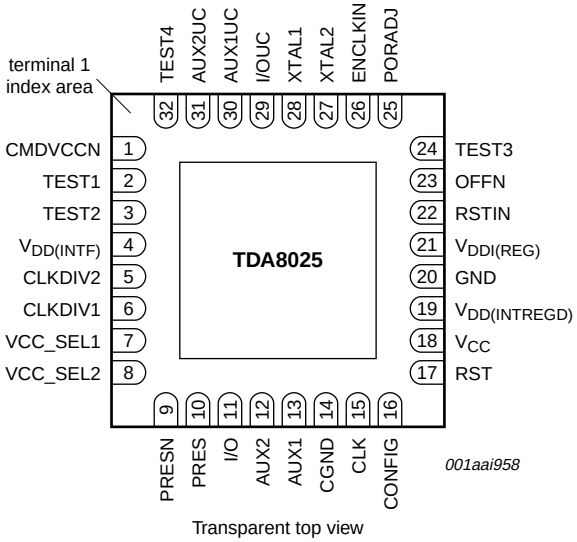



**Fig 2. Pin configuration (HVQFN32)**

## 7.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| CMDVCCN | 1 | I | microcontroller start activation sequence input; active LOW |
| TEST1 | 2 | I | test pin; connect to GND |
| TEST2 | 3 | I | test pin; connect to GND |
| $V_{DD(INTF)}$ | 4 | P | interface supply voltage |
| CLKDIV2 | 5 | I | sets the clock frequency; used together with pin CLKDIV1; see Table 4 on page 12 |
| CLKDIV1 | 6 | I | sets the clock frequency; used together pin CLKDIV2; see Table 4 on page 12 |
| VCC_SEL1 | 7 | I | optional 1.2 V selection control signal:<br>active HIGH: $V_{CC}$ = 1.2 V<br>active LOW: disables 1.2 V selection |
| VCC_SEL2 | 8 | I | 3 V or 1.8 V selection control signal:<br>active LOW: $V_{CC}$ = 3 V<br>active HIGH: $V_{CC}$ = 1.8 V when pin VCC_SEL1 is active LOW |
| PRESN | 9 | I | card presence contact input; active LOW[2] |
| PRES | 10 | I | card presence contact input; active HIGH[2] |
| I/O | 11 | I/O | card input/output data line (C7)[3] |
| AUX2 | 12 | I/O | card auxiliary 2 input/output data line (C8)[3] |
| AUX1 | 13 | I/O | card auxiliary 1 input/output data line (C4)[3] |

**Table 3. Pin description** *...continued*

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| CGND | 14 | G | card signal ground |
| CLK | 15 | O | card clock (C3) |
| CONFIG | 16 | I | 3.3 V or 5 V core regulator supply voltage selection; see Figure 3 on page 7 |
| RST | 17 | O | card reset (C2) |
| $V_{CC}$ | 18 | P | card supply (C1); decouple to pin CGND using one 470 nF and one 220 nF capacitor with an Equivalent Series Resistance (ESR) < 100 mΩ |
| $V_{DD(INTREGD)}$ | 19 | P | internally regulated supply voltage |
| GND | 20 | G | ground |
| $V_{DDI(REG)}$ | 21 | P | regulator input supply voltage |
| RSTIN | 22 | I | microcontroller card reset input; active HIGH |
| OFFN | 23 | O | NMOS interrupt to microcontroller[4]; active LOW; see Section 8.10 on page 19 |
| TEST3 | 24 | O | test pin; do not connect to the application |
| PORADJ | 25 | I | power-on reset threshold adjustment input[4] |
| ENCLKIN | 26 | I | enable external clock on pin XTAL1; active HIGH |
| XTAL2 | 27 | O | crystal connection pin; open when used with an external clock source |
| XTAL1 | 28 | I | crystal connection pin; supply reference $V_{DD(INTREGD)}$<br>external clock input; supply reference $V_{DD(INTF)}$ |
| I/OUC | 29 | I/O | microcontroller input/output data line[4] |
| AUX1UC | 30 | I/O | microcontroller auxiliary 1 input/output data line[4] |
| AUX2UC | 31 | I/O | microcontroller auxiliary 2 input/output data line[4] |
| TEST4 | 32 | I | test pin; connect to GND |

[1] I = input, O = output, I/O = input/output, G = ground and P = power supply.

[2] If pin PRESN or pin PRES is true, the card is considered to be present. During card insertion, debouncing can occur on these signals. To counter this, the TDA8025 has a built-in debouncing timer (typically 4.5 ms).

[3] Using the internal pull-up resistor connected to pin $V_{CC}$.

[4] Using the internal pull-up resistor connected to pin $V_{DD(INTF)}$.

# 8. Functional description



**Remark:** Throughout this document the ISO7816 terminology conventions have been adhered to and it is assumed that the reader is familiar with these.

## 8.1 Power supplies

Two supply selections can be made using pin CONFIG (see Figure 3) depending on the active state of the pin:

- pin CONFIG is LOW: supply is pin $V_{DDI(REG)}$. The voltage range of the pin is between 3.6 V and 5.5 V. The regulator output range is between 3 V and 3.6 V.
- pin CONFIG is HIGH: supply pins $V_{DDI(REG)}$ and $V_{DD(INTREGD)}$ are connected together to bypass the regulator. Pin $V_{DDI(REG)}$ voltage is between 3 V and 3.6 V.

**Remark:** $V_{DD(INTF)}$ must not exceed $V_{DD(INTREGD)}$ + 0.3 V.

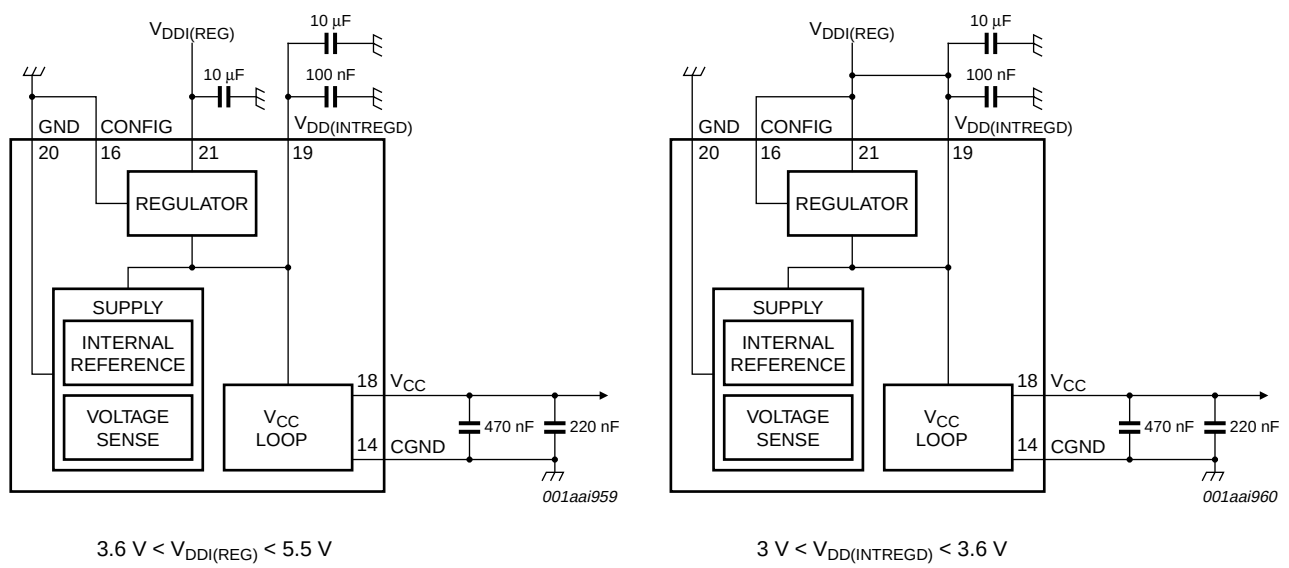



**Fig 3. Power strategy**

The following examples illustrate the voltage restrictions for $V_{DD(INTF)}$.

- CONFIG pin driven to GND: when $V_{DD(INTREGD)}$ is generated by the internal regulator, $V_{DD(INTF)}$ must not exceed 3.3 V.
- CONFIG pin is driven by $V_{DDI(REG)}$ without $V_{DD(INTF)}$ tied to $V_{DDI(REG)}$ while $V_{DD(INTREGD)}$ is tied to $V_{DDI(REG)}$: $V_{DD(INTF)}$ must not exceed $V_{DDI(REG)}$ + 0.3 V.
- CONFIG pin is driven by $V_{DDI(REG)}$ with $V_{DD(INTF)}$ tied to both $V_{DDI(REG)}$ and $V_{DD(INTREGD)}$: there no are restrictions for $V_{DD(INTF)}$.

The TDA8025 is held in the reset state until $V_{DD(INTREGD)}$ reaches $V_{th}$ + $V_{hys}$ and PORADJ $V_{th}$ + $V_{hys}$ plus the $t_{w(POR)}$ delay. If the $V_{DD(INTREGD)}$ and PORADJ signals fall below $V_{th}$, an automatic contact deactivation is triggered.

All interface signals to the microcontroller are referenced to $V_{DD(INTF)}$. In addition, all card contacts remain inactive during power-up and power-down cycles.

After powering up the device, pin OFFN remains LOW until pins CMDVCCN and PRES are both HIGH or pin CMDVCCN is HIGH and pin PRESN is LOW. During power off, pin OFFN is driven LOW when $V_{DD(INTREGD)}$ is below the falling threshold voltage ($V_{th}$).

When pin CMDVCCN is HIGH, the internal oscillator frequency ($f_{osc(int)}$) is switched to Low frequency (inactive) mode to reduce power consumption.

## 8.2 Voltage supervisors

### 8.2.1 Block diagram

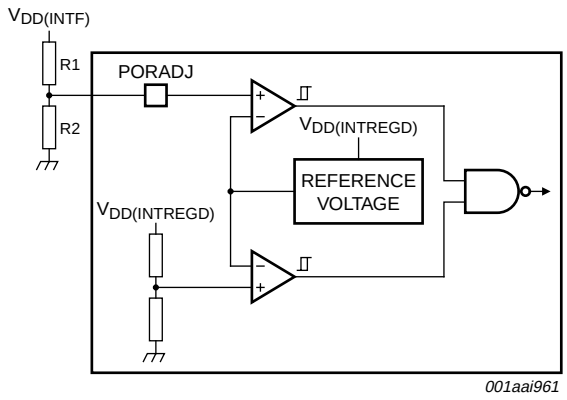



**Fig 4. Voltage supervisor circuit**

### 8.2.2 Description

The voltage supervisors provide both the Power-On Reset (POR) and supply drop-out detection functions. They control the internal regulated supply voltage ($V_{DD(INTREGD)}$) and the microcontroller interface supply voltage ($V_{DD(INTF)}$) to ensure problem-free operation of the TDA8025.

By monitoring both $V_{DD(INTREGD)}$ and $V_{DD(INTF)}$, the voltage supervisors ensure these voltages are high enough to ensure correct operation of the TDA8025 and flawless communication between it and the microcontroller. This information is combined and sent to the digital controller in order to reset the TDA8025.

An extension of the power-on reset pulse width of ± 8 ms ($t_{w(POR)}$) is used to maintain the TDA8025 in inactive mode after the supply voltage power on or off sequences (see Figure 5).

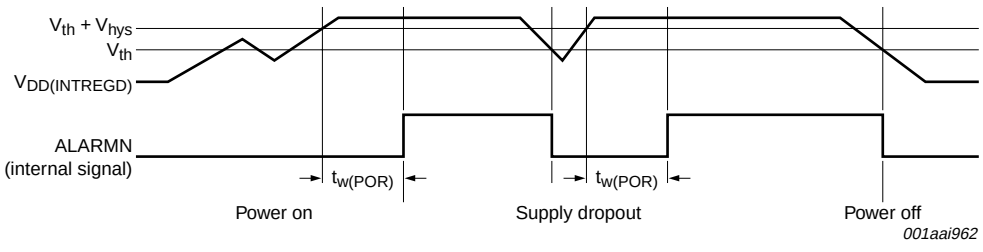



**Fig 5. Voltage supervisors $V_{DD(INTREGD)}$ and $V_{DD(INTF)}$**

### 8.2.3 $V_{DD(INTREGD)}$ voltage supervisor with pin PORADJ connected to $V_{DD(INTF)}$

The TDA8025 remains in inactive mode irrespective of the levels on the command lines when

- $V_{DD(INTREGD)}$ is less than $V_{th} + V_{hys}$ (on pin $V_{DD(INTREGD)}$)
- Pin PORADJ (monitoring $V_{DD(INTF)}$) is less than $V_{th} + V_{hys}$

In both cases, this lasts for the duration of $t_{w(POR)}$ after $V_{DD(INTREGD)}$ (on pin $V_{DD(INTREGD)}$) and $V_{DD(INTF)}$ (on pin $V_{DD(INTF)}$) have reached a level higher than $V_{th} + V_{hys}$. Two threshold voltages ($V_{th}$) are set by the hardware as follows:

- $V_{DD(INTREGD)}$ threshold voltage: is set to the minimum supply voltage (2.7 V) specified for the digital part of the TDA8025
- $V_{DD(INTF)}$ threshold voltage: is set to 1.24 V; see Table 8 on page 23 for detailed information.

### 8.2.4 $V_{DD(INTF)}$ voltage supervisor with external divider on pin PORADJ

An external resistor bridge can be used to divide $V_{DD(INTF)}$ on pin PORADJ to adapt the detection threshold when monitoring the microcontroller interface supply voltage.

Connecting the external resistor bridge as illustrated in Figure 4 on page 8 (R1 connected to $V_{DD(INTF)}$ and R2 connected to GND) to pin PORADJ overrides the internal threshold voltage $V_{th}$ on pin $V_{DD(INTF)}$.

The threshold voltage on pin $V_{DD(INTF)}$ is calculated as follows:

$$V_{th} \text{ on pin } V_{DD(INTF)} = V_{bg}\left(\frac{1 + R1}{R2}\right) \quad (1)$$

where

- $V_{bg}$ is the bandgap voltage

When the resistor bridge is not used, pin PORADJ must be connected to pin $V_{DD(INTF)}$.

#### 8.2.4.1 R1 and R2 resistor value calculation

This section describes how to calculate the values for resistors R1 and R2, taking into account the IC detector threshold spread and the external resistance, while ensuring reliable activation.

If for example, the controller is supplied by a regulator at 3.3 V ± 20 %. Activation can be triggered above $V_{DD(INTF)}$ = 3.3 V – 20 % (in this example 2.64 V). This activation threshold is defined as $V_{DD(INTF)actmin}$; i.e. the minimum value of $V_{DD(INTF)}$ above which activation can always be triggered.

In addition to this external input, activation is permitted provided all the following conditions are met (see Table 8 on page 23): card presence, IC temperature, $V_{DD(INTF)}$ and $V_{DD(INTREGD)}$ supplies, etc.

The voltage on PORADJ ($V_{PORADJ}$) can be calculated as: $V_{PORADJ} = \alpha \times V_{DD(INTF)}$



where:

- $V_{DD(INTF)}$ is the interface supply voltage
- ratio $\alpha$

$$\alpha = \frac{1}{1 + \frac{R1}{R2}} \quad (2)$$

An activation can be triggered if

$$V_{DD(INTF)} \times \alpha > V_{th(max)} \Rightarrow V_{DD(INTF)} > \frac{V_{th(max)}}{\alpha} \quad (3)$$

where

- $V_{th(max)}$ is the maximum rising external threshold voltage

The resistance spread of R1 between a minimum value $R1_{min}$ and a maximum value $R1_{max}$ induces a spread of the ratio $\alpha$. This is also true for R2. Based on this:

$$V_{DD(INTF)actmin} = \frac{V_{th(max)}}{\alpha_{min}} \quad (4)$$

where

$$\alpha_{min} = \frac{1}{1 + \frac{R1_{max}}{R2_{min}}} \quad (5)$$

If $\Delta R1$ is the maximum spread of R1 and $\Delta R2$ is the maximum spread of R2 then:

$$R1_{max} = R1_{nom} + \Delta R1 = R1_{nom} \cdot \left(1 + \frac{\Delta R1}{R1_{nom}}\right) \quad (6)$$

$$R2_{min} = R2_{nom} - \Delta R2 = R2_{nom} \cdot \left(1 - \frac{\Delta R2}{R2_{nom}}\right) \quad (7)$$

$$\alpha_{min} = \frac{1}{1 + \frac{R1_{nom} \cdot \left(1 + \frac{\Delta R1}{R1_{nom}}\right)}{R2_{nom} \cdot \left(1 - \frac{\Delta R2}{R2_{nom}}\right)}} = \frac{1}{1 + \frac{R1_{nom} \cdot (1 + \beta)}{R2_{nom} \cdot (1 - \beta)}} = \frac{V_{th(max)}}{V_{DD(INTF)actmin}} \quad (8)$$

where

- where $\beta$ is the accuracy ratio of R1 and R2 (R1 and R2 are considered to be of the same type).

Then

$$\frac{R1_{nom}}{R2_{nom}} = \frac{(1-\beta)}{(1+\beta)} \cdot \left(\frac{V_{DD(INTF)actmin}}{V_{th(max)}} - 1\right) \quad (9)$$

$$R2_{nom} = \frac{R_{sum}}{\left(1 + \frac{R1_{nom}}{R2_{nom}}\right)} = \frac{R_{sum}}{\left(1 + \frac{(1-\beta)}{(1+\beta)} \cdot \left(\frac{V_{DD(INTF)actmin}}{V_{th(max)}} - 1\right)\right)} \quad (10)$$

If we target 1 % accuracy resistors ($\beta$ = 0.01) and $R_{sum}$ = 100 kΩ; $V_{th(max)}$ = 1.33 V (see Table 8 on page 23) and $V_{DD(INTF)actmin}$ = 2.64 V then

- $R1_{nom}$ = 50.88 kΩ
- $R2_{nom}$ = 49.12 kΩ

Deactivation always occurs when

$$V_{PORADJ} < V_{th(min)} \Rightarrow V_{DD(INTF)deactmax} = \frac{V_{th(min)}}{\alpha_{max}} \quad (11)$$

where

- $V_{th(min)}$ is the minimum falling external threshold voltage
- $V_{DD(INTF)deactmax}$ is the maximum value of $V_{DD(INTF)}$ below which deactivation always occurs
- $\alpha_{max}$

$$\alpha_{max} = \frac{1}{1 + \frac{R1_{nom} \cdot (1-\beta)}{R2_{nom} \cdot (1+\beta)}} = \frac{V_{th(min)}}{V_{DD(INTF)deactmax}} \quad (12)$$

With the resulting values for $R1_{nom}$, $R2_{nom}$ and $\beta$; $V_{th(min)}$ = 1.17 V (see Table 8 on page 23) then $V_{DD(INTF)deactmax}$ is 2.28 V.

## 8.3 Clock circuits

The clock signal (pin CLK) to the card is either generated by the clock signal input on pin XTAL1 or from a crystal ($f_{xtal} \leq 26$ MHz) connected between pins XTAL1 and XTAL2. The voltage level applied to pin ENCLKIN defines which clock signal is used. When pin ENCLKIN is HIGH, connect the external clock to pin XTAL1.

Driving pin ENCLKIN LOW causes the external crystal to generate frequency $f_{xtal}$. Using pins CLKDIV1 and CLKDIV2, the crystal frequency can be set to either $f_{xtal}$, ½ $f_{xtal}$, ¼ $f_{xtal}$ or ⅛ $f_{xtal}$.

The frequency change is synchronous and as such during transition, no pulse is shorter than 45 % of the smallest period. In addition, only the first and last clock pulse around the change have the correct width. When dynamically changing the frequency, the modification is only effective after 10 periods of XTAL1.

The duty cycle on pin CLK should be between 45 % and 55 %. To ensure this, the following must be applied:

- when the CLK frequency is $f_{xtal}$:

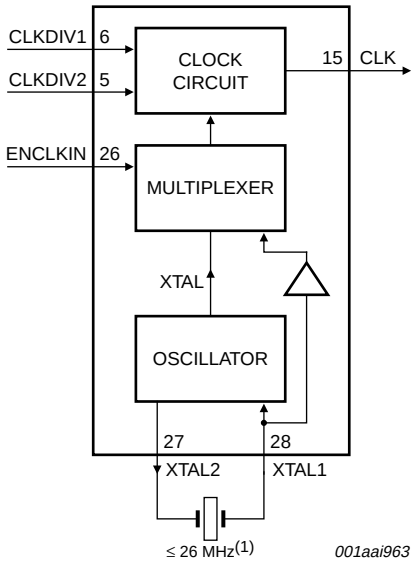
  If an external clock is connected to pin XTAL1, the duty cycle should be between 48 % and 52 % with an input signal period transition time of less than 5 %.

  If a crystal is used to generate $f_{xtal}$, the duty cycle on pin CLK should be between 45 % and 55 % depending on the layout, crystal characteristics and frequency.

- when CLK frequency is either $f_{xtal}$, $\frac{1}{2}$ $f_{xtal}$, $\frac{1}{4}$ $f_{xtal}$ or $\frac{1}{8}$ $f_{xtal}$:

  The duty cycle is guaranteed between 45 % and 55 % of the period frequency divisions.

  When a crystal is used, it runs when pin ENCLKIN is driven LOW.




(1) External crystal (optional).

**Fig 6. Clock circuits**

The clock signal is applied to the card based on the activation sequence as shown on the timing diagrams; see Figure 8 on page 15 to Figure 13 on page 19.

When the signal applied to XTAL1 is controlled by the microcontroller, the clock signal is sent to the card only after the activation sequence finishes.

**Table 4. Clock configuration**

*Clock circuitry definition (pins CLKDIV1 and CLKDIV2 can be changed simultaneously; a >10 XTAL1 period delay is needed. The minimum duration of any CLK state is 10 XTAL1 periods).*

| CLKDIV1 | CLKDIV2 | CLK |
|---|---|---|
| 0 | 0 | $\frac{1}{8}$ $f_{xtal}$ |
| 0 | 1 | $\frac{1}{4}$ $f_{xtal}$ |
| 1 | 1 | $\frac{1}{2}$ $f_{xtal}$ |
| 1 | 0 | $f_{xtal}$ |

## 8.4 Input and output circuits

When pins I/O and I/OUC are driven HIGH using an 11 kΩ resistor between pins I/O and $V_{CC}$ and/or between pins I/OUC and $V_{DD(INTF)}$, both lines enter the idle state. Pin I/O is referenced to $V_{CC}$ and pin I/OUC to $V_{DD(INTF)}$, thus allowing operation at $V_{CC} \neq V_{DD(INTF)}$.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables falling edge detection on the other line, making it the slave. After a time delay $t_{d(edge)}$, the NMOS transistor on the slave-side is turned on. It then sends logic 0 to the master-side. When the master returns logic 1, the PMOS transistor on the slave side is turned on during the time delay ($t_{pu}$). After this sequence, both the master and slave return to their idle states.

The active pull-up feature ensures fast LOW-to-HIGH transitions making the TDA8025 capable of delivering more than 1 mA, up to an output voltage of 0.9 $V_{CC}$, at a load of 80 pF. At the end of the active pull-up pulse, the output voltage is dependent on the internal pull-up resistor value and load current. The current sent to and received from the card's I/O lines is internally limited to 15 mA at a maximum frequency of 1 MHz.

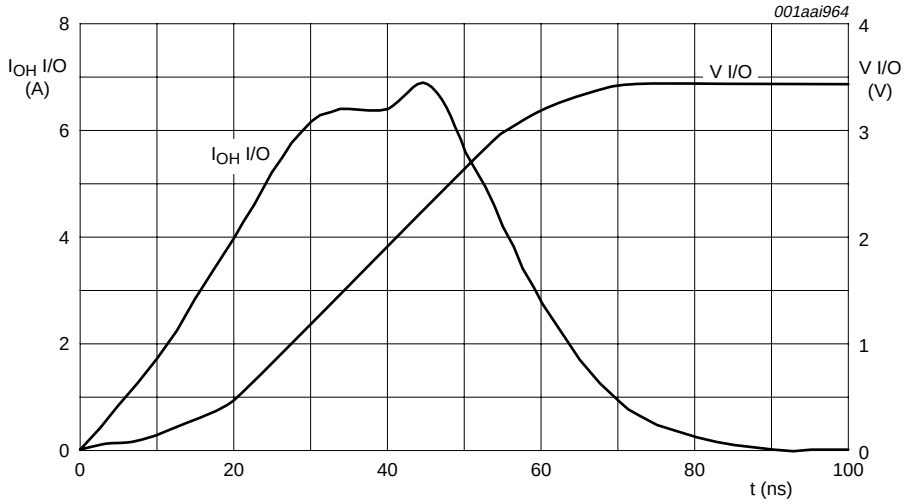



**Fig 7. Output voltage and current on pins I/O, AUX1 and AUX2 as a function of time during LOW-to-HIGH transitions**

## 8.5 Inactive mode

After a power-on reset, the circuit enters the inactive mode, ensuring only the minimum number of circuits are active while the TDA8025 waits for the microcontroller to start a session. The inactive mode conditions are as follows:

- all card contacts are inactive. The impedance between the contacts and GND is approximately 200 Ω.
- pins I/OUC, AUX1UC and AUX2UC are high-impedance using the 11 kΩ pull-up resistor connected to $V_{DD(INTF)}$
- the voltage generators and crystal oscillator are stopped
- the voltage supervisor is active
- the internal oscillator runs in low frequency mode

## 8.6 Activation sequence



After the power-on and internal pulse width delay, the microcontroller checks the presence of the card using signal OFFN.

- The card is present when pins OFFN and CMDVCCN are HIGH
- The card is not present when pin OFFN is LOW and pin CMDVCCN is HIGH

If the card is in the reader (either pin PRESN or pin PRES is true), the microcontroller can start a card session by pulling pin CMDVCCN LOW. When using an external crystal, the following sequence is applied (see Figure 8):

1. pin CMDVCCN is pulled LOW (t0)
2. the crystal oscillator is triggered
3. the internal oscillator changes to its high frequency (t1)
4. $V_{CC}$ rises either from 0 V to 3 V or 1.8 V on a controlled slope (t2)
5. pins I/O, AUX1 and AUX2 which were pulled LOW are driven HIGH (t3)
6. the clock (pin CLK) is applied to the C3 contact (t4)
7. pin RST is enabled (t5)

Calculation of the time delays is as follows:

- t1 = t0 + 2.13 ms
- t2 = t1
- t3 = t1 + 5T/2
- t4 = driven by host controller; > t3 and < t5
- t5 = t1 + 11T/2

**Remark:** The value of period T is 64 times the period interval of the internal oscillator (i.e. ±25 µs. t3 is called $t_{d(start)}$ and t5 is called $t_{d(end)}$.

The clock is applied to the card in one of the following ways:

- using pin RSTIN: The clock (pin CLK) start-up can be selected at either t3 or t5 using pin RSTIN. When pin RSTIN is HIGH and pin CMDVCCN is LOW, setting pin RSTIN to LOW between delays t3 and t5 sends signal CLK. Pin RSTIN should be held LOW until after delay t5. After passing t5, pin RST is a copy of pin RSTIN and has no further effect on pin CLK. It enables the microcontroller to precisely choose the CLK start by counting clock cycles from the falling edge of the RSTIN signal.
- not using pin RSTIN: If this feature is not needed, set both pins CMDVCCN and RSTIN to LOW. The clock (pin CLK) will start at delay t3 (a minimum 200 ns after the input/output transition). After delay t5, pin RSTIN can be set HIGH to receive the card Answer To Request (ATR).

**Remark:** Do not perform activation with pin RSTIN permanently pulled HIGH.

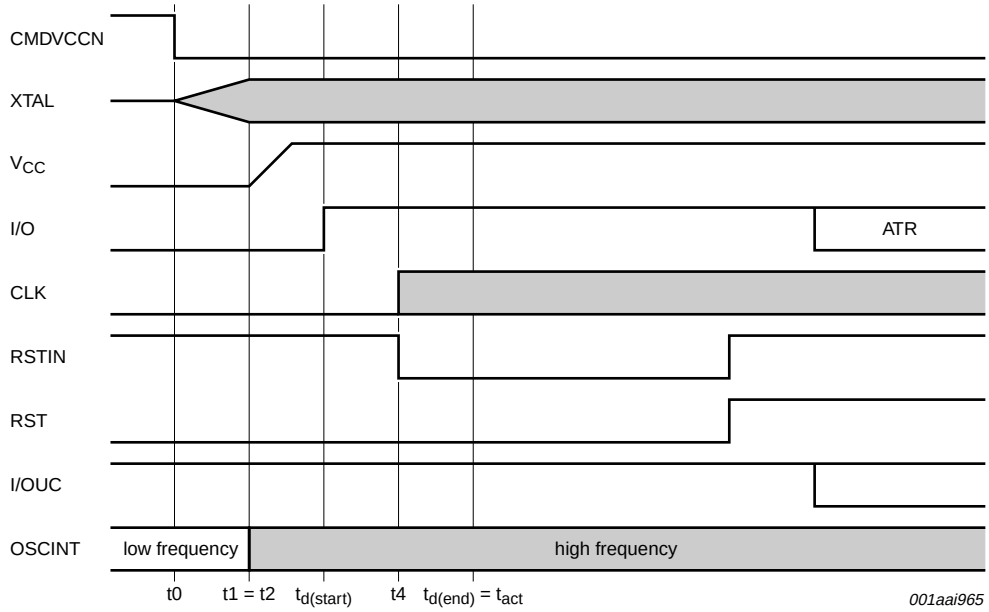



**Fig 8. Activation sequence: CLK controlled by pin RSTIN with the crystal oscillator**

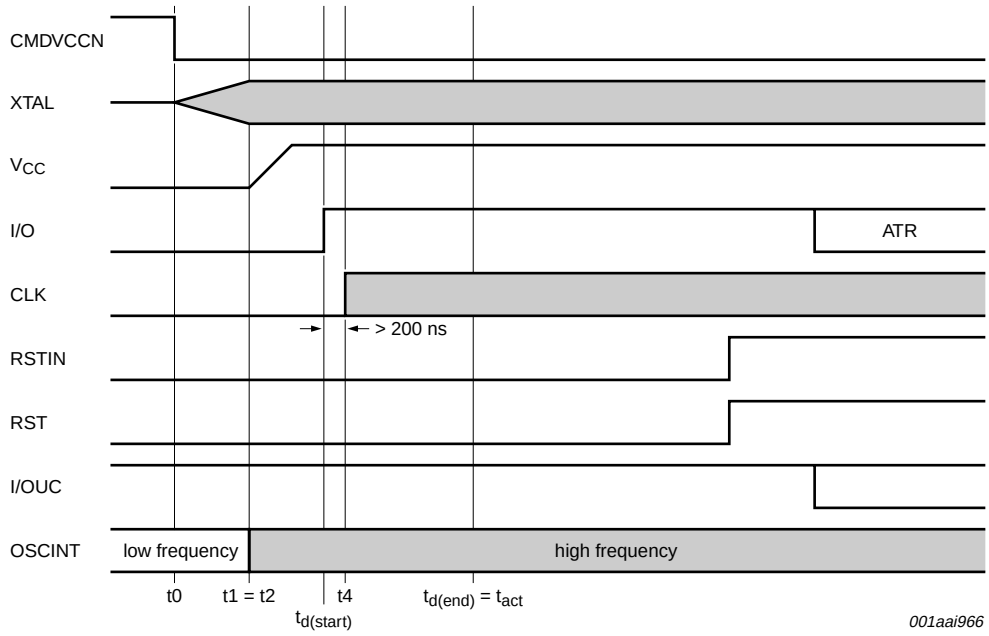



**Fig 9. Activation sequence: CLK not controlled by pin RSTIN with the crystal oscillator**

The following sequence occurs when using an external clock connected to pin XTAL1 (see Figure 10):

1. external clock (XTAL1) started by the microcontroller (t0)
2. CMDVCCN is pulled LOW and the internal oscillator changes to its high frequency (t1)
3. $V_{CC}$ rises either from 0 V to 3 V or 0 V to 1.8 V on a controlled slope (t2)

4. pins I/O, AUX1 and AUX2 are enabled (t3)
5. CLK is applied to the C3 contact (t4)
6. pin RST is enabled (t5)

Calculation of the time delays is as follows:

- t1 = t0 + 2.13 ms
- t2 = t1 = 3T/2 + 3($^1/_{f_{osc(int)low}}$)
- t3 = t1 + 5T/2
- t4 = driven by the host controller; > t3 and < t5
- t5 = t1 + 11T/2

**Remark:** The value of period T is 64 times the period interval of the internal oscillator (i.e. ±25 µs). t3 is called $t_{d(start)}$ and t5 is called $t_{d(end)}$. $f_{osc(int)low}$ is the low (or inactive mode) frequency of the defined $f_{osc(int)}$ parameter.

The CLK is applied to the card under control of pin RSTIN in exactly the same way as with the crystal oscillator.

**Remark:** Do not perform activation with pin RSTIN permanently pulled HIGH.

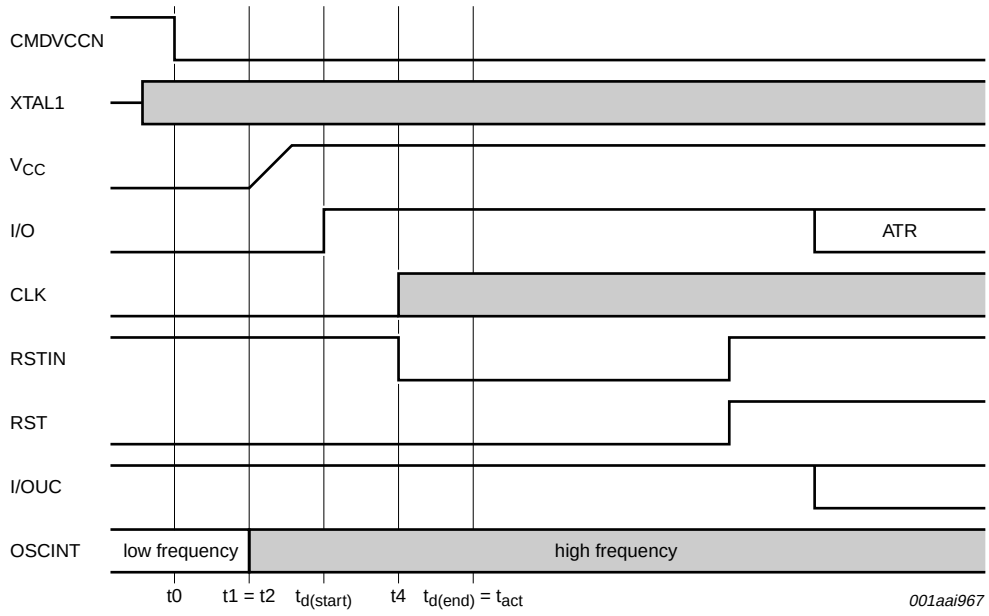



**Fig 10. Activation sequence: CLK controlled by pin RSTIN with an external clock connected to pin XTAL1**

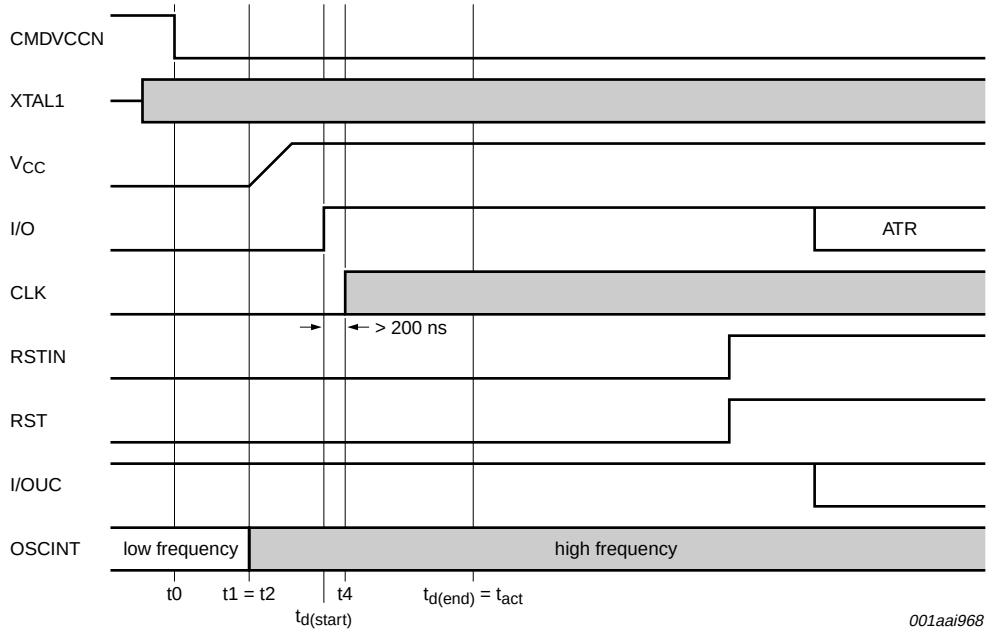



**Fig 11. Activation sequence: CLK not controlled by pin RSTIN and with an external clock connected to pin XTAL1**

## 8.7 Active mode

When the activation sequence has finished, the TDA8025 is in active mode. This mode enables data exchange between the card and the microcontroller using the input and output lines.

Depending on the layout and application test conditions, line C2 could become polluted with high frequency noise from line C3. For example, due to an additional 1 pF capacitance between lines C2/C3 and/or lines C2/C7. It is recommended that a 100 pF capacitor is added between line C2 and pin CGND, if this occurs.

When building the application, the following recommendations should be adhered to:

- Keep track C3 as far away as possible from other tracks.
- Keep the connection between pin CGND and line C5 straight. The two capacitors on line C1 should be connected to this ground track.
- Do not use ground loops between CGND and GND.

Following these layout recommendations will ensure that noise remains within the specifications and jitter on line C3 is less than 100 ps.

## 8.8 Deactivation sequence



When a session is completed, the microcontroller sets pin CMDVCCN to HIGH. The circuit then executes an automatic deactivation sequence by counting the sequencer back to the inactive state (see Figure 12 and Figure 13):

1. pin RST is pulled LOW (t11)
2. the clock is stopped, pin CLK is LOW (t12)
3. pins I/O, AUX1 and AUX2 are pulled LOW (t13)
4. $V_{CC}$ falls to zero (t14). The deactivation sequence is completed when $V_{CC}$ reaches its inactive state
5. all card contacts become low-impedance to GND. However, pins I/OUC, AUX1UC and AUX2UC remain pulled up to $V_{DD(INTREGD)}$ using the 11 kΩ resistor
6. The internal oscillator returns to its low frequency mode

Calculation of the time delays is as follows:

- t11 = t10 + 3T/64
- t12 = t11 + T/2
- t13 = t11 + T
- t14 = t11 + 3T/2

**Remark:** The value of period T is 64 times the period interval of the internal oscillator (i.e. ±25 µs).

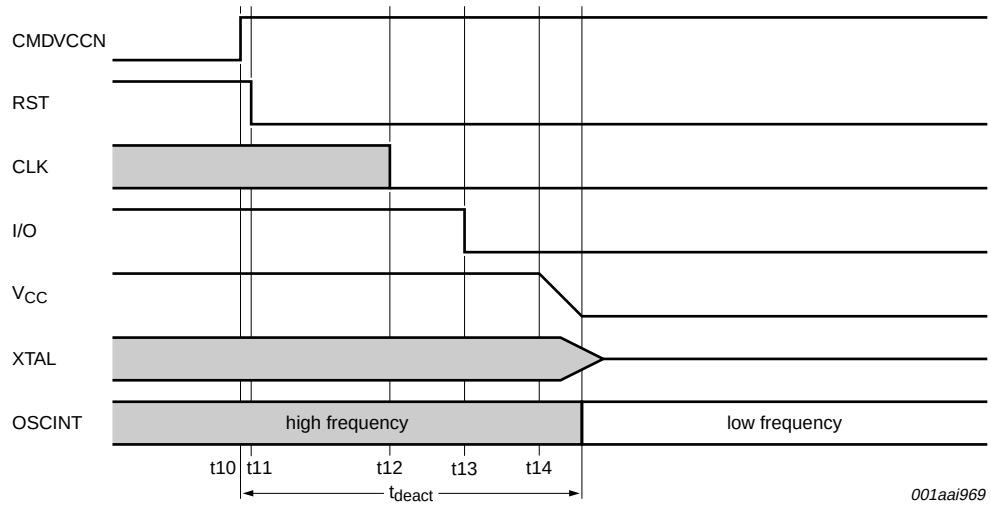



**Fig 12. Deactivation sequence with a crystal oscillator**

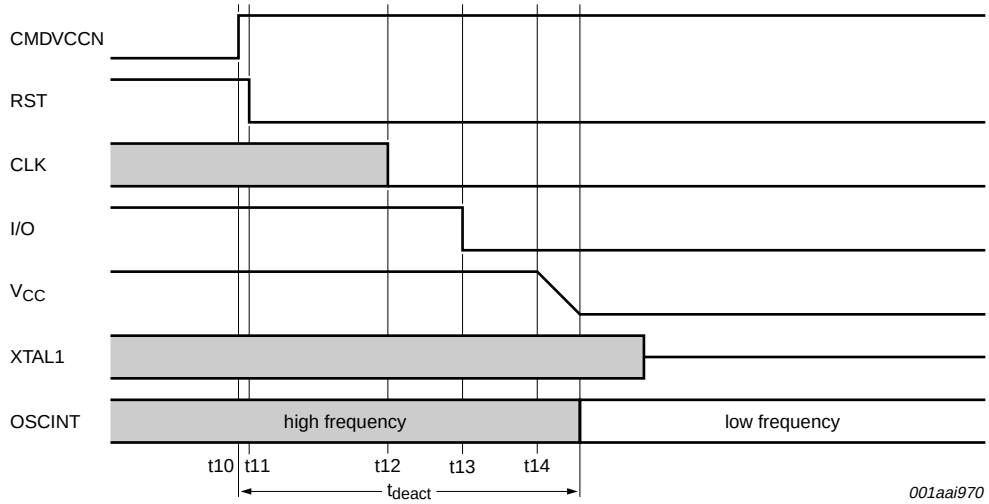



**Fig 13. Deactivation sequence with an external clock connected to pin XTAL1**

## 8.9 $V_{CC}$ regulator

**Table 5. Selection of $V_{CC}$ using pins VCC_SEL1 and VCC_SEL2**

| VCC_SEL1 | VCC_SEL2 | $V_{CC}$ |
|---|---|---|
| 0 | 0 | 3 V |
| 0 | 1 | 1.8 V |
| 1 | 0 | 1.2 V |
| 1 | 1 | 1.2 V |

The $V_{CC}$ buffer is able to continuously deliver up to:

- 65 mA at 3 V
- 65 mA at 1.8 V
- 30 mA at 1.2 V

The $V_{CC}$ buffer has an internal overload protection with a threshold value of ±135 mA. This detection is filtered, enabling spurious current pulses up to 200 mA with a duration of up to 200 ns to be drawn by the card without causing deactivation. However, the average current value must be below maximum.

To enhance $V_{CC}$ stability, one 470 nF capacitor should be tied to pin CGND near pin 18 and one 220 nF capacitor should be tied to pin CGND near the C1 contact. Both capacitors should have an ESR < 100 mΩ.

## 8.10 Fault detection

The following conditions are monitored by the fault detection circuit:

- Short-circuit or high current on pin $V_{CC}$
- Card removal during transaction
- $V_{DD(INTREGD)}$ falling

- $V_{DD(INTF)}$ falling
- Overheating

Fault detection monitors two different situations (see Figure 15 on page 21):

1. Outside card sessions, pin CMDVCCN is HIGH: pin OFFN is LOW if the card is not in the reader and HIGH if the card is in the reader. Any supply voltage drop on $V_{DD(INTREGD)}$ or $V_{DD(INTF)}$ is detected by the supply supervisor. This generates an internal power-on reset pulse but does not act upon the pin OFFN signal. The card is not powered-up and as such short-circuits and overheating are not detected.
2. Within card sessions, pin CMDVCCN is LOW: when pin OFFN falls LOW, the fault detection circuit triggers the automatic emergency deactivation sequence (see Figure 14). When the system controller resets pin CMDVCCN to HIGH, after the deactivation sequence, pin OFFN is rechecked. If the card is still present, pin OFFN returns to HIGH. This check identifies the fault as either a hardware problem or a card removal incident.

On card insertion or removal, bouncing can occur in the PRES and/or PRESN signals. This depends on the type of card presence switch in the connector (normally open or normally closed) and the mechanical characteristics of the switch. To correct for this, a debouncing feature is integrated in to the TDA8025. This feature operates at a typical duration of $640 \times (1/f_{osc(int)low})$. See Figure 15 for an overview of the debouncing feature.

**Remark:** $f_{osc(int)low}$ is the low frequency (or inactive) mode of the defined $f_{osc(int)}$ parameter.

On card insertion, pin OFFN goes HIGH after the debouncing time has elapsed. When the card is extracted, the automatic card deactivation sequence is performed on the first true or false transition on pin PRESN or pin PRES. After this pin OFFN goes LOW.

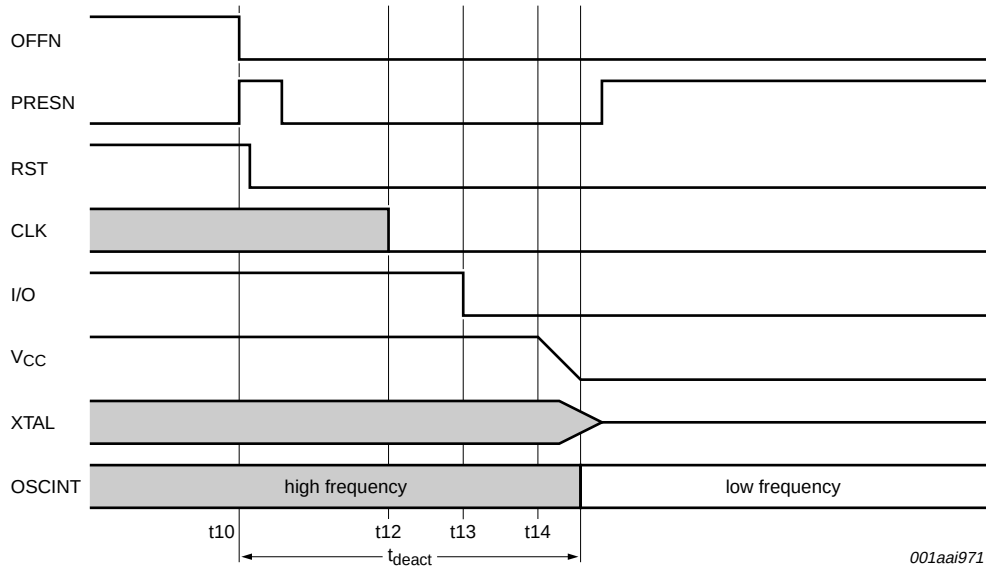
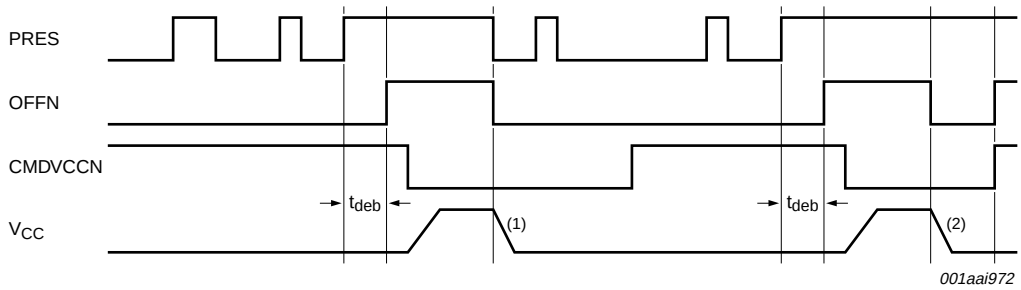



**Fig 14. Emergency deactivation sequence after card removal**




(1) Deactivation caused by card removal.

(2) Deactivation caused by short circuit.

**Fig 15. Operation of debounce feature pin OFFN in combination with pins CMDVCCN, PRES and $V_{CC}$**

## 9. Limiting values



**Remark:** All card contacts are protected against any short-circuit to any other card contact. Stress beyond the levels indicated in Table 6 can cause permanent damage to the device. This is a short-term stress rating only and under no circumstances implies functional operation under long-term stress conditions.

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DDI(REG)}$ | regulator input supply voltage | | –0.3 | +5.5 | V |
| $V_{DD(INTREGD)}$ | internal regulated supply voltage | | –0.3 | +5.5 | V |
| $V_I$ | input voltage | pins CMDVCCN, TEST1, TEST2, CLKDIV2, CLKDIV1, VCC_SEL1, VCC_SEL2, CONFIG, RSTIN, OFFN, TEST3, PORADJ, ENCLKIN, XTAL2, XTAL1, I/OUC, AUX1UC and AUX2UC | –0.3 | +5.5 | V |
| | | card contact pins PRES, PRESN, I/O, RST, AUX1, AUX2 and CLK | –0.3 | +6.5 | V |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –25 °C to +85 °C | - | 0.56 | W |
| $T_j$ | junction temperature | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | –25 | +85 | °C |
| $V_{ESD}$ | electrostatic discharge voltage | pins I/O, RST, $V_{CC}$, AUX1, CLK, AUX2, PRES and PRESN; within typical application | –6 | +6 | kV |
| | | Human Body Model (HBM); all pins; EIA/JESD22-A114-B, June 2000 | –2 | +2 | kV |
| | | Machine Model (MM); all pins; EIA/JESD22-A115-A, October 1997 | –200 | +200 | V |
| | | Charged Device Model (CDM); | | | |
| | | all pins, except corner pins | –500 | +500 | V |
| | | only corner pins (1, 8, 9, 16, 17, 24, 25 and 32) | –750 | +750 | V |

## 10. Thermal characteristics

**Table 7. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | with exposed pad soldered | 42 | K/W |
| | | without exposed pad soldered | 62 | K/W |

# 11. Characteristics



**Table 8. Characteristics of IC supply voltage**

*$T_{amb}$ = 25 °C; all parameters remain within limits but are only statistically tested for the temperature range; $f_{xtal}$ = 10 MHz; all currents flowing into the IC are positive; unless otherwise specified. Parameters specified as a function of $V_{DD(INTF)}$, $V_{DDI(REG)}$, $V_{DD(INTREGD)}$ or $V_{CC}$ refer to the actual value at the time of measurement.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | |
| $V_{DDI(REG)}$ | regulator input supply voltage | pin CONFIG = ground | | 3.6 | 5 | 5.5 | V |
| | | pin CONFIG = $V_{DDI(REG)}$; regulator is bypassed | | 3 | 3.3 | 3.6 | V |
| $V_{DD(INTREGD)}$ | internal regulated supply voltage | pin CONFIG = ground | [1] | 3 | 3.3 | 3.6 | V |
| $V_{DD(INTF)}$ | interface supply voltage | pin CONFIG = ground | [2] | 1.6 | 3.0 | 3.3 | V |
| | | pin CONFIG = $V_{DDI(REG)}$ and $V_{DD(INTF)}$ not connected to $V_{DDI(REG)}$ and $V_{DD(INTREGD)}$ | | 1.6 | 3.0 | $V_{DDI(REG)}$ + 0.3 | V |
| | | pin CONFIG = $V_{DDI(REG)}$ with $V_{DD(INTF)}$ connected to $V_{DDI(REG)}$ and $V_{DD(INTREGD)}$ | | 3 | 3.3 | 3.6 | V |
| $I_{DDI(REG)}$ | regulator input supply current | inactive mode | | | | | |
| | | $V_{DDI(REG)}$ = 5 V<br>$f_{xtal}$ = stopped | | - | - | 300 | µA |
| | | $V_{DDI(REG)}$ = 5 V<br>$f_{xtal}$ = 10 MHz;<br>$f_{CLK}$ = ⅛ $f_{xtal}$ | | - | - | 2.5 | mA |
| | | active mode | | | | | |
| | | $V_{CC}$ = 3 V; $I_{CC}$ = 65 mA | | - | - | 85 | mA |
| | | $V_{CC}$ = 1.8 V;<br>$I_{CC}$ = 65 mA | | - | - | 85 | mA |
| | | $V_{CC}$ = 1.2 V;<br>$I_{CC}$ = 30 mA | | - | - | 50 | mA |
| $I_{DD(INTF)}$ | interface supply current | | | - | - | 100 | µA |
| $V_{th}$ | threshold voltage | pin $V_{DD(INTREGD)}$; falling | | 2.60 | 2.70 | 2.80 | V |
| | | pin $V_{DD(INTREGD)}$; rising | | 2.65 | 2.80 | 2.95 | V |
| | | pin PORADJ; falling | | 1.17 | 1.24 | 1.31 | V |
| | | pin PORADJ; rising | | 1.19 | 1.26 | 1.33 | V |
| $V_{hys}$ | hysteresis voltage | pin $V_{DD(INTREGD)}$ | | 50 | 100 | 150 | mV |
| $t_{w(POR)}$ | power-on reset pulse width | | | 5 | 8 | 18 | ms |
| $\Delta V_{th}/\Delta T$ | threshold voltage variation with temperature | | | - | - | 0.25 | mV/°C |

**Table 8. Characteristics of IC supply voltage** *…continued*

*$T_{amb}$ = 25 °C; all parameters remain within limits but are only statistically tested for the temperature range; $f_{xtal}$ = 10 MHz; all currents flowing into the IC are positive; unless otherwise specified. Parameters specified as a function of $V_{DD(INTF)}$, $V_{DD(REG)}$, $V_{DD(INTREGD)}$ or $V_{CC}$ refer to the actual value at the time of measurement.*



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_L$ | leakage current | pin PORADJ < 0.5 V | –0.1 | +4 | +10 | µA |
| | | pin PORADJ > 1 V | –1 | - | +1 | µA |
| **Card supply voltage**[3] | | | | | | |
| $C_{dec}$ | decoupling capacitance | connected to $V_{CC}$ | 550 | - | 830 | nF |
| $V_{CC}$ | supply voltage | including ripple | | | | |
| | | inactive mode | | | | |
| | | no load | –0.1 | - | +0.1 | V |
| | | $I_{CC}$ = 1 mA | –0.1 | - | +0.3 | V |
| | | active mode | | | | |
| | | 3 V card: | | | | |
| | | $I_{CC}$ < 65 mA DC | 2.85 | 3.05 | 3.15 | V |
| | | single current pulse –100 mA; 2 µs | 2.76 | 3.05 | 3.20 | V |
| | | current pulses of 40 nAs at $I_{CC}$ < 200 mA; t < 400 ns | 2.76 | 3.05 | 3.20 | V |
| | | 1.8 V card: | | | | |
| | | $I_{CC}$ < 65 mA DC | 1.71 | 1.83 | 1.89 | V |
| | | single current pulse –100 mA; 2 µs | 1.66 | 1.83 | 1.94 | V |
| | | current pulses of 15 nAs with $I_{CC}$ < 200 mA; t < 400 ns | 1.66 | 1.83 | 1.94 | V |
| | | 1.2 V card: | | | | |
| | | $I_{CC}$ < 30 mA DC | 1.1 | 1.2 | 1.3 | V |
| | | single current pulse –100 mA; 2 µs | 1.1 | 1.2 | 1.3 | V |
| | | current pulses of 15 nAs with $I_{CC}$ < 200 mA; t < 400 ns | 1.10 | 1.2 | 1.3 | V |
| $V_{ripple(p-p)}$ | peak-to-peak ripple voltage | pin $V_{CC}$; 20 kHz to 200 MHz | - | - | 350 | mV |
| $I_{CC}$ | supply current | 0 V to 3 V | - | - | 65 | mA |
| | | 0 V to 1.8 V | - | - | 65 | mA |
| | | 0 V to 1.2 V | - | - | 30 | mA |
| SR | slew rate | up or down | 0.02 | 0.14 | 0.26 | V/µs |
| **Crystal oscillator: pins XTAL1 and XTAL2** | | | | | | |
| $C_{ext}$ | external capacitance | pins XTAL1/XTAL2; depending on the crystal or resonator specification | - | - | 15 | pF |

**Table 8. Characteristics of IC supply voltage** *…continued*

*$T_{amb}$ = 25 °C; all parameters remain within limits but are only statistically tested for the temperature range; $f_{xtal}$ = 10 MHz; all currents flowing into the IC are positive; unless otherwise specified. Parameters specified as a function of $V_{DD(INTF)}$, $V_{DDI(REG)}$, $V_{DD(INTREGD)}$ or $V_{CC}$ refer to the actual value at the time of measurement.*



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{xtal}$ | crystal frequency | card clock reference; crystal oscillator | 2 | - | 26 | MHz |
| $f_{ext}$ | external frequency | external clock on pin XTAL1 | 0 | - | 26 | MHz |
| $V_{IL}$ | LOW-level input voltage | pin XTAL1 | –0.3 | - | $+0.3V_{DD(INTF)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | pin XTAL1 | | | | |
| | | $V_{DD(INTF)} \leq V_{DD(INTREGD)}$ | $0.7V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.3 | V |
| | | $V_{DD(INTF)} > V_{DD(INTREGD)}$ | $0.7V_{DD(INTF)}$ | - | $V_{DD(INTREGD)}$ + 0.3 | V |
| **Data lines: pins I/O, I/OUC, AUX1, AUX2, AUX1UC and AUX2UC** | | | | | | |
| $t_d$ | delay time | falling edge on pins I/O and I/OUC or vise versa | - | - | 200 | ns |
| $t_{w(pu)}$ | pull-up pulse width | | - | - | 100 | ns |
| $f_{io}$ | input/output frequency | on data lines | - | - | 1 | MHz |
| $C_i$ | input capacitance | on data lines | - | - | 10 | pF |
| **Data lines to the card: pins I/O, AUX1 and AUX2[4]** | | | | | | |
| $V_o$ | output voltage | inactive mode | | | | |
| | | no load | 0 | - | 0.1 | V |
| | | $I_o$ = 1 mA | - | - | 0.3 | V |
| $I_o$ | output current | from data lines when in inactive mode with pins grounded | - | - | –1 | mA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 1 mA | 0 | - | 0.3 | V |
| | | $I_{OL} \geq$ 15 mA | $V_{CC}$ – 0.4 | - | $V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | no DC load | $0.9V_{CC}$ | - | $V_{CC}$ + 0.1 | V |
| | | $I_{OH}$ < –40 µA; 3 V | $0.75V_{CC}$ | - | $V_{CC}$ + 0.1 | V |
| | | $I_{OH}$ < –20 µA; 1.8 V or 1.2 V card | $0.75V_{CC}$ | - | $V_{CC}$ + 0.1 | V |
| | | current limit $I_{OH}$ = –15 mA | 0 | - | 0.4 | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = +3 V | –0.3 | - | +0.8 | V |
| | | $V_{CC}$ = +1.8 V | –0.3 | - | +0.6 | V |
| | | $V_{CC}$ = +1.2 V | –0.3 | - | +0.4 | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.6V_{CC}$ | - | $V_{CC}$ + 0.3 | V |
| $V_{hys}$ | hysteresis voltage | pin I/O | - | 350 | - | mV |
| $I_{IL}$ | LOW-level input current | pin I/O; $V_{IL}$ = 0 V | - | - | 600 | µA |

**Table 8. Characteristics of IC supply voltage** *…continued*

*$T_{amb}$ = 25 °C; all parameters remain within limits but are only statistically tested for the temperature range; $f_{xtal}$ = 10 MHz; all currents flowing into the IC are positive; unless otherwise specified. Parameters specified as a function of $V_{DD(INTF)}$, $V_{DD(REG)}$, $V_{DD(INTREGD)}$ or $V_{CC}$ refer to the actual value at the time of measurement.*



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IH}$ | HIGH-level input current | pin I/O; $V_{IH} = V_{CC}$ | - | - | 10 | µA |
| $t_{r(i)}$ | input rise time | $V_{IL}$ maximum to $V_{IH}$ minimum | - | - | 1.2 | µs |
| $t_{r(o)}$ | output rise time | $C_L \leq 80$ pF; 10 % to 90 %; 0 V to $V_{CC}$ | - | - | 0.1 | µs |
| $t_{f(i)}$ | input fall time | $V_{IL}$ maximum to $V_{IH}$ minimum | - | - | 1.2 | µs |
| $t_{f(o)}$ | output fall time | $C_L \leq 80$ pF; 10 % to 90 %; 0 V to $V_{CC}$ | - | - | 0.1 | µs |
| $R_{pu}$ | pull-up resistance | between I/O and $V_{CC}$ | 8 | 11 | 13 | kΩ |
| $I_{OH}$ | HIGH-level output current | pin I/O when active pull-up; $V_{OH} = 0.9V_{CC}$; C = 80 pF | –8 | –6 | –4 | mA |
| **Data lines to the system: pins I/OUC, AUX1UC and AUX2UC[5]** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 1 mA | 0 | - | 0.3 | V |
| $V_{OH}$ | HIGH-level output voltage | no DC load | $0.9V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.1 | V |
| | | $I_{OH} \leq 40$ µA; $V_{DD(INTF)} > 2$ V | $0.75V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.1 | V |
| | | $I_{OH} \leq 20$ µA; $V_{DD(INTF)} < 2$ V | $0.75V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.1 | V |
| $V_{IL}$ | LOW-level input voltage | | –0.3 | - | $+0.3V_{DD(INTF)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.3 | V |
| $V_{hys}$ | hysteresis voltage | pin I/OUC | - | $0.19V_{DD(INTF)}$ | - | V |
| $I_{IH}$ | HIGH-level input current | pin I/OUC; $V_{IH} = V_{DD(INTF)}$ | - | - | 10 | µA |
| $I_{IL}$ | LOW-level input current | pin I/OUC; $V_{IL}$ = 0 V | - | - | 600 | µA |
| $R_{pu}$ | pull-up resistance | between I/OUC and $V_{DD(INTF)}$ | 8 | 11 | 13 | kΩ |
| $t_{r(i)}$ | input rise time | $V_{IL}$ maximum to $V_{IH}$ minimum | - | - | 1.2 | µs |
| $t_{r(o)}$ | output rise time | $C_L \leq 80$ pF; 10 % to 90 %; 0 V to $V_{CC}$ | - | - | 0.1 | µs |
| $t_{f(i)}$ | input fall time | $V_{IL}$ maximum to $V_{IH}$ minimum | - | - | 1.2 | µs |
| $t_{f(o)}$ | output fall time | $C_L \leq 80$ pF; 10 % to 90 %; 0 V to $V_{CC}$ | - | - | 0.1 | µs |

**Table 8. Characteristics of IC supply voltage** *…continued*

*$T_{amb}$ = 25 °C; all parameters remain within limits but are only statistically tested for the temperature range; $f_{xtal}$ = 10 MHz; all currents flowing into the IC are positive; unless otherwise specified. Parameters specified as a function of $V_{DD(INTF)}$, $V_{DD(REG)}$, $V_{DD(INTREGD)}$ or $V_{CC}$ refer to the actual value at the time of measurement.*



| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ | HIGH-level output current | pin I/OUC when active pull-up; $V_{OH} = 0.9V_{DD}$; C = 30 pF | | –1 | - | - | mA |
| **Internal oscillator** | | | | | | | |
| $f_{osc(int)}$ | internal oscillator frequency | inactive mode | | 55 | 140 | 200 | kHz |
| | | active mode | | 1.9 | 2.7 | 3.2 | MHz |
| **Reset output to the card: pin RST** | | | | | | | |
| $V_o$ | output voltage | inactive mode | | | | | |
| | | no load | | 0 | - | 0.1 | V |
| | | $I_o$ = 1 mA | | - | - | 0.3 | V |
| $I_o$ | output current | when inactive and pin RST grounded | | 0 | - | –1 | mA |
| $t_d$ | delay time | between pins RSTIN and RST; RST enabled | | - | - | 2 | µs |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 200 µA | | 0 | - | 0.2 | V |
| | | current limit $I_{OL}$ = 20 mA | | $V_{CC}$ – 0.4 | - | $V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –200 µA | | $0.9V_{CC}$ | - | $V_{CC}$ | V |
| | | current limit $I_{OH}$ = –20 mA | | 0 | - | 0.4 | V |
| $t_r$ | rise time | $C_L$ = 100 pF; $V_{CC}$ = 3 V, 1.8 V or 1.2 V | [6] | - | - | 0.1 | µs |
| $t_f$ | fall time | $C_L$ = 100 pF; $V_{CC}$ = 3 V, 1.8 V or 1.2 V | [6] | - | - | 0.1 | µs |
| **Clock output to the card: pin CLK** | | | | | | | |
| $V_o$ | output voltage | inactive mode | | | | | |
| | | no load | | 0 | - | 0.1 | V |
| | | $I_o$ = 1 mA | | - | - | 0.3 | V |
| $I_o$ | output current | pin CLK when inactive and grounded | | 0 | - | –1 | mA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 200 µA | | 0 | - | 0.3 | V |
| | | current limit $I_{OL}$ = 70 mA | | $V_{CC}$ – 0.4 | - | $V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –200 µA | | $0.9V_{CC}$ | - | $V_{CC}$ | V |
| | | current limit $I_{OH}$ = –70 mA | | 0 | - | 0.4 | V |
| $t_r$ | rise time | $C_L$ = 30 pF | [6] | - | - | 16 | ns |
| $t_f$ | fall time | $C_L$ = 30 pF | [6] | - | - | 16 | ns |
| δ | duty cycle | except for $f_{xtal}$; $C_L$ = 30 pF | [6] | 45 | - | 55 | % |
| SR | slew rate | rise and fall; $C_L$ = 30 pF; $V_{CC}$ = 3 V or 1.8 V | | 0.2 | - | - | V/ns |
| | | $C_L$ = 30 pF; $V_{CC}$ = 1.2 V | | 0.1 | - | - | V/ns |

**Table 8. Characteristics of IC supply voltage** *…continued*

*$T_{amb}$ = 25 °C; all parameters remain within limits but are only statistically tested for the temperature range; $f_{xtal}$ = 10 MHz; all currents flowing into the IC are positive; unless otherwise specified. Parameters specified as a function of $V_{DD(INTF)}$, $V_{DD(REG)}$, $V_{DD(INTREGD)}$ or $V_{CC}$ refer to the actual value at the time of measurement.*



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Control inputs: pins CLKDIV1, CLKDIV2, CMDVCCN, RSTIN, VCC_SEL2, VCC_SEL1 and ENCLKIN[7]** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | –0.3 | - | +0.3$V_{DD(INTF)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7$V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.3 | V |
| $V_{hys}$ | hysteresis voltage | control inputs | - | 0.14$V_{DD(INTF)}$ | - | V |
| $I_{IL}$ | LOW-level input current | $V_{IL}$ = 0 V | - | - | 1 | µA |
| $I_{IH}$ | HIGH-level input current | $V_{IH}$ = $V_{DD(INTF)}$ | - | - | 1 | µA |
| **Control inputs CMDVCCN and CONFIG[7]** | | | | | | |
| $f_{CMDVCCN}$ | frequency on pin CMDVCCN | | - | - | 150 | kHz |
| $V_{IL}$ | LOW-level input voltage | | –0.3 | - | +0.3$V_{DD(INTF)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7 $V_{DD(INTREGD)}$ | - | $V_{DD(INTREGD)}$ + 0.3 | V |
| $V_{hys}$ | hysteresis voltage | pin CONFIG | - | 0.14$V_{DD(INTF)}$ | - | V |
| $I_{IL}$ | LOW-level input current | $V_{IL}$ = 0 V | - | - | 1 | µA |
| $I_{IH}$ | HIGH-level input current | $V_{IH}$ = $V_{DD(INTREGD)}$ | - | - | 1 | µA |
| **Card detection inputs: pins PRES and PRESN[7][8][9]** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | –0.3 | - | +0.3$V_{DD(INTREGD)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7 $V_{DD(INTREGD)}$ | - | $V_{DD(INTREGD)}$ + 0.3 | V |
| $V_{hys}$ | hysteresis voltage | pins PRES and PRESN | - | 0.17 $V_{DD(INTREGD)}$ | - | V |
| $I_{IL}$ | LOW-level input current | $V_{IL}$ = 0 V | - | - | 5 | µA |
| $I_{IH}$ | HIGH-level input current | $V_{IH}$ = $V_{DD(INTREGD)}$ | - | - | 5 | µA |
| **OFFN output[10]: pin OFFN** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 2 mA | 0 | - | 0.3 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –15 µA | 0.75$V_{DD(INTF)}$ | - | - | V |
| $R_{pu}$ | pull-up resistance | to $V_{DD}$ | 16 | 20 | 24 | kΩ |

[1] Two decoupling capacitors connected in parallel to $V_{DD(INTREGD)}$ rated at 100 nF and 1 µF.

[2] To enable the microcontroller to provide the required maximum voltage input level on XTAL1, $V_{DD(INTF)}$ must not exceed $V_{DD(INTREGD)}$ + 0.3 V. See Section 8.1 on page 7 for specific limitations on the maximum $V_{DD(INTF)}$ voltage and Table 8 on page 23 for the limits of XTAL1.



[3] To meet these specifications, $V_{CC}$ should be decoupled to pin CGND using two low ESR, ceramic multilayer capacitors one of 470 nF and one of 220 nF with an ESR of < 100 mΩ.

[4] Using the internal pull-up resistor to $V_{CC}$.

[5] Using the internal pull-up resistor to $V_{DD(INTF)}$.

[6] The transition time and the duty factor definitions are shown in Figure 16 on page 30; δ = t1/(t1 + t2).

[7] Pins PRESN and CMDVCCN are active LOW. Pins RSTIN and PRES are active HIGH; see Table 4 on page 12 for pins CLKDIV1 and CLKDIV2; see Table 5 on page 19 for pins VCC_SEL1 and VCC_SEL2.

[8] If PRESN or PRES is true, the card is considered to be present. A debouncing feature of 4.5 ms typical is built-in.

[9] Pin PRES has an integrated current source to pin GND, pin PRES to $V_{DD(INTREGD)}$; the card is considered as present if at least one of the two inputs is true.

[10] Pin OFFN is an NMOS drain, using an internal pull-up resistor to $V_{DD(INTREGD)}$.

**Table 9. Protection characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CC}$ | supply current | shutdown current on pin $V_{CC}$ | 95 | 135 | 185 | mA |
| | | pin $V_{CC}$ | 135 | 175 | 225 | mA |
| | | pin CLK | –70 | - | +70 | mA |
| | | pin RST | –20 | - | +20 | mA |
| $I_{IO}$ | input/output current | pins I/O, AUX1 and AUX2 | –15 | - | +15 | mA |
| $T_{sd}$ | shutdown temperature | | - | 150 | - | °C |

**Table 10. Timing characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{act}$ | activation time | total sequence with the crystal oscillator | [1] | 35 | - | 3000 | µs |
| | | external clock | [2] | 35 | - | 240 | µs |
| $t_{deact}$ | deactivation time | total sequence | [3] | 35 | 80 | 100 | µs |
| $t_d$ | delay time | CLK sent to a card with the crystal oscillator | | | | | |
| | | $t_{d(start)}$ = t3 | [1] | 35 | - | 3000 | µs |
| | | $t_{d(end)}$ = t5 | [1] | 160 | - | 3090 | µs |
| | | CLK sent to card using an external clock | | | | | |
| | | $t_{d(start)}$ = t3 | [2] | 35 | - | 150 | µs |
| | | $t_{d(end)}$ = t5 | [2] | 160 | - | 240 | µs |
| $t_{deb}$ | debounce time | on pins PRES and PRESN | [4] | 3.2 | 4.5 | 12 | ms |

[1] See Figure 8 on page 15.

[2] See Figure 10 on page 16.

[3] See Figure 12 on page 18.

[4] See Figure 15 on page 21.

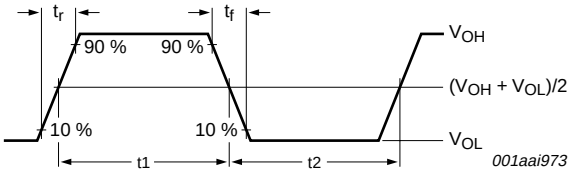
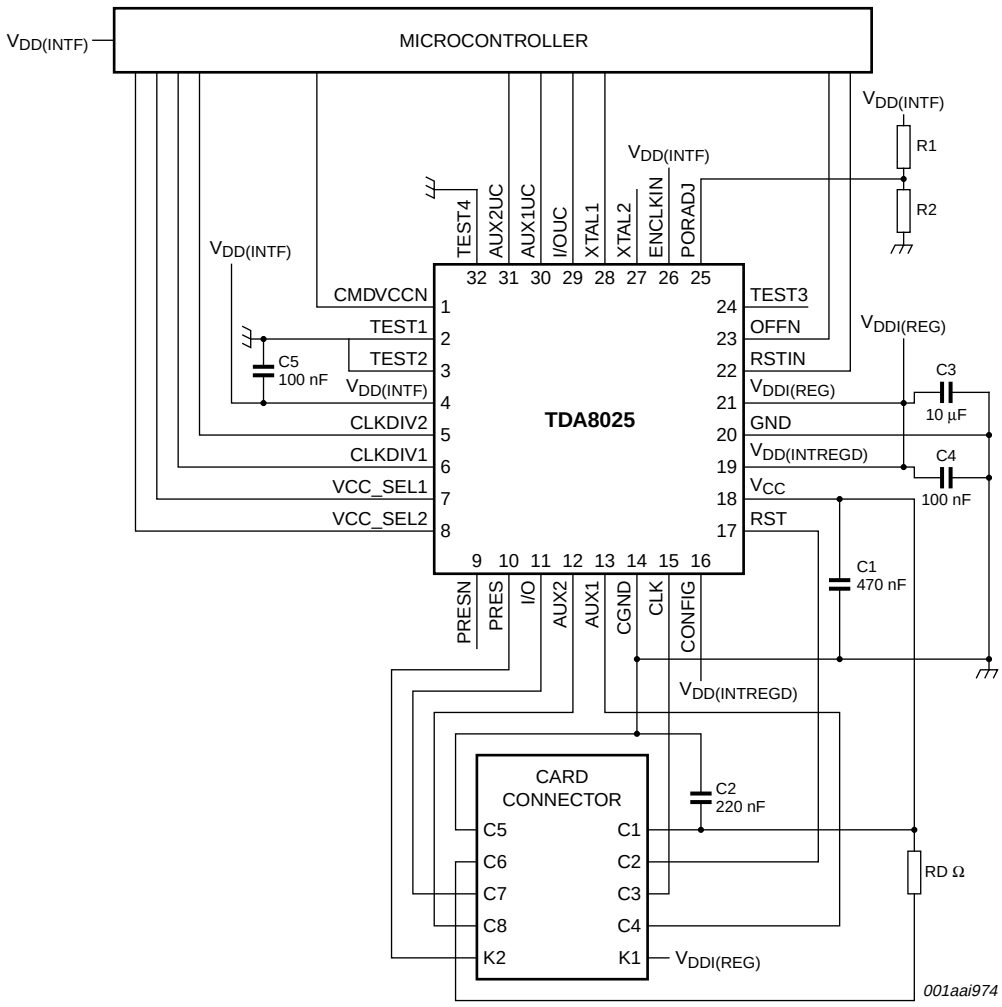



**Fig 16. Definition of output and input transition times**

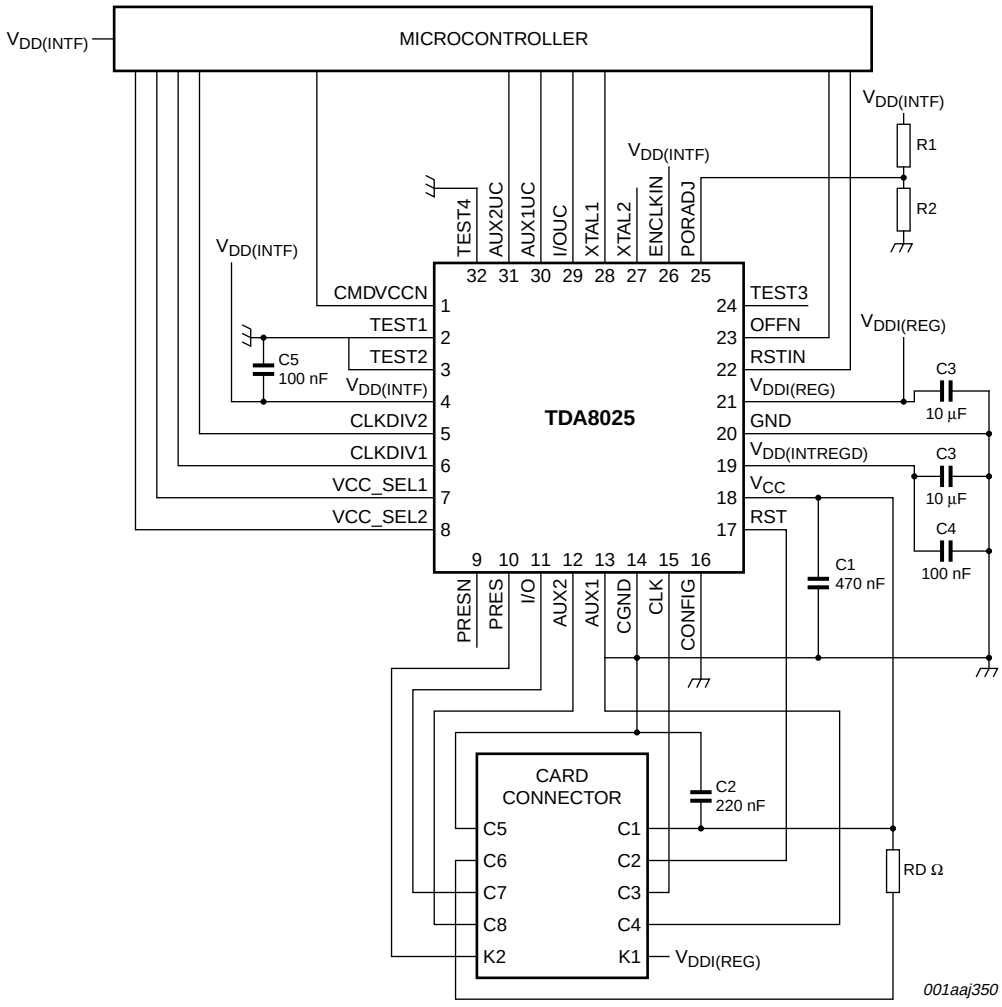
## 12. Application information






Refer to Table 8 on page 23 and Section 8.1 “Power supplies” on page 7 for detailed information on the $V_{DD(INTF)}$ restrictions.

**Fig 17. Application diagram (3 V < $V_{DDI(REG)}$ < 3.6 V)**



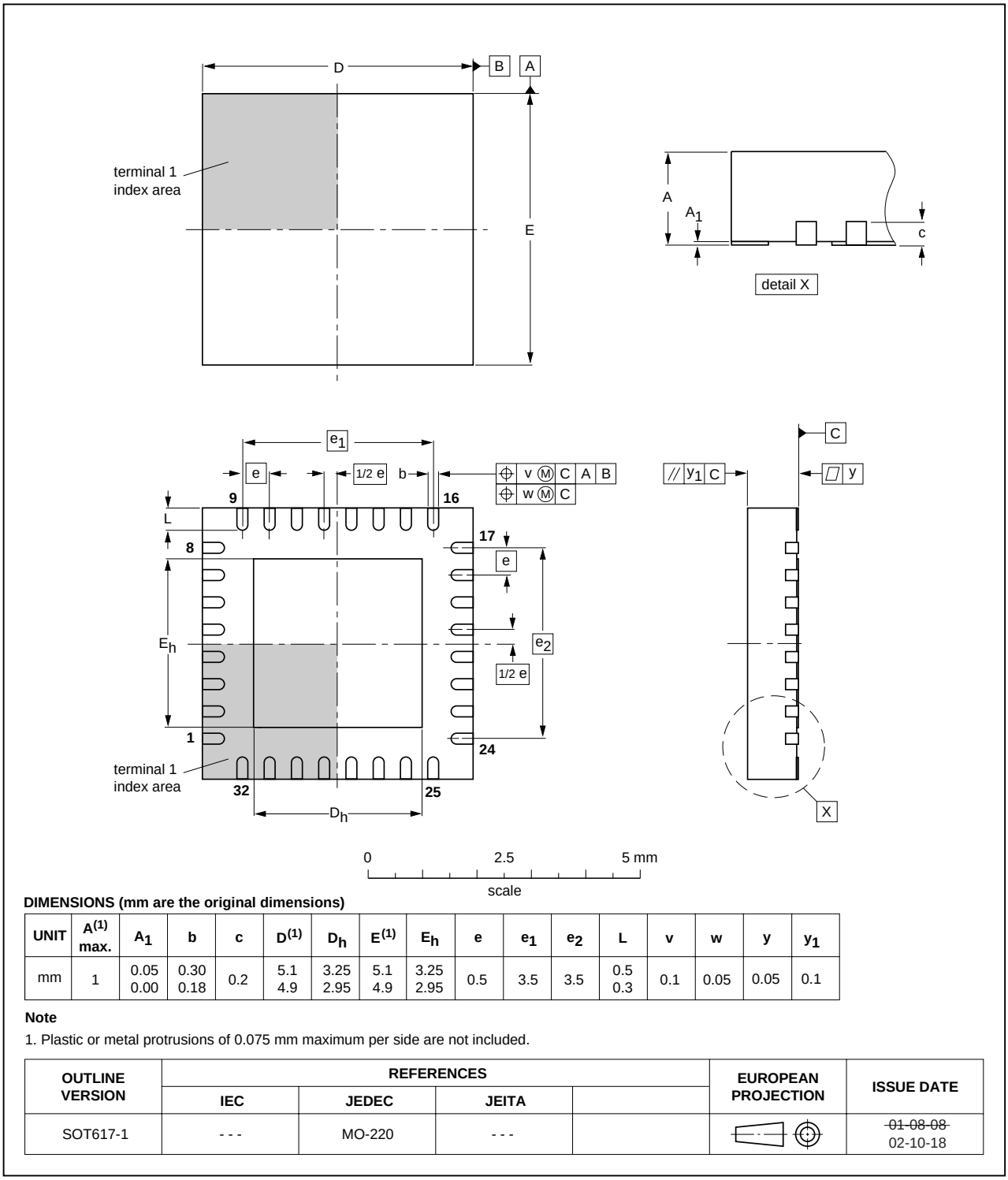

Refer to Table 8 on page 23 and Section 8.1 “Power supplies” on page 7 for detailed information on the $V_{DD(INTF)}$ restrictions.

**Fig 18. Application diagram (3.6 V < $V_{DDI(REG)}$ < 5.5 V)**

## 13. Package outline



**HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm** **SOT617-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 5.1<br>4.9 | 3.25<br>2.95 | 5.1<br>4.9 | 3.25<br>2.95 | 0.5 | 3.5 | 3.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT617-1 | - - - | MO-220 | - - - | | | ~~01-08-08~~<br>02-10-18 |

**Fig 19. Package outline SOT617-1**

# 14. Soldering of SMD packages



This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering



Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

**Table 11. SnPb eutectic process (from J-STD-020C)**

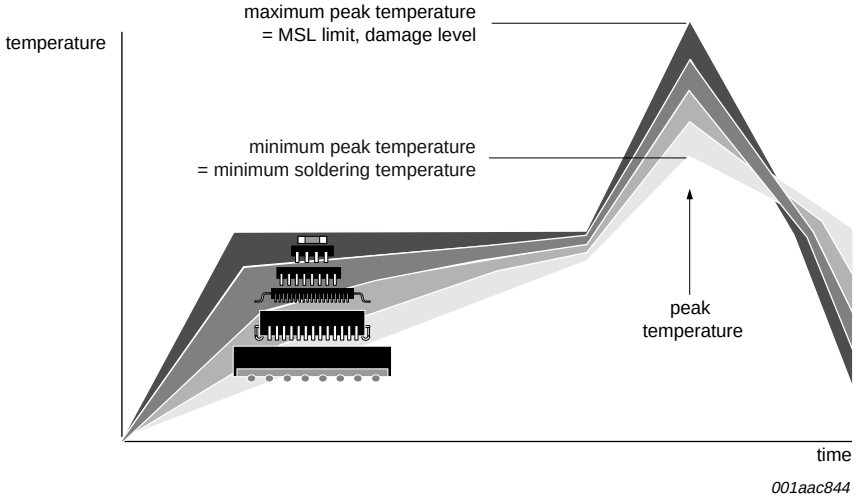
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 12. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.




MSL: Moisture Sensitivity Level

**Fig 20. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 15. Abbreviations

**Table 13. Abbreviations**

| Acronym | Description |
|---|---|
| ATR | Answer To Request |
| ESD | ElectroStatic Discharge |
| ESR | Equivalent Series Resistance |
| NMOS | Negative-channel Metal-Oxide Semiconductor |
| POR | Power-On Reset |
| PMOS | Positive-channel Metal-Oxide Semiconductor |

## 16. Revision history

**Table 14. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TDA8025_1 | 20090406 | Product data sheet | - | - |

# 17. Legal information



## 17.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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