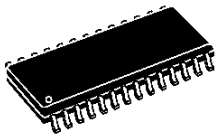
SGS-THOMSON MICROELECTRONICS

TDA7435

DIGITALLY CONTROLLED AUDIO PROCESSOR WITH LOUDSPEAKERS EQUALIZER

- INPUT
  - FOUR HIGH PASS CHANNELS
  - TWO AUX STEREO CHANNELS
- VOLUME CONTROL IN 1dB STEPS WITH GAIN UP TO 15dB
- SOFT MUTE AND DIRECT MUTE
- FOUR AUXILIARY CHANNELS:
  - TWO SPEAKERS CONTROL IN 1dB STEP
  - TWO CHANNELS MULTIPLEXED WITH THE HIGH PASS CHANNELS
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL I^2 CBUS



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ORDERING NUMBER: TDA7435D

DESCRIPTION

The audioprocessor TDA7435 is an upgrade of the TDA731X audioprocessor family.

Due to a highly linear signal processing, using CMOS-switching techniques instead of standard bipolar multipliers, very low distortion and very low noise are obtained.

A second programmable high pass filtering provides the loudspeakers equalization.

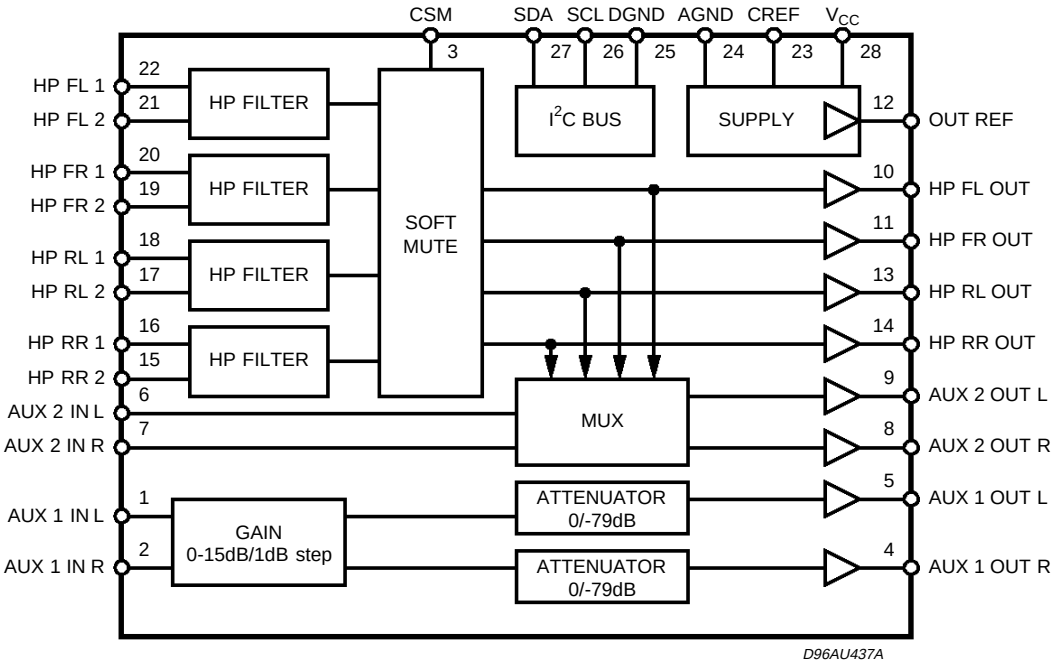
The soft Mute function is implemented andcan be activated in two ways:

1 Via serial bus (Mute byte, bit D0)

2 Directly on pin 3 through an I/O line of the microcontroller

Very low DC stepping is obtained by use of a BICMOS technology.

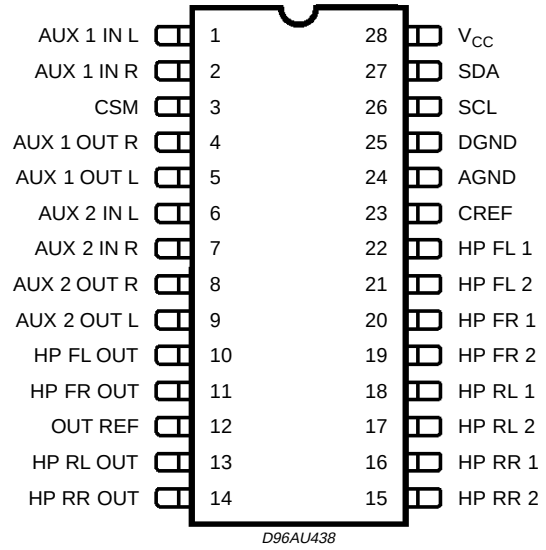
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

PIN CONNECTION



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THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-pins	65	°C/W

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	6	9	10.2	V
V_{CL}	Max. input signal handling	2.1	2.6		Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz		0.01	0.08	%
S/N	Signal to Noise Ratio		106		dB
S_C	Channel Separation f = 1KHz		80		dB
	Input Gain AUX1 1dB step	0		15	dB

ELECTRICAL CHARACTERISTICS (V_S = 9V; R_L = 10KΩ; R_g = 50Ω; T_{amb} = 25°C; all gains = 0dB; f = 1KHz. Refer to the test circuit, unless otherwise specified.)

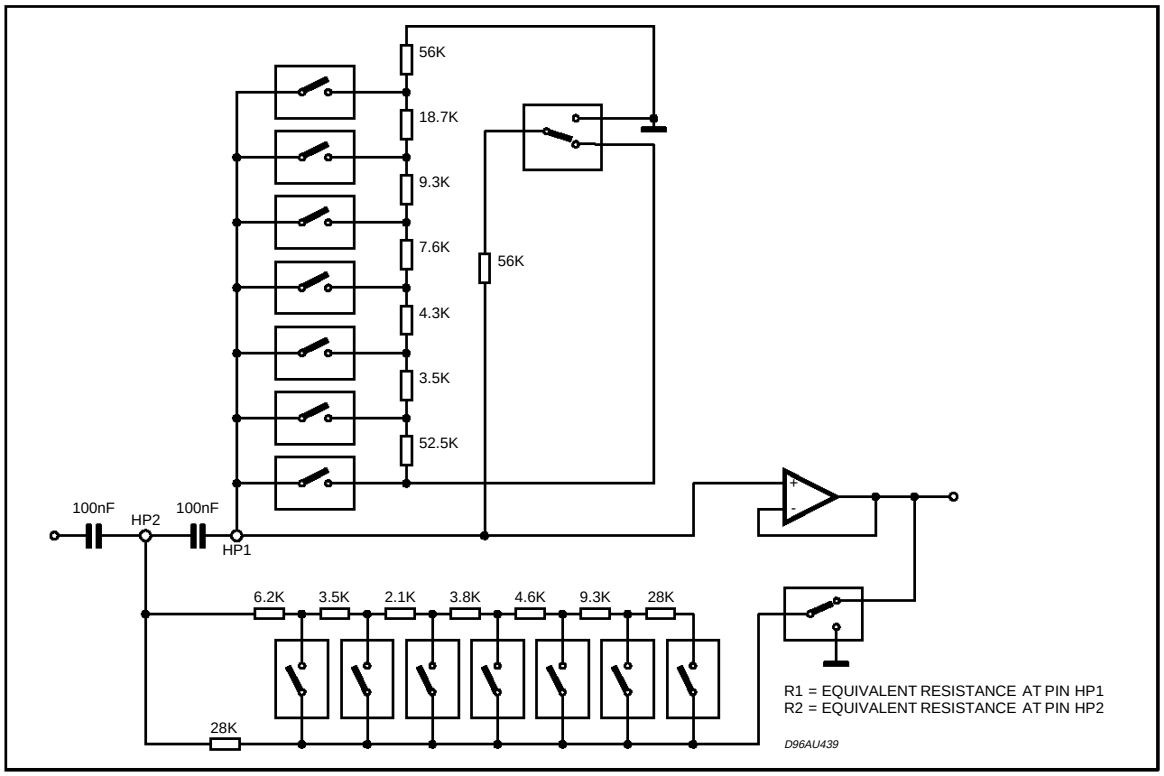
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT STAGE: AUX1						
R_I	Input Resistance		24	33	42	KΩ
V_{CL}	Clipping Level	d ≤ 0.3%	2.1	2.6		V_{RMS}
S_I	Input Separation		70	80		dB
$G_{I\ MIN}$	Minimum Input Gain		-0.75	0	0.75	dB
$G_{I\ MAX}$	Maximum Input Gain		13.75	15	16.25	dB
G_{step}	Step Resolution		0.5	1.0	1.5	dB
E_a	Set Error		-1.25	0	1.25	dB
V_{DC}	DC Steps	Adiacent Gain Steps		0.5	10	mV
		G_{IIN} to G_{IMAX}		2.5		mV
SPEAKER ATTENUATORS - AUX 1						
C_{RANGE}	Control Range			79		dB
A_{step}	Step Resolution	Av = 0 to -40dB	0.5	1	1.5	dB
A_{MUTE}	Output Mute Attenuation	Data Word = 1111XXXX	80	105		dB
E_A	Attenuation Set Error	Av = 0 to -40dB			1.5	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps		0	3	mV
AUDIO OUTPUT (Pin 4 - 5, 8 - 9, 10 - 14)						
V_{clip}	Clipping Level	d = 0.3%	2.1	2.6		Vrms
R_L	Output Load Resistance		2			KΩ
R_O	Output Impedance		20	30	100	Ω
V_{DC}	DC Voltage Level		3.5	3.8	4.1	V
STAGE: AUX2						
R_I	Input Resistance		24	33	42	KΩ
V_{CL}	Clipping Level		2.1	2.6		Vrms
S_I	Input Separation		70	80		dB
G_I	Gain		-0.75	0	0.75	dB
	Input Mute		80	100		dB
STAGE: HP FILTER						
R1	Resistance at pin HP1	HIGHPASS BYTE D3 = 1 XXXX1XXX	120	170	220	KΩ
R2	Resistance at pin HP2			1		MΩ
V_{CL}	Clipping Level	d ≤ 0.3%	2.1	2.6		Vrms
SOFT MUTE						
A_{MUTE}	Mute Attenuation		40	50		dB
T_{DON}	ON Delay Time	C_{CSM} = 22nF; 0 to -20dB; I = I_{MAX}	0.7	1	2	ms
		C_{CSM} = 22nF; 0 to -20dB; I = I_{MIN}	10	30	50	ms
T_{DOFF}	OFF Current	V_{CSM} = 0V; I = I_{MAX}	60		160	µA
		V_{CSM} = 0V; I = I_{MIN}	110		210	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{THSM}	Soft Mute Threshold			2.3		V
R_{INT}	Pullup Resistor (pin 3)	(note 2)		100		KΩ
V_{SMH}	(pin 3) Level High		3.5			V
V_{SML}	(pin 3) Level Low	Soft Mute Active			1	V
GENERAL						
V_{CC}	Supply Voltage		6	9	10.2	V
I_{CC}	Supply Current		7	11	15	mA
PSRR	Power Supply Rejection Ratio	f = 1KHz	60	70		dB
e_{NO}	Output Noise	Output Muted (B = 20 to 20kHz flat)		3.5		µV
		All Gains 0dB (B = 20 to 20kHz flat)		5	15	µV
S/N	Signal to Noise Ratio	All Gains = 0dB; V_O = 1V_{rms}		106		dB
S_C	Channel Separation		70	80		dB
d	Distortion	V_{IN} =1V		0.01	0.08	%
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IN}	Input High Voltage		3			V
I_{IN}	Input Current	VIN = 0.4V	-5		5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

Note 1: WIN represents the MUTE programming bit pair D_6, D_5 for the zero crossing window threshold
Note 2: Internall pullup resistor to Vs/2; "LOW" = softmute active

Figure 1: HP Filter.



I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7435 and viceversa takes place thru the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

Data Validity

As shown in fig. 2, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.3 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.
A STOP conditions must be sent before each START condition.

Byte Format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 4). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.
The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.
This approach of course is less protected from misworking and decreases the noise immunity.

Figure 2: Data Validity on the I²CBUS

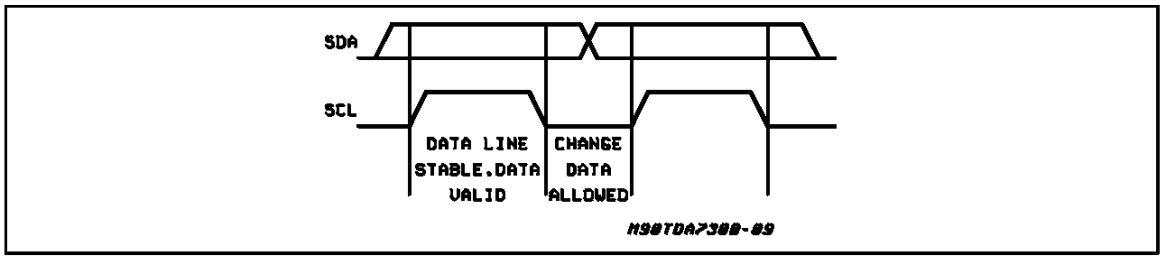


Figure 3: Timing Diagram of I²CBUS

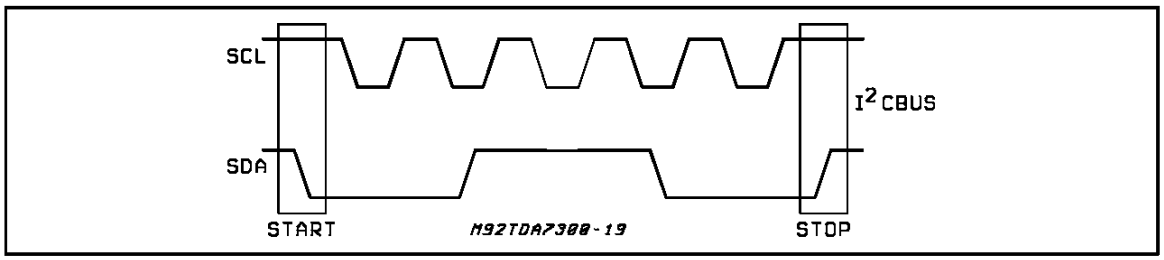
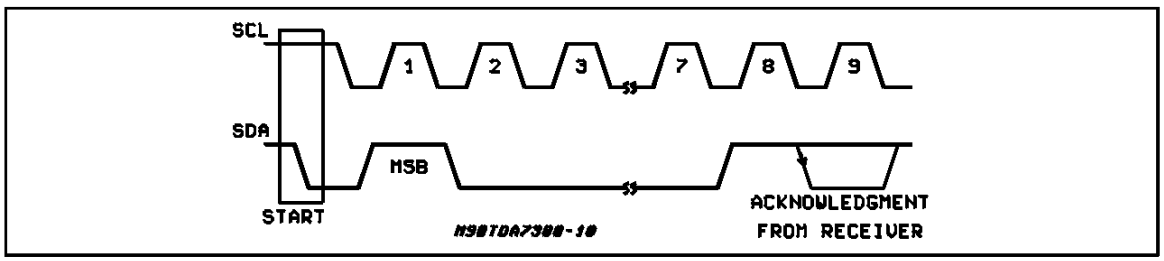


Figure 4: Acknowledge on the I²CBUS

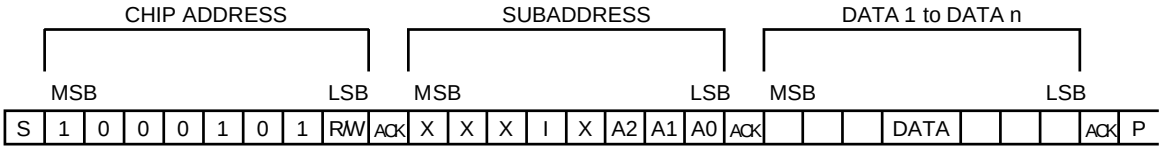


SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte,(the LSB bit determines read/write transmission)
- A subaddress byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge
S = Start
P = Stop
I = Auto Increment
X = Not used

MAX CLOCK SPEED 500kbits/s

AUTO INCREMENT

If bit I in the subaddress byte is set to "1", the autoincrement of the subaddress is enabled

SUBADDRESS (receive mode)

MSB							LSB	FUNCTION
X	X	X	I	X	D2	D1	D0	
					0	0	0	Mux & Gain
					0	0	1	Mute
					0	1	0	Speaker Attenuator AUX 1 L
					0	1	1	Speaker Attenuator AUX 1 R
					1	0	0	High Pass Filter FL
					1	0	1	High Pass Filter FR
					1	1	0	High Pass Filter RL
					1	1	1	High Pass Filter RR

TRANSMITTED DATA

Send Mode

MSB							LSB
X	X	X	X	X	SM	X	X

SM = Soft mute activated (HIGH active)
X = Not used

The transmitted data is automatically updated after each ACK.
Transmission can be repeated without new chipaddress.

DATA BYTE SPECIFICATION

MUX & GAIN

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								AUX 1 Input Gain
				0	0	0	0	0dB
				0	0	0	1	1dB
				0	0	1	0	2dB
				0	0	1	1	3dB
				0	1	0	0	4dB
				0	1	0	1	5dB
				0	1	1	0	6dB
				0	1	1	1	7dB
				1	0	0	0	8dB
				1	0	0	1	9dB
				1	0	1	0	10dB
				1	0	1	1	11dB
				1	1	0	0	12dB
				1	1	0	1	13dB
				1	1	1	0	14dB
				1	1	1	1	15dB
								AUX 2 Output Selection
		0	0					High Pass Filter Front
		0	1					High Pass Filter Rear
		1	0					Aux 2 Input
		1	1					Mute

Mute

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
						0	0	Soft mute - SLOW SLOPE
						0	1	Soft mute - FAST SLOPE
						0		Soft mute ON
						1		Soft mute OFF
					0	0		AUX 1 Input Mute Enabled
					1	0		AUX 1 Input Mute Disabled

Speaker

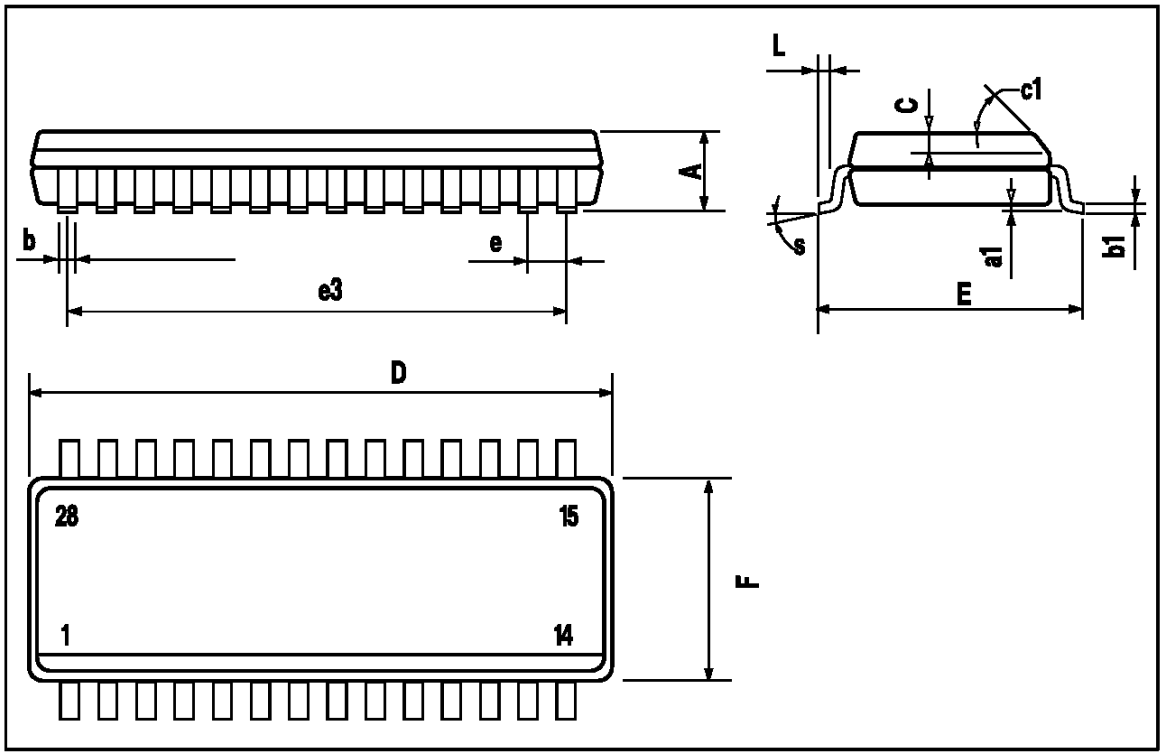
MSB							LSB	AUX 1 L, R
D7	D6	D5	D4	D3	D2	D1	D0	
								-1dB STEPS
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
								-8dB STEPS
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	0	1	1	0				-48dB
	0	1	1	1				-56dB
	1	0	0	0				-64dB
	1	0	0	1				-72dB
	1	0	0					MUTE
	1	0	1					
	1	1	1					

HIGH PASS FILTERS

MSB							LSB	FL, FR, RL, RR
D7	D6	D5	D4	D3	D2	D1	D0	
								2nd order HP Filter Mode (C1 = C2 = 100nF)
				0	0	0	0	f_c = 40Hz
				0	0	0	1	f_c = 60Hz
				0	0	1	0	f_c = 80Hz
				0	0	1	1	f_c = 100Hz
				0	1	0	0	f_c = 120Hz
				0	1	0	1	f_c = 150Hz
				0	1	1	0	f_c = 180Hz
				0	1	1	1	f_c = 220Hz
								First order HP Flat Mode
				1				f_c = 9Hz

SO28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					



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