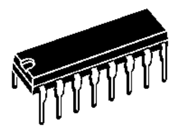
SGS-THOMSON MICROELECTRONICS

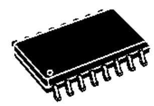
TDA7326

AM-FM RADIO FREQUENCY SYNTHESIZER

- FM INPUT AND PRECOUNTER FOR UP TO 140MHz
- AM INPUT FOR UP TO 40MHz
- 6-BIT SWALLOW COUNTER, 8-BIT PROGRAMMABLE COUNTER FOR FM AND SW
- 14-BIT PROGRAMMABLE COUNTER FOR LW AND MW
- THREE WIRES 8-BIT SERIAL INTERFACE
- ON-CHIP REFERENCE OSCILLATOR AND COUNTER
- PROGRAMMABLE SCANNING STEPS FOR AM AND FM
- DIGITAL PHASE DETECTOR AND LOOP FILTER
- TWO SEPARATE FREE PROGRAMMABLE FILTER APPLICATIONS AVAILABLE
- TUNING VOLTAGE OUTPUT 0.5 TO 9.5V
- PROGRAMMABLE CURRENT SOURCES TO SET THE LOOP GAIN
- ON-CHIP POWER ON RESET
- STANDBY MODE



DIP16



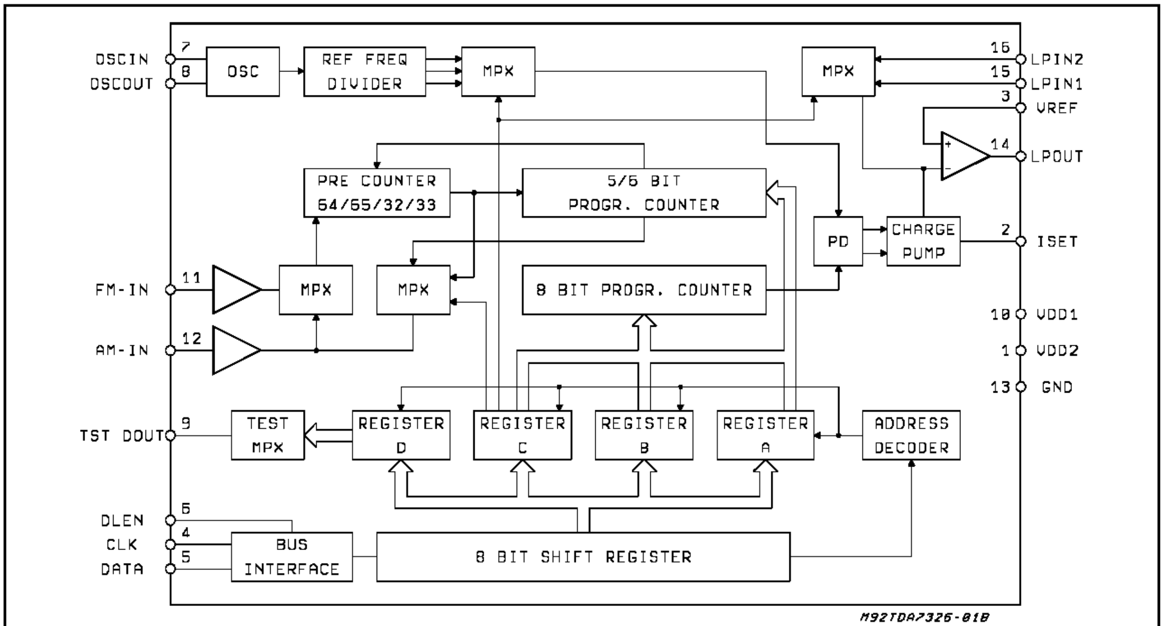
SO16W

ORDERING NUMBERS: TDA7326 (DIP16)
TDA7326D (SO16W)

DESCRIPTION

The TDA7326 is a PLL frequency synthesizer in CMOS technology that performs all the function of a PLL radio tuning system for FM and AM (LW, MW, SW)

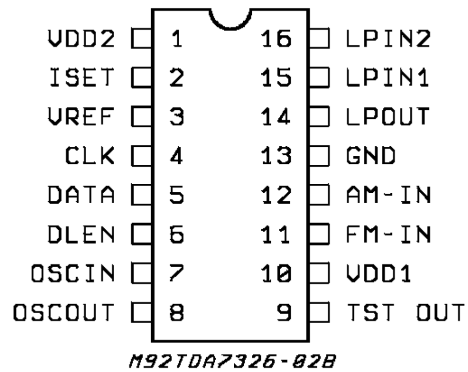
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD1} - V_{SS}	Supply Voltage	- 0.3 to + 7	V
V_{DD2} - V_{SS}	Supply Voltage	- 0.3 to + 12	V
V_{IN}	Input Voltage	VSS - 0.3 to V_{DD} + 0.3	V
V_{OUT}	Output Voltage	VSS - 0.3 to V_{DD} + 0.3	V
I_{IN}	Input Current	- 10 to + 10	mA
I_{OUT}	Output Current	- 10 to + 10	mA
T_{stg}	Storage Temperature	- 55 to + 125	^oC
T_A	Ambient Temperature	-40 to + 85	^oC

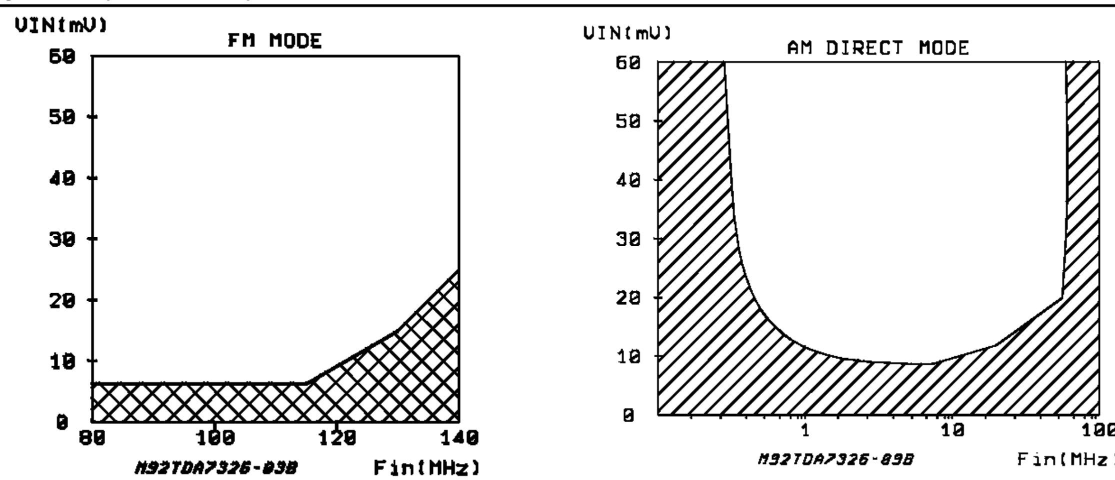
PIN CONNECTION



THERMAL DATA

Symbol	Parameter	DIP 16	SO 16L	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	100	200	°C/W

Figure 1: Input Sensitivity



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ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C ; V_{DD1} = 5V; V_{DD2} = 9V f_{OSC} = 4MHz; R_{ISET} = 68KΩ; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD1}	Supply Voltage		4.5	5.0	5.5	V
V_{DD2}	Supply Voltage			9.0	10.0	V
$I_{DD1\ FM}$	Supply Current	no output load, FM mode, f_{in} = 100MHz	10	18	25	mA
$I_{DD1\ AM}$	Supply Current	no output load, AM mode, fin = 1MHz	3	5	10	mA
$I_{DD1\ STB}$	Supply Current	Standby mode		3	20	µA
I_{DD2}	Supply Current		0.5	2	3	mA
V_{REF}	Voltage at pin 3		3.0	3.5	4.0	V
V_{iSET}	Voltage at pin 2	RiSET = 68KΩ	7.0	8.0	9.0	V

RF INPUT (AMIN FMIN)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{iAM}	Input Frequency AM	Direct Mode, V_{in} = 50mV	0.5		20	MHz
		Swallow Mode, V_{in} = 50mV	16		40	MHz
f_{iFM}	Input Frequency FM	Sinus, V_{in} = 50mV	30		140	MHz
V_{iAM}	Input Voltage AM	Direct Mode 0.6 to 16MHz (Sinus)	40		600	mVrms
		Swallow Mode 16 to 40MHz (Sinus)	40		600	mVrms
V_{iFM}	Input Voltage FM	70 to 120MHz (Sinus)	30		600	mVrms
Z_{in}	Input Impedance FM	fin = 120MHz		200		Ω
Z_{in}	Input Impedance AM	fin = 12MHz		1400		Ω

OSCILLATOR

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{OSC}	Oscillator Frequency			4		MHz
t_{bu}	Built Up Time	Euro-Quartz ITT			100	ms
C_{in}	Internal Capacitance			9		pF
C_{OUT}	Internal Capacitance			9		pF
Z_{in}	Input Impedance			4	15	KΩ
V_{in}	Input Voltage		0.5		V_{DD1}	Vpp

PLL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{step}	Step Width AM			1/2.5		KHz
f_{step}	Step Width FM			12.5/25		KHz
f_{ref}	Ref Frequency AM			1/2.5		KHz
f_{ref}	Ref Frequency FM			12.5/25		KHz

LOOP FILTER INPUT (LP_{IN1}, LP_{IN2} = PIN 15,16)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$-I_{in}$	Input Leakage Current	VIN = V_{SS}; Phase Detector Output = Tristate	-1	-0.1		µA
I_{in}	Input Leakage Current	VIN = V_{DD}; Phase Detector Output = Tristate		0.1	+1	µA

ELECTRICAL CHARACTERISTICS (continued)

LOOP FILTER OUTPUT (LP_{OUT} = PIN 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OL}	Output Voltage Low	ILOAD = 0.2mA V_{DD2}; = 10V		0.5	0.8	V
V_{OH}	Output Voltage High	-ILOAD = 0.2mA V_{DD2}; = 10V	9	9.5		V
CHARGE PUMP CURRENT GENERATION (LP_{IN1}, LP_{IN2} = PIN 15, 16)						
I_{si}	Sink Current LPIN1,2	CURR1 = 0, CURR2 = 0	2	5	7	µA
		CURR1 = 0, CURR2 = 1	120	200	280	µA
		CURR1 = 1, CURR2 = 1	180	300	420	µA
		CURR1 = 1, CURR2 = 0	370	500	630	µA
$-I_{so}$	Source Current LPIN1,2	CURR1 = 0, CURR2 = 0	2	5	7	µA
		CURR1 = 0, CURR2 = 1	120	200	280	µA
		CURR1 = 1, CURR2 = 1	180	300	420	µA
		CURR1 = 1, CURR2 = 0	370	500	630	µA
DOUT1 OPENDRAIN OUTPUT(PIN 9)						
V_{OL}	Output Voltage Low	ILOAD = 1mA		0.2	0.5	V
BUS INTERFACE						
$-I_{IL}$	Input Leakage Current	VIN = V_{SS}	-1	0.1	1	µA
I_{IH}	Input Leakage Current	VIN = V_{SS}	-1	0.1	1	µA
V_{IH}	Input Voltage High	Leading edge	3.4	4.0		V
V_{IL}	Input Voltage Low	Leading edge		1.0	1.6	V
BUS INTERFACE, WAITING TIME (see fig. 5) The Data is Acquired at the High → Low Clock Transition						
t_1	CLK Low to DLEN L → H		0.2			µs
t_3	DATA Transition to CLK H → L		0.1			µs
t_5	CLK H → L to DATA Transition		0.4			µs
BUS INTERFACE, DATA REPETITION TIME (see fig. 5)						
t_{r1}	Release Time Between 2 bytes, except byte 4		5			µs
t_{r2}	Release Time after the transmission of byte 4	FM mode	180			µs
		AM mode	2			ms
BUS INTERFACE, SETUP TIME (see fig. 5)						
t_2	DLEN High to CLK L → H		0.1			µs
BUS INTERFACE, HOLD TIME (see fig. 5)						
t_4	DATA Transition to CKL L → H		0			µs
t_6	CLK H → L to DLEN H → L		0.4			µs
f_{CLK}	CLK Frequency				500	KHz
	Duty Cycle			50		%
t_{pl}	Clock Pulse Low		1			µs
t_{ph}	Clock Pulse High		1			µs

2.0 GENERAL DESCRIPTION

This circuit contains a frequency synthesizer and a loop filter for an FM and AM radio tuning system. Only a V_{CO} is required to build a complete PLL system.
For FM and SW application, the counter works in a two stages configuration.
The first stage is a swallow counter with a four modulus (:32/33/64/65) precounter.
The second stage is an 8-bit programmable counter.
For LW and MW application, a 14-bit programmable counter is available.
The circuit receives the scaling factors for the programmable counters and the values of the reference frequencies via a three line serial bus interface.
The reference frequency is generated by a 4MHz XTAL oscillator followed by the reference divider.
An external oscillator (f = 4MHz) can be used instead of the internal one; it must be connected to OSCIN (pin 7).
The reference step-frequency is 1 or 2.5kHz for AM. For FM mode a step frequency of 12.5 and 25kHz can be selected.
The circuit checks the format of the received data words.
Valid data in the interface shift register are stored automatically in buffer registers at the end of transmission.
The output signals of the phase detector are switching the programmable current sources.
Their currents are integrated in the loop filter to a DC voltage.The values of the current sources are programmable by two bits also received via the serial bus.
The loop filter amplifier is supplied by a separate positive power supply, to minimize the noise induced by the digital part of the system.
The loop gain can be set for different conditions.
After a power on reset, all registers are reset to zero and the standby mode is activated.
In standby mode, oscillator, reference counter, AM input and FM input are stopped. The power consumption is reduced to a minimum.

3.0 DETAILED DESCRIPTION OF THE PLL FREQUENCY SYNTHESIZER

3.1 INPUT AMPLIFIERS

The signals applied on AM and FM input are amplified to get a logic level in order to drive the frequency dividers.

3.1.1 Input Impedance

The typical input impedance: for the FM input is 200Ω and for AM input is 1.4kΩ.

3.1.2 Input sensitivity

(see Figures 1a and 1b).

3.2 DATA AND CONTROL REGISTER

3.2.1 Register Location

The data registers (bit2...bit7) for the control register and the data registers PC7...PC0, SC5...SC0 for the counters are organized in four words, identified by two address bits (bit 7 and bit 6), bit 7 is the first bit to be sent by the controller, bit0 is the last one. The order and the number of the bytes to be transmitted is free of choice. The modification of the PC7...PC0 registers is valid for the internal counters only after transmission of byte 4 (SC5...SC0).

3.2.2 CONTROL AND STATUS REGISTERS

Register Configuration

	ADDRESS BITS		DATA BITS					
BYTE	**MSB-BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**LSB BIT 0**
Function	adr 0	adr 1	data 0	data 1	data 2	data 3	data 4	data 5
byte 1	0	0	test 0	test 1	test 2	SOUT	CURR2	f_{REF}
byte 2	0	1	PC7	PC6	LPF1/2	CURR 1	SWM/DIR	AM/FM
byte 3	1	0	PC5	PC4	PC3	PC2	PC1	PC0
byte 4	1	1	SC5	SC4	SC3	SC2	SC1	SC0

REGISTER NAME	FUNCTION
SWM/DIR	Swallow direct-mode switch 1 = SWM, 0 = DIR
AM/FM	AM - FM band switch 1=AM, 0 = FM
f_{REF}	Selection of reference frequency (see table 3.4)
CURR1	Current select of change pump
CURR2	Current select of change pump
LPF1/LPF2	Loop filter input select 1= I_{PF1}, 0 = I_{PF2}
SOUT	Switch output condition 1=output high, 0 = output low

3.3 DIVIDER FROM V_{CO} FREQUENCY TO REFERENCE FREQUENCY

This divider provides a low frequency f_{SYN} which is phase compared with the reference frequency f_{REF}.

3.4 OPERATING MODE

Four operating modes are available:
- FM mode,
- AM swallow mode,
- AM direct mode,
- Standby mode

They are user programmable with the SWR/DIR and AM/FM bits in the byte 2.
Standby mode: all functions are stopped. This allows low current consumption without lost of information in all register, it is activated by forcing bit 0 (AM/FM) and bit 1 (SWM/DIR) both at zero value.

MODE SECTION	SWM/DIR	AM/FM
STAND-BY	0	0
FM	1	0
AM SWALLOW	0	1
AM DIRECT	1	1

3.4.1 FM and AM (SW) Operation (Swallow Mode)

The FM or AM signal is applied to a four modulus: 32/33/64/65 high speed prescaler, which is controlled by a 6 bit divider 'A'.This divider is controlled by the 6 bit SC register. In parallel the output of the prescaler is connected to a 8 bit divider 'B'. This divider is controlled by the 8 bit PC register. For FM mode with 25kHz reference frequency operation, the divider A is a 5 bit divider. The high speed prescaler is working in : 32/33 dividing mode. Bit 6 of the SC register has to be kept to "0".

Dividing range calculation :
For FM mode with 12.5kHz reference frequency and SW swallow mode operation :
$f_{VCO} = [\,65 \cdot A_1 + (B_1 + 1 - A_1) \cdot 64\,] \,.\, f_{REF}$ or

$$f_{VCO} = (64 \cdot B_1 + A_1 + 64) \cdot f_{REF}$$

Important : For correct operation B ≥ 64 and B ≥ A.
At FM mode with 25kHz reference frequency :
$f_{VCO} = [\,33 \cdot A_2 + (B_2 + 1 - A_2) \cdot 32\,] \cdot f_{REF}$

$$f_{VCO} = (32 \cdot B_2 + A_2 + 32) \cdot f_{REF}$$

Important: For correct operation B ≥ 32 and B ≥ A.
A and B are variable values of the dividers.
To keep the actual tuning frequency after a modification of the reference frequency, the values of the dividers have to be modified in the following way.
Switching from 25kHz to 12.5kHz reference frequency : $B_1 = B_2$, $A_1 = A_2 \cdot 2$
Switching from 12.5kHz to 25kHz reference frequency:

$$B_2 = B_1,\ A_2 = \frac{A_1}{2} \ \text{and}\ A_2 = \frac{(A_1 + 1)}{2}$$

for odd values A_1.

The AM signal is directly applied to the 14 bit static divider 'C'. This divider is controlled by both SC and PC registers.
Dividing range:

$$f_{VCO} = (C + 1) \cdot f_{REF}$$

Figure 2: FM and AM (SW) operation (swallow mode)

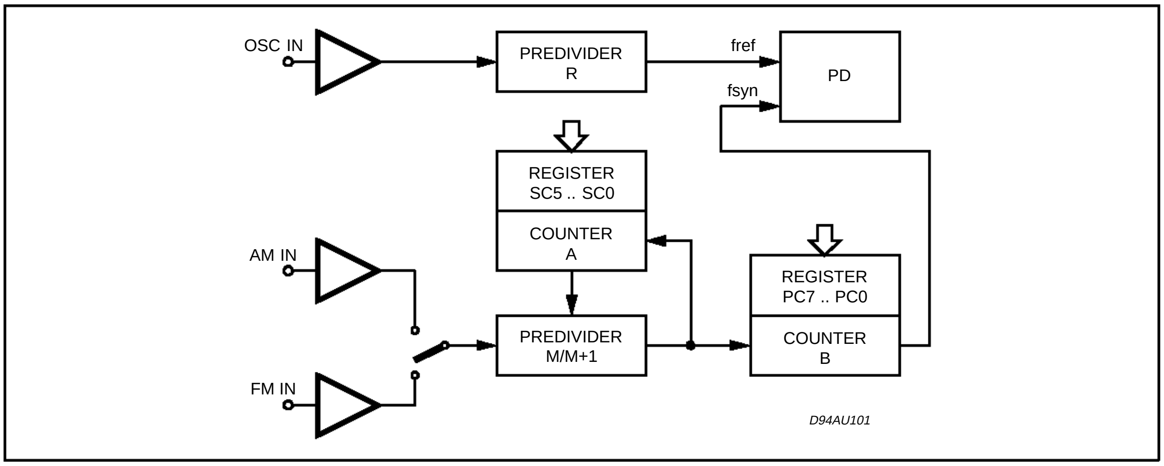

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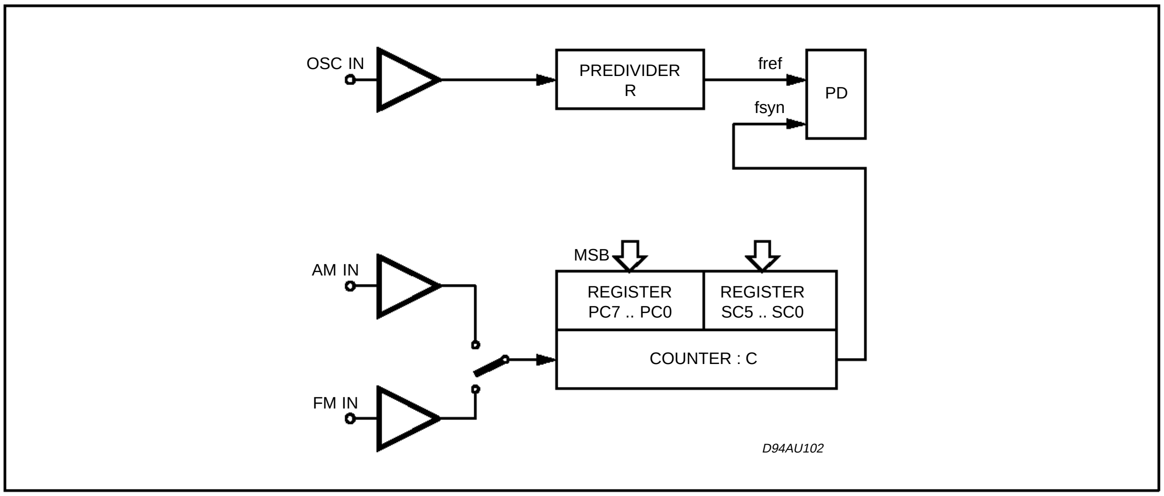
Figure 3: AM direct mode operation for SW, MW and LW



3.4 REFERENCE FREQUENCY GENERATOR

The crystal oscillator clock is divided by the reference frequency divider to provide the reference frequency to the phase comparator. Reference frequency divider range is selectable by the programming bit 'f_{REF}'.
Available reference frequency are shown in following table.

TABLE 3.4

AM/FM	f_{REF}	f_{REF} (kHz)
0	0	12.5
0	1	25
1	0	1
1	1	2.5

Figure 4: Phase comparator

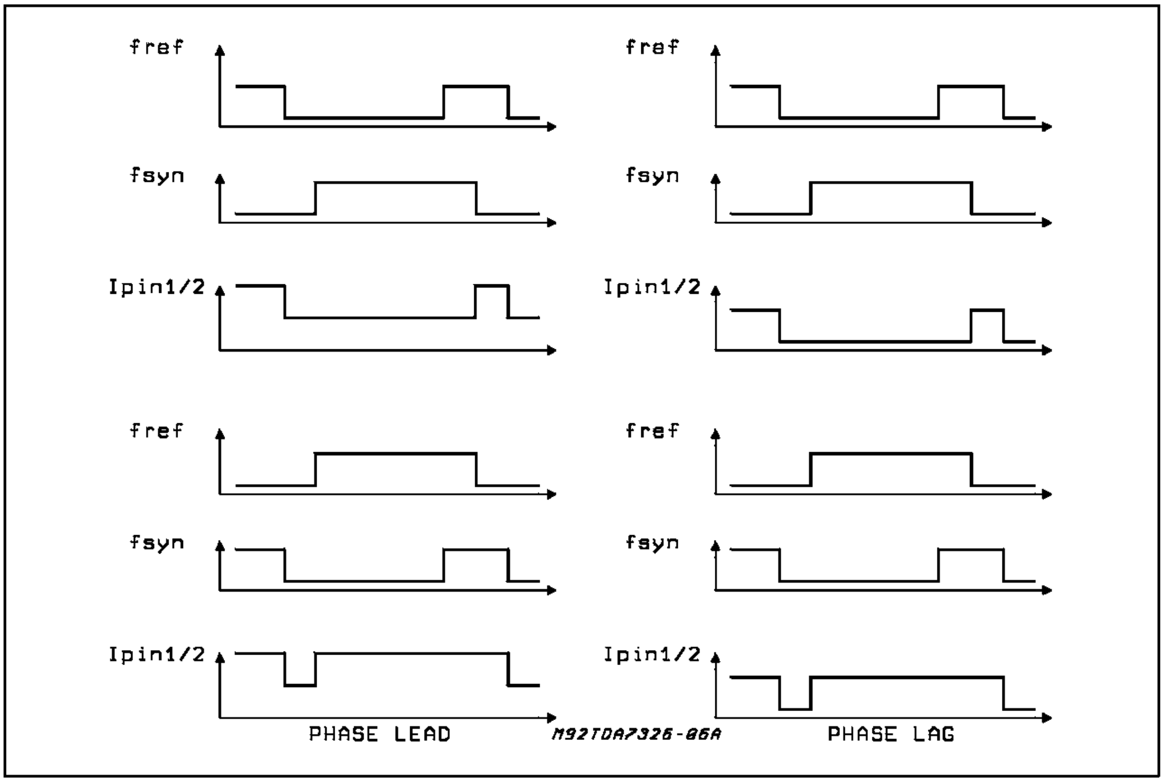
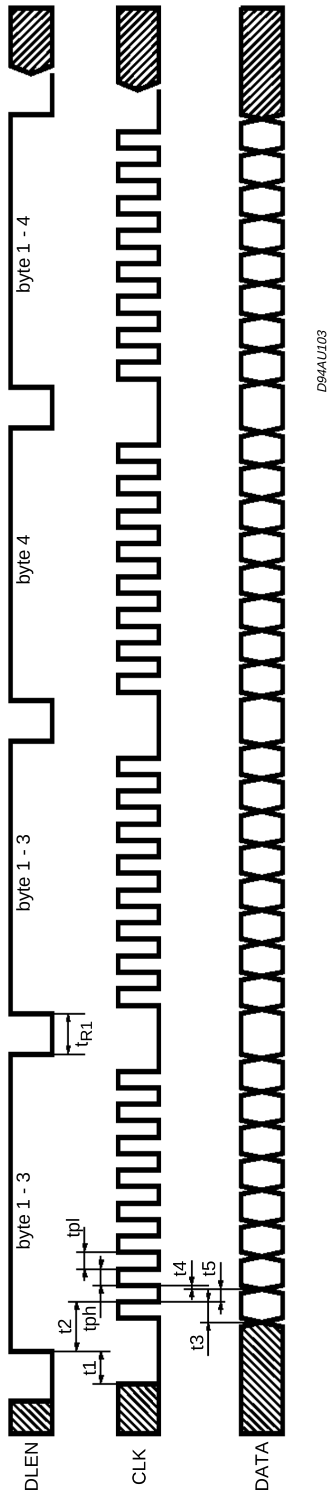


Figure 5



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3.5 THREE STATE PHASE COMPARATOR

The phase comparator generates a phase error signal according to phase difference between f_{SYN} and f_{REF}. This phase error signal drives the charge pump current generator

3.6 CHARGE PUMP CURRENT GENERATOR

This system generates signed pulses of current. Duration and polarity of those pulses are determined by the phase error signal. The absolute current values are programmable by 'CURR1' and 'CURR2' bits and controlled by an external resistor R_{ISET} connected to Pin 2 and GND.

3.7 LOW NOISE CMOS OP-AMP

A low noise Op-Amp is available on chip. The positive input of this Op-Amp is connected to an internal voltage divider and to Pin 3 'V_{REF}'. The negative input is connected to the charge pump output. In cooperation with this internal amplifier and external components, an active filter can be provided. To increase the flexibility in application the negative input can be switched to two input pins (Pins 15 and 16). This switch is controlled by 'LPF' register with 'LPF' low Pin 15 is active and 'LPF' high Pin 16 is active. This feature allows two separate active filters with different performance.

3.8 TEST FUNCTION

The test pin (Test Out) is used only for testing: it has no use in real applications. The three bits test0, test1, test2, of the test REGISTER must be programmed as 0,0,0 in application.
Some device internal signals can be checked at pin 9 (TST OUT) and pin 7 (OSC IN) by programming different codes of the test register according to the Table 1.

For example by programming the code 110 the "fsyn out" will be available at pin 9 and "f_{REF} input" at pin 7.

TABLE 1:

Test Register Status			Test Function	
test 0	test 1	test 2	PIN9 (TEST/OUT)	PIN 7 (OSCIN)
0	0	0	S_{out} (appl. mode)	O_{scin} (appl. mode)
1	0	0	f_{ref} Output	O_{scin} (appl. mode)
0	1	0	P_{hi} Output	f_{ref} Input
1	1	0	f_{syn} Output	fref Input
0	0	1	P_{hi} input	O_{scin} (appl. mode)

3.9 C-BUS INTERFACE

This interface allows communication between the PLL device and µp systems. A bus control system check the format of transmission, only eight bit word transmission is allowed. Four registers with 6 bit are user programmable. The selection of this four registers is controlled by two address bits.

4.0 BIT ORGANIZATION OF THE BUS TRANSFER OPERATION

Loading registers for all bytes of the programmable counters and all control registers

0	1	PC7	PC6	LPF1/ LPF2	CURR1	SWM DIR	AM FM	1	0	PC5	PC4	PC3	PC2	PC1	PCO	⇒

®	1	1	SC5 (0)*	SC4	SC3	SC2	SC1	SC0	0	0	0	0	0	S_{OUT}	CURR2	f_{ref}

Loading registers for all bytes of the programmable counters and all control registers

0	1	PC7	PC6	LPF2/ LPF1	CURR1	SWM DIR	AM FM	1	0	PC5	PC4	PC3	PC2	PC1	PCO	⇒

®	1	1	SC5 (0)*	SC4	SC3	SC2	SC1	SC0

Loading registers for 11 or 12 bits of the programmable counters

1	0	PC5	PC4	PC3	PC2	PC1	PC0	1	1	SC5 (0)*	SC4	SC3	SC2	SC1	SC0

Loading registers for 5 or 6 bits of the programmable counters

1	1	SC5 (0)*	SC4	SC3	SC2	SC1	SC0

Setting control register for loop filter selection charge pump current bit 1, mode AM/FM selection

0	1	X	X	LPF2/ LPF1	CURR1	SWM/ DIR	AM FM

Test mode inizialization (Test0 = Test1 = Test2 = 0)

0	0	TST0	TST1	TST2	S_{OUT}	CURR2	f_{REF}

Setting control register for switch output pin 9, charge pump current bit 2, reference frequency select

0	0	0	0	0	S_{OUT}	CURR2	f_{REF}

(*) This bit has to be ”0” for f_{REF} = ”1” (f_{REF} = 25kHz in FM mode or 2.5KHz AM swallow mode)

5.0 FREQUENCY PROGRAMMATION

5.1 AM/FM Computation Resume

FM SWALLOW MODE

$f_{REF} = 12.5KHz$ $F_{VCO} = (64 \cdot PC + SC + 64) \cdot f_{REF}$

$$\boxed{F_{VCO} = (DIV\_VAL + 64) \cdot f_{REF}}$$ swallow 6bit

$f_{REF} = 25KHz$ $F_{VCO} = (32 \cdot PC + SC + 32) \cdot f_{REF}$

$$\boxed{F_{VCO} = (DIV\_VAL + 32) \cdot f_{REF}}$$ swallow 5bit (bit SC5 = 0)

where:
PC = Program Counter Value (PC7 to PC0)
SC = Swallow Counter Value (SC5 to SC0)
DIV_VAL = Divider Factor

AM SWALLOW MODE

$f_{REF} = 1KHz$ $F_{VCO} = (64 \cdot PC + SC + 64) \cdot f_{REF}$

$$F_{VCO} = (DIV\_VAL + 64) \cdot f_{REF}$$ swallow 6bit

$f_{REF} = 2.5KHz$ $F_{VCO} = (32 \cdot PC + SC + 32) \cdot f_{REF}$

$$F_{VCO} = (DIV\_VAL + 32) \cdot f_{REF}$$ swallow 5bit (bit SC5 = 0)

AM DIRECT MODE

$$F_{VCO} = (DIV\_VAL + 1) \cdot f_{REF}$$

5.2: Examples

a) CONDITIONS:

FM MODE (f_{RF} = 98.1MHz, f_{REF} = 25KHz; IF = 10.7MHz

it follows: that F_{VCO} = 98.1 + 10.7 = 108.8MHz

$DIV\_VAL = \frac{F_{VCO}}{f_{ref}} - 32 = 4352 - 32 = 4320 = 10\ E\ 0$ Hex

=

1	0	0	0	0	1	1	1	0	0	0	0	0	0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	SC5	SC4	SC3	SC2	SC1	SC0

binary ⇒ SC = 0 (*)
PC = 135

b) CONDITIONS:

FM MODE (f_{RF} = 98.8MHz, f_{REF} = 25KHz; IF = 10.7MHz

it follows: F_{VCO} = 98.8 + 10.7 = 109.5MHz

DIV_VAL = 4380 - 32 = 4348 = 10 FC Hex

=

1	0	0	0	0	1	1	1	0	1	1	1	0	0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	SC5	SC4	SC3	SC2	SC1	SC0

binary ⇒ SC = 28 (*)
PC = 135

NOTE: (*) The bit SC5 is FORCED = 0, and higher weigth bits are left shift ed one position.

c) CONDITIONS:

FM MODE (f_{RF} = 98.8MHz, f_{REF} = 12.5KHz; IF = 10.7MHz

it follows: F_{VCO} = 98.8 + 10.7 = 109.5MHz

DIV_VAL = 8760 - 64 = 8696 = 21 F8 Hex

=

1	0	0	0	0	1	1	1	1	1	1	0	0	0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	SC5	SC4	SC3	SC2	SC1	SC0

binary ⇒ SC = 56

PC = 135

d) CONDITIONS:

AM DIRECT MODE, (f_{RF} = 530KHz, f_{REF} = 1KHz; IF = 450KHz

it follows: F_{VCO} = 530 + 450 = 980KHz

$$DIV\_VAL = \frac{F_{VCO}}{f_{REF}} \pm 1 = \frac{980}{1} \pm 1 = 979 = 3D3\ Hex$$

=

0	0	0	0	1	1	1	1	0	1	0	0	1	1
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	SC5	SC4	SC3	SC2	SC1	SC0

binary

e) CONDITIONS:

AM DIRECT MODE, (f_{RF} = 1710KHz, f_{REF} = 1KHz; IF = 450KHz

it follows: F_{VCO} = 1710 + 450 = 2160KHz

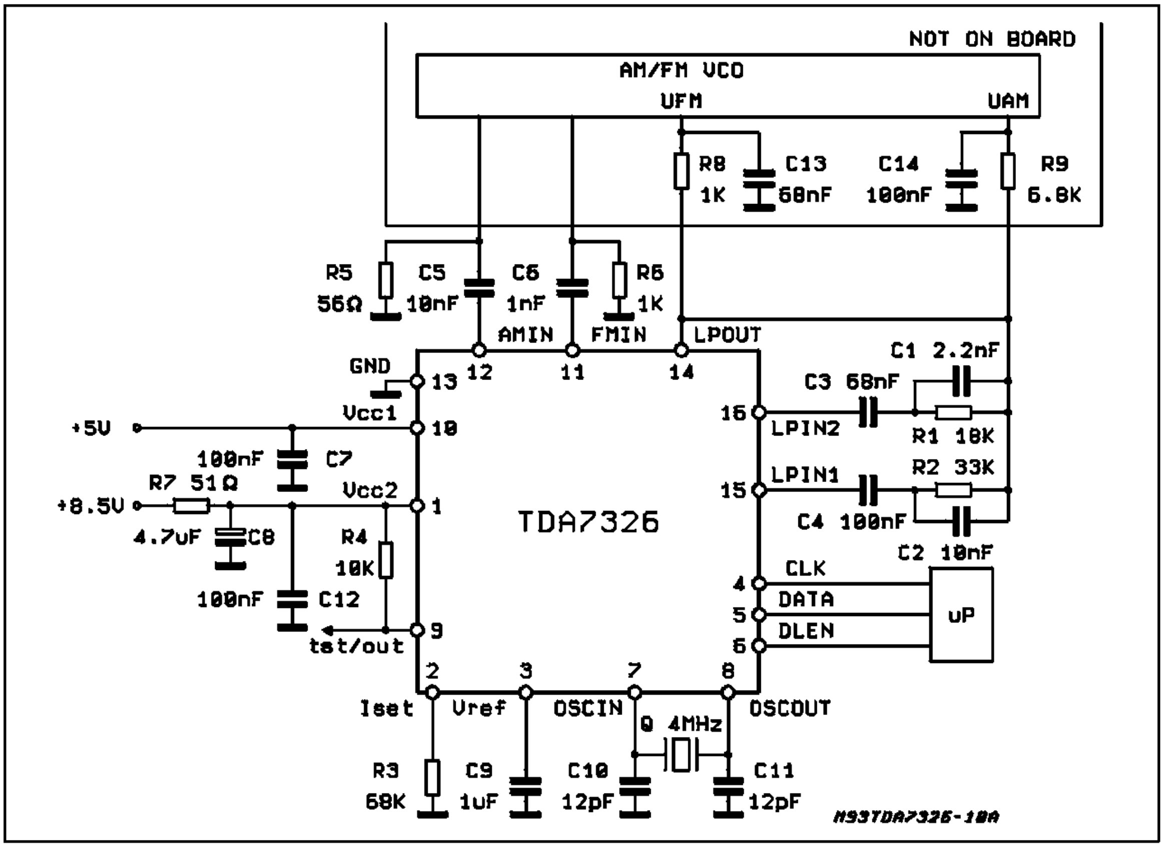
$$DIV\_VAL = \frac{F_{VCO}}{f_{REF}} \pm 1 = \frac{2160}{1} \pm 1 = 2159 = 86F\ Hex$$

=

0	0	1	0	0	0	0	1	1	0	1	1	1	1
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	SC5	SC4	SC3	SC2	SC1	SC0

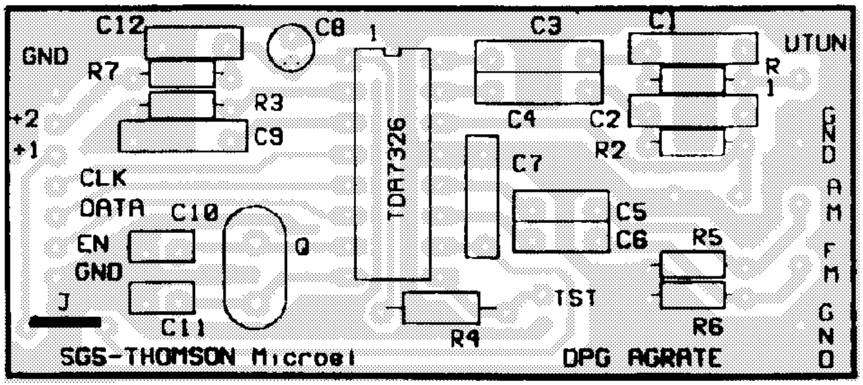
binary

Figure 5: Application with two loop-filters



*) C7 must be connected as closed as possible between pin 10 and pin 13

Figure 6: PC Board and Component Layout of fig. 5



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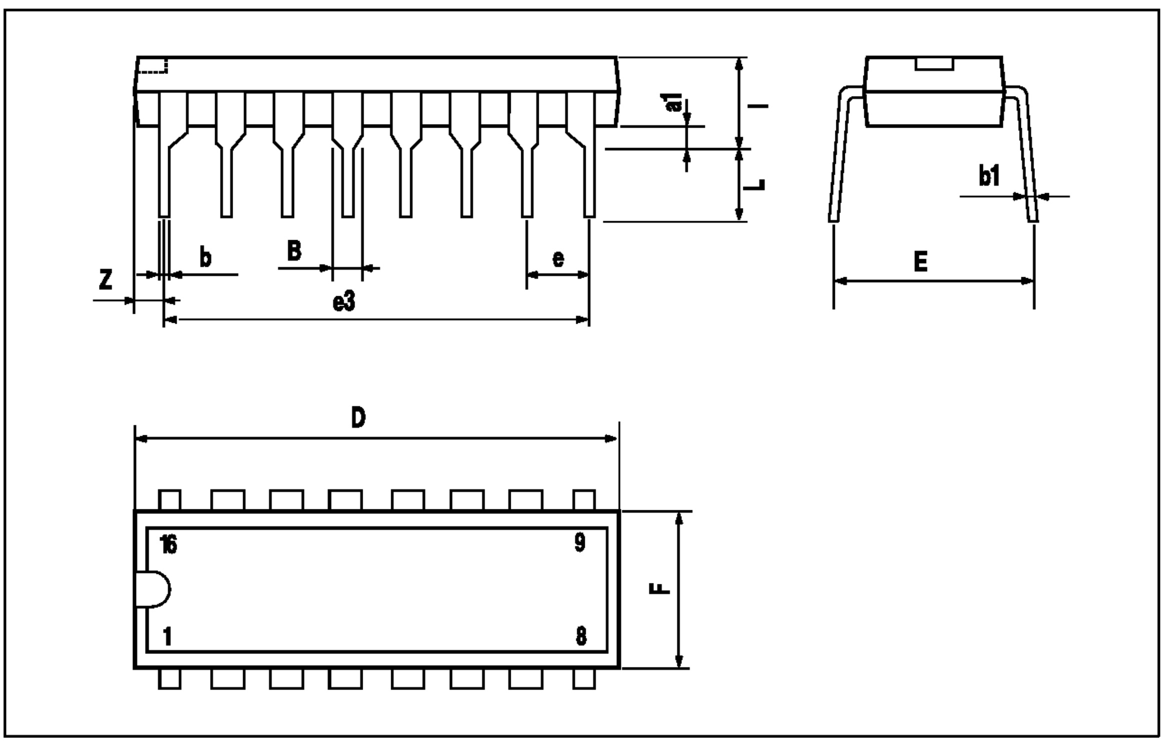
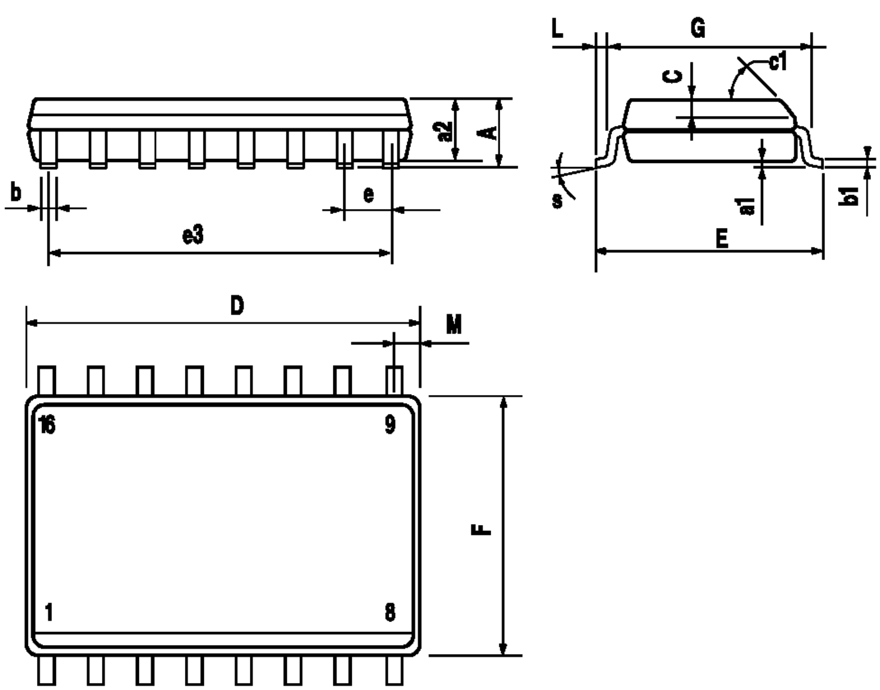
DIP16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.398		0.413
E	10.0		10.65	0.394		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					



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