

FOUR BANDS DIGITAL CONTROLLED GRAPHIC EQUALIZER

- VOLUME CONTROL IN 0.375dB STEP
- FOUR BANDS STEREO GRAPHIC EQUAL-IZER
- CENTER FREQUENCY, BANDWIDTH, MAX BOOST/CUT DEFINED BY EXTERNAL COM-PONENTS
- ±14dB CUT/BOOST CONTROL IN 2dB/STEP
- ALL FUNCTIONS PROGRAMMABLE VIA SE-RIALBUS
- VERY LOW DISTORTION
- VERY LOW NOISE AND DC STEPPING BY USE OF A MIXED BIPOLAR/CMOS TECH-NOLOGY

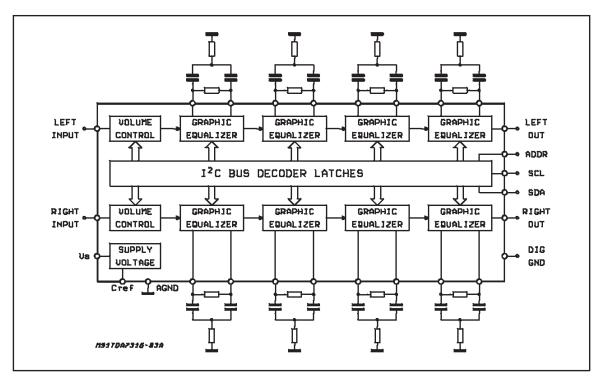


DESCRIPTION

The TDA7316 is a monolithic, digitally controlled graphic equalizer realized in BiCMOS mixed technology. The stereo signal, before any filtering, can be at-

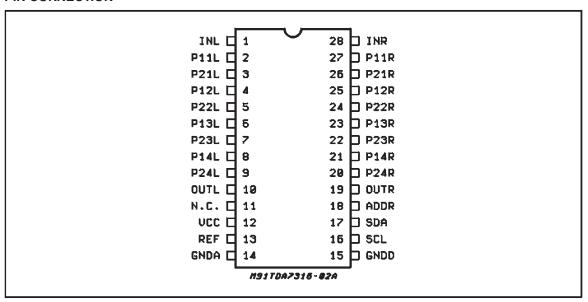
tenuated down to -17.625dB in 0.375dB step. All the functions can be programmed via serial bus making easy to build a μP controlled system. Signal path is designed for very low noise and distortion.

BLOCK DIAGRAM



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PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	Supply Voltage	10.2	V
T _{op}	Operating Temperature Range	-40 to +85	°C
T _{stg}	Storage Temperature Range	-55 to +150	°C
R _{tjvins}	Thermal Resistance Junction pins max	85	°C/W

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25$ °C, $V_S = 9V$, $R_L = 10 \text{K}\Omega$, $R_g = 600 \Omega$, $f = 1 \text{KHz V}_{IN} = 1 \text{Vrms}$, all controls in flat position (AV = 0dB) unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
SUPPLY						
Vs	Supply Voltage		6	9	10	V
Is	Supply Current		8	14	20	mA
SVR	Ripple Rejection		60	80		dB

ELECTRICAL CHARACTERISTICS (continued)

Nax Input Signal	Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
VIN miax Max Input Signal THD = 0.3% 2.0 2.5 VI INS Input Separation (1) 80 100 0 0 VOLUME CONTROL	INPUT						
INS	R _I	Input Resistance		20	30	40	ΚΩ
INS	V _{IN max}	Max Input Signal	THD = 0.3%	2.0	2.5		V_{RMS}
CRANGE Control Range 17.625 0 AVMIN Min. Attenuation -0.5 0 0.5 0 AVMAX Max. Attenuation 16.7 17.625 18.6 0 ASTEP Step Resolution 0.175 0.375 0.575 0 EA Attenuation Set Error -1.0 1 0 0 ET Tracking Error 0.5 0 3.0 n GRAPHIC EQUALIZER THD Distortion 0.01 0.1 0.1 Cs Channel Separation 80 100 0 0 eNO Output Noise BW = 20Hz to 20KHz 8 20 1 BW = 20Hz to 20KHz AV = 0dB 8 20 1 1 2 3 1 S/N Signal to Noise Ratio Ay = 0dB; Vref = 1VRMS 100 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0		Input Separation (1)		80	100		dB
Avmin Min. Attenuation -0.5 0 0 0.5 0 0.5 0 0 0.5 0 0 0.5 0 0 0.5 0 0 0.5 0 0 0.5 0 0 0.5 0 0 0.5 0 0 0.5 0 0 0 0 0 0 0 0 0	VOLUME C	ONTROL					
Name	C _{RANGE}	Control Range			17.625		dB
ASTEP Step Resolution	A _{VMIN}	Min. Attenuation		-0.5	0	0.5	dB
E_A	A _{VMAX}	Max. Attenuation		16.7	17.625	18.6	dB
ET	A _{STEP}	Step Resolution		0.175	0.375	0.575	dB
VDC DC Steps adjacent attenuation steps 0 3.0 n	E _A	Attenuation Set Error		-1.0		1	dB
THD	Ет	Tracking Error				0.5	dB
THD	V_{DC}	DC Steps	adjacent attenuation steps		0	3.0	mV
Cs Channel Separation 80 100 0 eNO Output Noise BW = 20Hz to 20KHz flat, AV = 0dB AL Low Pold BAL Low Po	GRAPHIC E	QUALIZER					
BW = 20Hz to 20KHz Representation	THD	Distortion			0.01	0.1	%
flat, AV = 0dB	Cs	Channel Separation		80	100		dB
BW = 20Hz to 20KHz AV = 0dB All bands = max. boost All bands = max. boost All bands = max. cut All bands	e _{NO}	Output Noise			8	20	μV
All bands = max. boost All bands = max. cut All bands = max. boost All bands = max. boost All cut All bands = max. boost All cut All cut			A curve		6		μV
B _{step} Step Resolution 1 2 3 0 C _{RANGE} Control Range max boost/cut ±12 ±14 ±16 0 VDC DC Steps Adiacent Control Steps 0.5 3 n AUDIO OUTPUTS V _O Output Voltage 2 2.5 V/ R _L Output Load Resistance 2 10 r C _L Output Load Capacitance 10 r R _O Output Resistance 5 10 20 V _{OUT} DC Voltage Level 4.2 4.5 4.8 BUS INPUTS V _{IL} Input Low Voltage 3 1 V _{IL} Input High Voltage 3 1			All bands = max. boost				μV μV
B _{Step} Step Resolution 1 2 3 0 C _{RANGE} Control Range max boost/cut ±12 ±14 ±16 0 VDC DC Steps Adiacent Control Steps 0.5 3 n AUDIO OUTPUTS Vo Output Voltage 2 2.5 V/ RL Output Load Resistance 2 F V/ I	S/N	Signal to Noise Ratio	$A_V = 0$ dB; $V_{ref} = 1V_{RMS}$		100		dB
CRANGE Control Range max boost/cut ±12 ±14 ±16 Creation VDC DC Steps Adiacent Control Steps 0.5 3 n AUDIO OUTPUTS Vo Output Voltage 2 2.5 Vr RL Output Load Resistance 2 2 2 CL Output Load Capacitance 10 r RO Output Resistance 5 10 20 VOUT DC Voltage Level 4.2 4.5 4.8 BUS INPUTS VIL Input Low Voltage 1 1 VIH Input High Voltage 3 1	B _{step}			1	2	3	dB
VDC DC Steps Adiacent Control Steps 0.5 3 n AUDIO OUTPUTS Vo Output Voltage 2 2.5 Voltage RL Output Load Resistance 2 Property Control Steps Property Control Steps Voltage Property Control Steps Property Control Steps Voltage Property Control Steps <		Control Range	max boost/cut	±12	±14	±16	dB
Vo Output Voltage 2 2.5 Voltage RL Output Load Resistance 2 Resistance 10 resistance 10 </td <td></td> <td>DC Steps</td> <td>Adiacent Control Steps</td> <td></td> <td>0.5</td> <td>3</td> <td>mV</td>		DC Steps	Adiacent Control Steps		0.5	3	mV
RL Output Load Resistance 2 R CL Output Load Capacitance 10 r RO Output Resistance 5 10 20 VOUT DC Voltage Level 4.2 4.5 4.8 BUS INPUTS VIL Input Low Voltage 1 1 VIH Input High Voltage 3 3	AUDIO OUT	PUTS					
CL Output Load Capacitance 10 r RO Output Resistance 5 10 20 VOUT DC Voltage Level 4.2 4.5 4.8 BUS INPUTS VIL Input Low Voltage 1 1 VIH Input High Voltage 3 3	Vo	Output Voltage		2	2.5		V _{RMS}
RO Output Resistance 5 10 20 VOUT DC Voltage Level 4.2 4.5 4.8 BUS INPUTS VIL Input Low Voltage 1 1 VIH Input High Voltage 3 3	RL	Output Load Resistance		2			ΚΩ
VOUT DC Voltage Level 4.2 4.5 4.8 BUS INPUTS VIL Input Low Voltage 1 VIH Input High Voltage 3	CL	Output Load Capacitance				10	nF
BUS INPUTS V _{IL} Input Low Voltage 1 V _{IH} Input High Voltage 3	Ro	Output Resistance		5	10	20	Ω
V _{IL} Input Low Voltage 1 V _{IH} Input High Voltage 3	V _{OUT}	DC Voltage Level		4.2	4.5	4.8	V
V _{IH} Input High Voltage 3	BUS INPUT	S					
V _{IH} Input High Voltage 3	V _{IL}	Input Low Voltage				1	V
las Input Current _5 _5		Input High Voltage		3			V
Input outlient	I _{IN}	Input Current		-5		+5	μА
V _O Output Voltage SDA I _O = 1.6mA 0.4	Vo		I _O = 1.6mA			0.4	V
ADDRESS PIN (Internal 50KΩ pull down resistor)	ADDRESS I	PIN (Internal 50KΩ pull down	resistor)				
V _{IL} Input Low Voltage	V _{IL}	Input Low Voltage				1	V
V _{IH} Input High Voltage V _{CC} -1V	V_{IH}	Input High Voltage		V _{CC} -1V			V

NOTE1: The selected input is grounded thre the 2.2 μF capacitor



DEVICE DESCRIPTION

The TDA7316 is a four bands, digitally controlled stereo Graphic Equalizer.

The device is intended for high quality audio application in Hi-Fi, TV and car radio systems where feature like low noise and THD are key factors. A mixed Bipolar Cmos Technology allows:

Cmos analog switches for pop free commutations, high frequency op.amp. (GWB = 10MHz) and high linearity polisilicon resistor for THD = 0.01 (at Vin = 1Vrms) and a S/N ratio of 102dB. The internal Block Diagram is shown on page 1.

The first stage is a volume control. The control range is 0 to -17.625dB with 0.375dBstep.

The very high resolution (0.375dB step) allows the implementation of closed loop amplitude control system completely free from any acustical effect (stepping variation and pumping effect).

The volume control is followed by a serial four bands equalizer. Each filtering cell is the biquad cell shown in fig. 1

The internal resistor string is fixing the boost/cut value while the buffer makes the Q (quality factor) and central frequency, set by external components, fully indipendent from the internal resistors. Each filtering cell is realized using only 4 external components (2 capacitors and 2 resistors) allowing a flexible selection of centre frequency fo, Q factor and gain. Here below the basic formulae and the key features of each band pass filter are reported:

 f_0 = center frequency Gv = gain/loss at the center frequency f_0 Gv = 20log(Av)

$$Q = \frac{f_0}{f_2 - f_1}$$

where f_2 , $f_1 = 3dB$ Bandwidth limits.

$$\begin{split} A_V &= \frac{(R2 \cdot C2) + (R2 \cdot C1) + (R1 \cdot C1)}{(R2 \cdot C1) + (R2 \cdot C2)} \\ Q &= \frac{\sqrt{(R1 \cdot C1 \cdot R2 \cdot C2)}}{(R2 \cdot C1) + (R2 \cdot C2)} \\ f_0 &= \frac{1}{2\pi \cdot \sqrt{(R1 \cdot R2 \cdot C1 \cdot C2)}} \end{split}$$

If C1 is fixed, then:

$$C2 = \frac{Q^{2}}{A_{v} - 1 - Q^{2}} \cdot C1$$

$$R2 = \frac{1}{2 \pi \cdot C1 \cdot f_{o} \cdot \frac{(A_{v} - 1) \cdot Q}{(A_{v} - 1 - Q^{2})}}$$

$$R1 = \frac{(A_{v} - 1)^{2}}{A_{v} - 1 - Q^{2}} \cdot R2$$

Likewise, the components values can be determined by fixing one of the other three parameters. Referring to fig. 1 the suggested R2 value should be higher than $2K\Omega$ in order to have a good THD (internal op. amp. current limit). Viceversa the R1 value should be equal or lower

Viceversa the R1 value should be equal or lower than 51K Ω in order to keep the "click"(DC step) very low.

A typical application is shown by fig. 2

Fig. 1

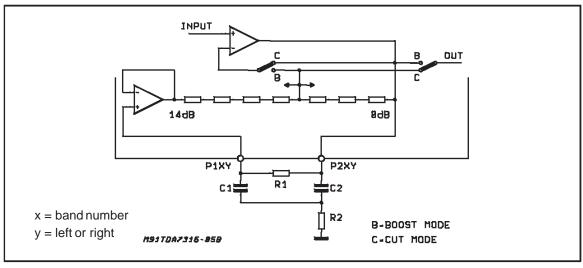
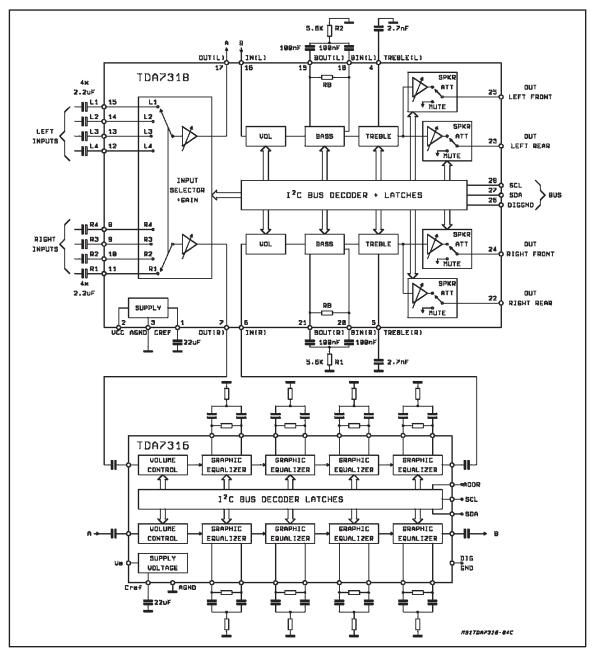


Figure 2: Application Circuit



A five bands graphic equalizer is implemented using the 4 bands of the TDA7316 plus a fifth band obtained from the bass control circuit of the TDA7318 (or another audioprocessor of the SGS-THOMSON 731X family). Applications requiring higher number of external equalizer bands could be implemented by cascading 2 or more TDA7316 devices. In fact the dedicated ADDR pin allows 2 addresses selection. Anyway, the ad-

dress of the graphic equalizer is different from the audioprocessorone.

For example, 9 bands are implemented by using of 2 TDA7316 plus an audioprocessor (TDA731X family).

In case one filtering cell is not needed, a short circuit must be provided between the P1xy and P2xy pins.

I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7316 and viceversa takes place thru the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

Data Validity

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Figure 3: Data Validity on the I²CBUS

Acknowledge

The master (μ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the μP can use a simplier transmission: simply it generates the 9th clock pulse without checking the slave acknowledging, and then sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

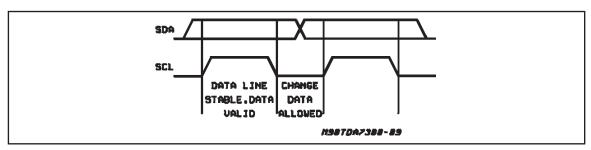


Figure 4: Timing Diagram of I²CBUS

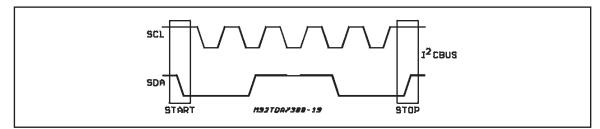
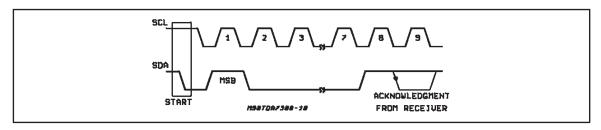


Figure 5: Acknowledge on the I²CBUS



SOFTWARE SPECIFICATION

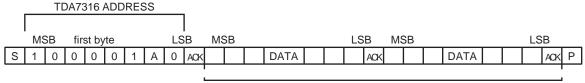
Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7316

address (the 8th bit of the byte must be 0). The TDA7316 must always acknowledge at the end of each transmitted byte.

- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



Data Transferred (N-bytes + Acknowledge)

ACK = Acknowledge

S = Start

P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address (84 or 86 Hex)

1	0	0	0	0	1	Α	0
MSB							LSB

A = Logic level on pin ADDR

A = 1 if ADDR pin = open

A = 0 if ADDR pin = connected to ground

SOFTWARE SPECIFICATION (continued)

DATA BYTES (detailed description)

Volume

MSB							LSB	FUNCTION
0	Χ	B2	B1	В0	A2	A1	A0	Volume 0.375dB steps
					0	0	0	0
					0	0	1	-0.375
					0	1	0	-0.75
					0	1	1	-1.125
					1	0	0	-1.5
					1	0	1	-1.875
					1	1	0	-2.25
					1	1	1	-2.625
0	Χ	B2	B1	В0	A2	A1	A0	Volume -3dB steps
		0	0	0				0
		0	0	1				-3
		0	1	0				-6
		0	1	1				-9
		1	0	0				-12
		1	0	1				-15



TDA7316

Graphic Equalizer

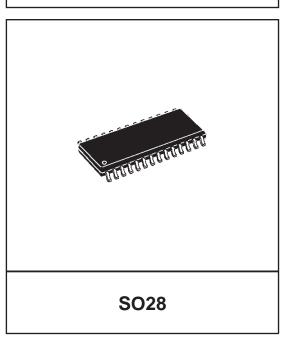
MSB							LSB	FUNCTION
1	D3	D2	D1	D0	S2	C1	C0	
	0 0 0 1	0 1 1 0	1 0 1 0					Band 1 Band 2 Band 3 Band 4
	D3 D3	D2 D2	D1 D1	1 0	C2 C2	C1 C1	C0 C0	cut Boost
					0 0 0 0 1 1 1	0 0 1 1 0 0	0 1 0 1 0 1 0	0dB 2dB 4dB 6dB 8dB 10dB 12dB 14dB

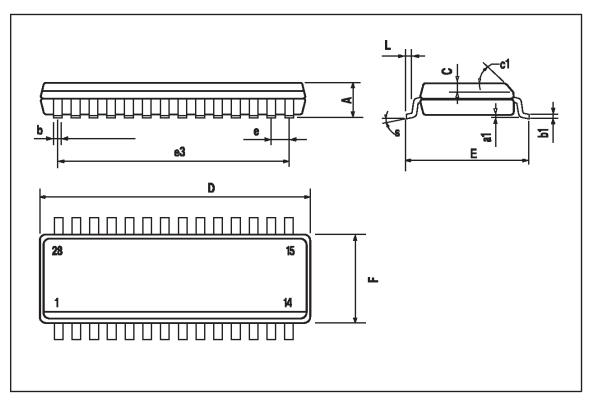
AX = 0.375dB steps, BX = 3dB steps, CX = 2dB steps, X = dont'care

STATUS AFTER POWER-ON RESET							
Volume	-17.25dB						
Graphic equalizer bands	-12dB						

DIM.		mm	_	inch				
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
А			2.65			0.104		
a1	0.1		0.3	0.004		0.012		
b	0.35		0.49	0.014		0.019		
b1	0.23		0.32	0.009		0.013		
С		0.5			0.020			
c1			45° ((typ.)				
D	17.7		18.1	0.697		0.713		
Е	10		10.65	0.394		0.419		
е		1.27			0.050			
е3		16.51			0.65			
F	7.4		7.6	0.291		0.299		
L	0.4		1.27	0.016		0.050		
S	8 ° (max.)							

OUTLINE AND MECHANICAL DATA





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