# MCP3909

## Energy Metering IC with SPI Interface and Active Power Pulse Output

### Features

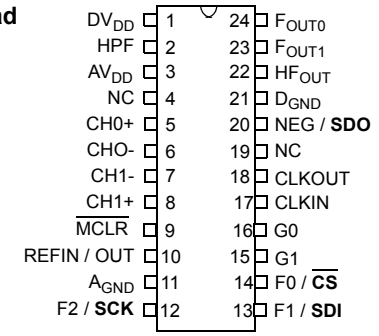
- Supports IEC 62053 International Energy Metering Specification and legacy IEC 1036/ 61036/687 Specifications
- Digital waveform data access through SPI interface
  - 16-bit Dual ADC output data words
  - 20-bit Multiplier output data word
- Dual functionality pins support serial interface access and simultaneous Active Power Pulse Output
- Two 16-bit second order delta-sigma Analog-to-Digital Converters (ADCs) with multi-bit DAC
  - 81 dB SINAD (typ.) both channels
- 0.1% typical active energy measurement error over **1000:1** dynamic range
- PGA for small signal inputs supports low value shunt current sensor
- Ultra-low drift on-chip reference: 15 ppm/°C (typ.)
- Direct drive for electromagnetic mechanical counter and two-phase stepper motors
- Low $I_{DD}$ of 4 mA (max.)
- Tamper output pin for negative power indication
- Industrial Temperature Range: -40°C to +85°C

### Description

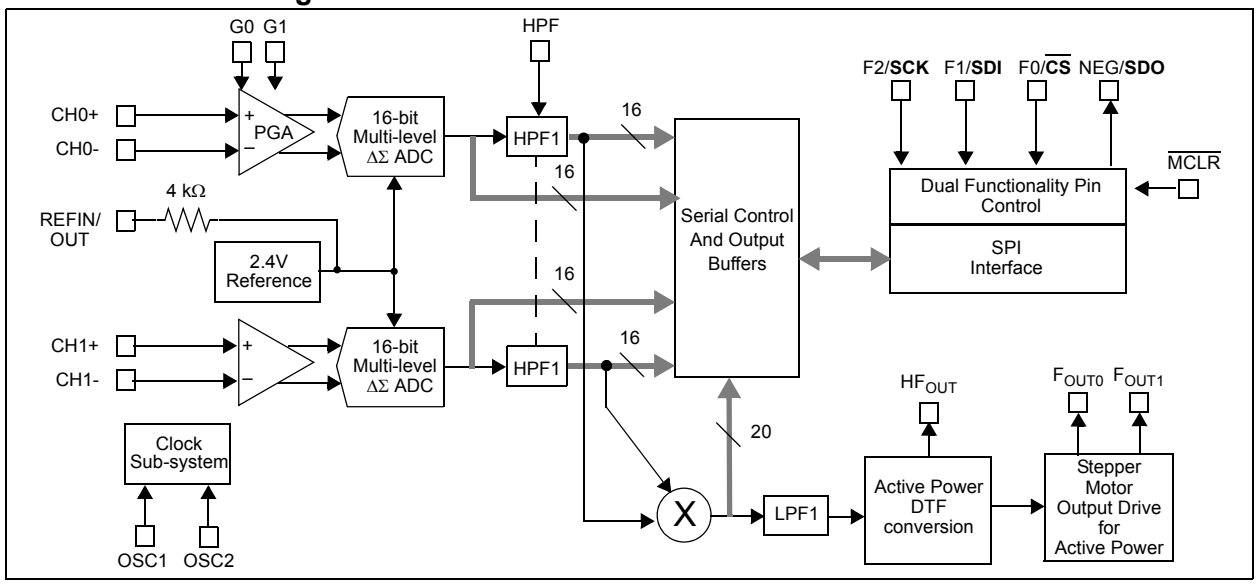
The MCP3909 device is an energy-metering IC designed to support the IEC 62053 international metering standard specification. It supplies a frequency output proportional to the average active real power, with simultaneous serial access to ADC channels and multiplier output data. This output waveform data is available at up to 14 kHz with 16-bit ADC output and 20-bit multiplier output words. The 16-bit, delta-sigma ADCs allow for a wide range of $I_B$ and $I_{MAX}$ currents and/or small shunt (<200 µOhms) meter designs. A no-load threshold block prevents any current creep measurements for the active power pulse outputs. The integrated on-chip voltage reference has an ultra-low temperature drift of 15 ppm per degree C.This accurate energy metering IC with high field reliability is available in the industry standard 24-lead SSOP pinout.

### Package Type

**24-Lead SSOP**




### Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

$V_{DD}$ .....7.0V
Digital inputs and outputs w.r.t. $A_{GND}$ ..... -0.6V to $V_{DD}$ +0.6V
Analog input w.r.t. $A_{GND}$ .....-6V to +6V
$V_{REF}$ input w.r.t. $A_{GND}$ ..... -0.6V to $V_{DD}$ +0.6V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) .....4.0 kV, 400V
ESD on all other pins (HBM,MM) .....4.0 kV, 400V

**† Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at $AV_{DD} = DV_{DD}$ = 4.5V to 5.5V, Internal $V_{REF}$, HPF turned on (AC mode), $A_{GND}$, $D_{GND}$ = 0V, MCLK = 3.58 MHz; $T_A$ = -40°C to +85°C.

| Parameter | Sym | Min | Typ. | Max | Units | Comment |
|---|---|---|---|---|---|---|
| **Active Power Measurement Accuracy** | | | | | | |
| Active Energy Measurement Error | E | — | 0.1 | — | % $F_{OUT}$ | Channel 0 swings 1000:1 range, $F_{OUT0}$, $F_{OUT1}$ Frequency outputs only, does not apply to serial interface data. (**Note 1, Note 4)** |
| No-Load Threshold/ Minimum Load | NLT | — | 0.0015 | — | % $F_{OUT}$ Max | Frequency outputs only, does not apply to serial interface data. Disabled when F2, F1, F0 = 0, 1, 1 **(Note 5, Note 6)** |
| System Gain Error | | — | 1 | 5 | % $F_{OUT}$ | **(Note 2, Note 5)** |
| AC Power Supply Rejection (output frequency variation) | AC PSRR | — | 0.01 | — | % $F_{OUT}$ | F2, F1, F0 = 0, 1, 1 **(Note 3)** |
| DC Power Supply Rejection (output frequency variation) | DC PSRR | — | 0.01 | — | % $F_{OUT}$ | HPF = 1, Gain = 1 **(Note 3)** |
| **Waveform Sampling** | | | | | | |
| A/D Converter Signal-to-Noise and Distortion Ratio | SINAD | — | 81 | — | dB | Applies to both channels, $V_{IN}$ = 0 dBFS at 50 Hz ($V_{IN}$ = Full Scale) |
| Bandwidth (Notch Frequency) | | — | 14 | — | kHz | Applies to both channels, MCLK/256 |
| Phase Delay Between Channels | | — | — | 1/MCLK | s | HPF = 0 and 1, < 1 MCLK period **(Note 4, Note 6, Note 7)** |

**Note 1:** Measurement error = (Energy Measured By Device - True Energy)/True Energy * 100%. Accuracy is measured with signal (±660 mV) on Channel 1. $F_{OUT0}$, $F_{OUT1}$ pulse outputs. Valid from 45 Hz to 75 Hz. See typical performance curves for higher frequencies and increased dynamic range.

**2:** Does not include internal $V_{REF}$. Gain = 1, CH0 = 470 mVDC, CH1 = 660 mVDC, difference between measured output frequency and expected transfer function.

**3:** Percent of $HF_{OUT}$ output frequency variation; Includes external $V_{REF}$ = 2.5V, CH1 = 100 $mV_{RMS}$ @ 50 Hz, CH2 = 100 $mV_{RMS}$ @ 50 Hz, $AV_{DD}$ = 5V + 1$V_{pp}$ @ 100 Hz. DC PSRR: 5V ±500 mV

**4:** Error applies down to 60 degree lead (PF = 0.5 capacitive) and 60 degree lag (PF = 0.5 inductive).

**5:** Refer to **Section 4.0 "Device Overview"** for complete description.

**6:** Specified by characterization, not production tested.

**7:** 1 MCLK period at 3.58 MHz is equivalent to less than <0.005 degrees at 50 or 60 Hz.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at $AV_{DD}$ = $DV_{DD}$ = 4.5V to 5.5V, Internal $V_{REF}$, HPF turned on (AC mode), $A_{GND}$, $D_{GND}$ = 0V, MCLK = 3.58 MHz; $T_A$ = -40°C to +85°C.

| Parameter | Sym | Min | Typ. | Max | Units | Comment |
|---|---|---|---|---|---|---|
| **ADC/PGA Specifications** | | | | | | |
| Offset Error | $V_{OS}$ | — | 2 | 5 | mV | Referred to Input, applies to both channels |
| Gain Error Match | | — | 0.5 | — | % $F_{OUT}$ | **(Note 5)** |
| **Internal Voltage Reference** | | | | | | |
| Voltage | | — | 2.4 | — | V | |
| Tolerance | | — | ±2 | — | % | |
| Tempco | | — | 15 | — | ppm/°C | |
| **Reference Input** | | | | | | |
| Input Range | | 2.2 | — | 2.6 | V | |
| Input Impedance | | 3.2 | — | — | kΩ | |
| Input Capacitance | | — | — | 10 | pF | |
| **Analog Inputs** | | | | | | |
| Maximum Signal Level | | — | — | ±1 | V | CH0+,CH0-,CH1+,CH1- to $A_{GND}$ |
| Differential Input Voltage Range Channel 0 | | — | — | ±470/G | mV | G = PGA Gain on Channel 0 |
| Differential Input Voltage Range Channel 1 | | — | — | ±660 | mV | |
| Input Impedance | | 390 | — | — | kΩ | Proportional to 1/MCLK |
| **Oscillator Input** | | | | | | |
| Frequency Range | MCLK | 1 | — | 4 | MHz | |
| **Power Specifications** | | | | | | |
| Operating Voltage | | 4.5 | — | 5.5 | V | $AV_{DD}$, $DV_{DD}$ |
| $I_{DD,A}$ | $I_{DD,A}$ | — | 2.3 | 2.8 | mA | $AV_{DD}$ pin only |
| $I_{DD,D}$ | $I_{DD,D}$ | — | 0.8 | 1.2 | mA | $DV_{DD}$ pin only |

**Note 1:** Measurement error = (Energy Measured By Device - True Energy)/True Energy * 100%. Accuracy is measured with signal (±660 mV) on Channel 1. $F_{OUT0}$, $F_{OUT1}$ pulse outputs. Valid from 45 Hz to 75 Hz. See typical performance curves for higher frequencies and increased dynamic range.

**2:** Does not include internal $V_{REF}$. Gain = 1, CH0 = 470 mVDC, CH1 = 660 mVDC, difference between measured output frequency and expected transfer function.

**3:** Percent of $HF_{OUT}$ output frequency variation; Includes external $V_{REF}$ = 2.5V, CH1 = 100 $mV_{RMS}$ @ 50 Hz, CH2 = 100 $mV_{RMS}$ @ 50 Hz, $AV_{DD}$ = 5V + 1$V_{pp}$ @ 100 Hz. DC PSRR: 5V ±500 mV

**4:** Error applies down to 60 degree lead (PF = 0.5 capacitive) and 60 degree lag (PF = 0.5 inductive).

**5:** Refer to **Section 4.0 "Device Overview"** for complete description.

**6:** Specified by characterization, not production tested.

**7:** 1 MCLK period at 3.58 MHz is equivalent to less than <0.005 degrees at 50 or 60 Hz.

## TEMPERATURE CHARACTERISTICS

| **Electrical Specifications:** Unless otherwise indicated, $V_{DD}$ = 4.5V to 5.5V, $A_{GND}$, $D_{GND}$ = 0V. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +85 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | **Note** |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |

**Note:** The MCP3909 operates over this extended temperature range, but with reduced performance. In any case, the Junction Temperature ($T_J$) must not exceed the Absolute Maximum specification of +150°C.

## TIMING CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at $AV_{DD}$ = $DV_{DD}$ = 4.5V to 5.5V, $A_{GND}$, $D_{GND}$ = 0V, MCLK = 3.58 MHz; $T_A$ = -40°C to +85°C.

| Parameter | Sym | Min | Typ | Max | Units | Comment |
|---|---|---|---|---|---|---|
| **Frequency Outputs** | | | | | | |
| $F_{OUT0}$ and $F_{OUT1}$ Pulse Width (Logic Low) | $t_{FW}$ | — | 275 | — | ms | 984376 MCLK periods **(Note 1)** |
| $HF_{OUT}$ Pulse Width | $t_{HW}$ | — | 90 | — | ms | 322160 MCLK periods **(Note 2)** |
| $F_{OUT0}$ and $F_{OUT1}$ Pulse Period | $t_{FP}$ | Refer to Equation 4-1 | | | s | |
| $HF_{OUT}$ Pulse Period | $t_{HP}$ | Refer to Equation 4-2 | | | s | |
| $F_{OUT0}$ to $F_{OUT1}$ Falling-Edge Time | $t_{FS2}$ | — | 0.5 $t_{FP}$ | — | | |
| $F_{OUT0}$ to $F_{OUT1}$ Minimum Separation | $t_{FS}$ | — | 4/MCLK | — | | |
| **Digital I/O** | | | | | | |
| $F_{OUT0}$ and $F_{OUT1}$ Output High Voltage | $V_{OH}$ | 4.5 | — | — | V | $I_{OH}$ = 12 mA, $DV_{DD}$ = 5.0V |
| $F_{OUT0}$ and $F_{OUT1}$ Output Low Voltage | $V_{OL}$ | — | — | 0.5 | V | $I_{OL}$ = 12 mA, $DV_{DD}$ = 5.0V |
| $HF_{OUT}$ and NEG Output High Voltage | $V_{OH}$ | 4.5 | — | — | V | $I_{OH}$ = 12 mA, $DV_{DD}$ = 5.0V |
| $HF_{OUT}$ and NEG Output Low Voltage | $V_{OL}$ | — | — | 0.5 | V | $I_{OL}$ = 12 mA, $DV_{DD}$ = 5.0V |
| High-Level Input Voltage (All Digital Input Pins) | $V_{IH}$ | 2.4 | — | — | V | $DV_{DD}$ = 5.0V |
| Low Level Input Voltage (All Digital Input Pins) | $V_{IL}$ | — | — | 0.85 | V | $DV_{DD}$ = 5.0V |
| Input Leakage Current | | — | 0.1 | ±1 | µA | $V_{IN}$ = 0, $V_{IN}$ = $DV_{DD}$ |
| Pin Capacitance | | — | — | 10 | pF | **(Note 3)** |
| **Serial Interface Timings (Note 4)** | | | | | | |
| Output Data Rate | $f_{ADC}$ | — | MCLK/256 | — | | |
| Serial Clock Frequency | $f_{CLK}$ | | — | 20 | MHz | $V_{DD}$ = 5V |
| Window for serial mode entry codes | $t_{WINDOW}$ | — | — | 8/MCLK | — | Last bit must be clocked in before this time. |
| Window start time for serial mode entry codes | $t_{WINSET}$ | 1/MCLK | — | — | — | First bit must be clocked in after this time. |
| Serial Clock High Time | $t_{HI}$ | 10 | — | 40 | ns | |
| Serial Clock Low Time | $t_{LO}$ | 30 | — | 20 | ns | |
| $\overline{CS}$ Fall to First Rising CLK Edge | $t_{SUCS}$ | 15 | — | — | ns | |
| Data Input Setup Time | $t_{SU}$ | 10 | — | — | ns | |
| Data Input Hold Time | $t_{HD}$ | — | — | 10 | ns | |
| $\overline{CS}$ Rise to Output Disable | $t_{DIS}$ | — | — | 150 | ns | |
| CLK Fall to Output Data Valid | $t_{DO}$ | — | — | 30 | ns | |

**Note 1:** If output pulse period ($t_{FP}$) falls below 984376*2 MCLK periods, then $t_{FW}$ = 1/2 $t_{FP}$.

**2:** If output pulse period ($t_{HP}$) falls below 322160*2 MCLK periods, then $t_{HW}$ = 1/2 $t_{HP}$. When F2, F1, F0 equals 0,1,1, the $HF_{OUT}$ pulse time is fixed at 64 x MCLK periods or 18 µs for MCLK = 3.58 MHz

**3:** Specified by characterization, not production tested.

**4:** Serial timings specified and production tested with 180 pF load.

## TIMING CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at $AV_{DD}$ = $DV_{DD}$ = 4.5V to 5.5V, $A_{GND}$, $D_{GND}$ = 0V, MCLK = 3.58 MHz; $T_A$ = -40°C to +85°C.

| Parameter | Sym | Min | Typ | Max | Units | Comment |
|---|---|---|---|---|---|---|
| SDO Rise Time | $t_R$ | — | 2 | — | ns | |
| SDO Fall Time | $t_F$ | — | 2 | — | ns | |

**Note 1:** If output pulse period ($t_{FP}$) falls below 984376*2 MCLK periods, then $t_{FW}$ = 1/2 $t_{FP}$.

**2:** If output pulse period ($t_{HP}$) falls below 322160*2 MCLK periods, then $t_{HW}$ = 1/2 $t_{HP}$. When F2, F1, F0 equals 0,1,1, the $HF_{OUT}$ pulse time is fixed at 64 x MCLK periods or 18 µs for MCLK = 3.58 MHz

**3:** Specified by characterization, not production tested.

**4:** Serial timings specified and production tested with 180 pF load.

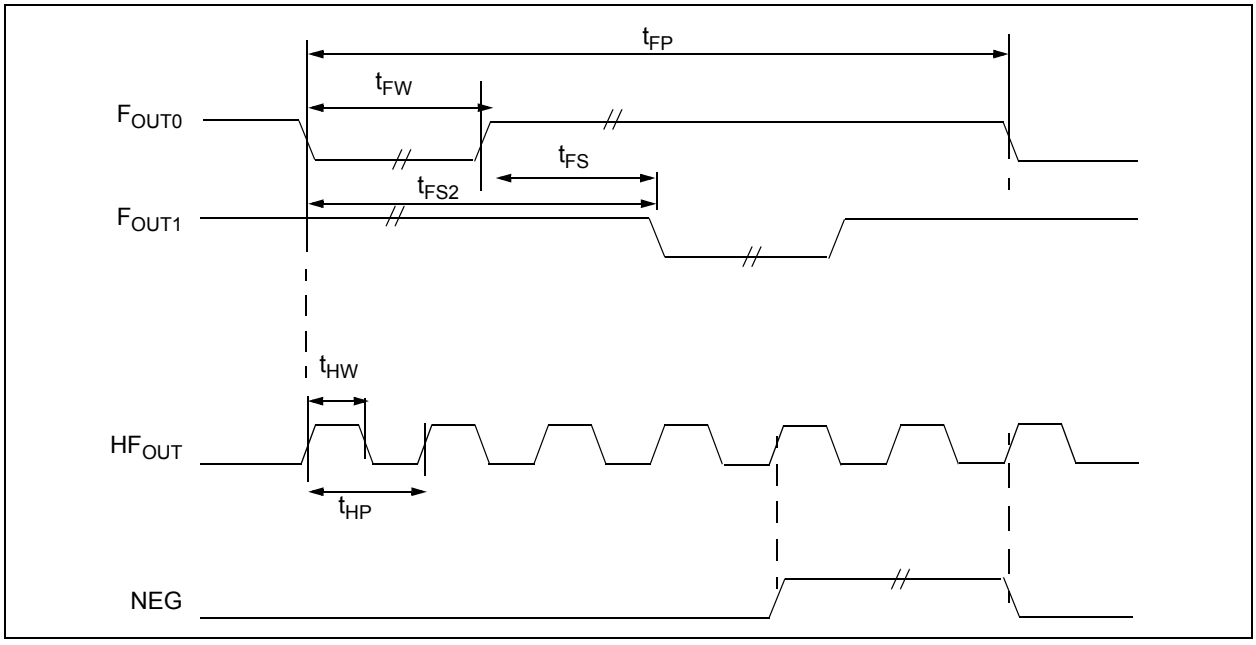



***FIGURE 1-1:*** *Output Timings for Active Power Pulse Outputs and Negative Power Pin.*

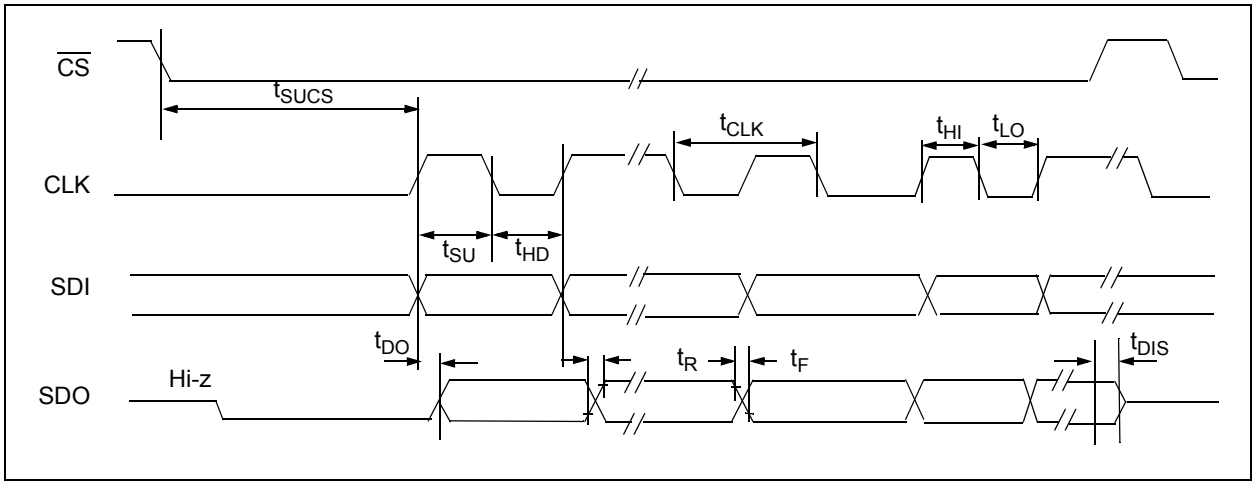



***FIGURE 1-2:*** *Serial Interface Timings showing Output, Rise, Hold, and $\overline{CS}$ Times.*

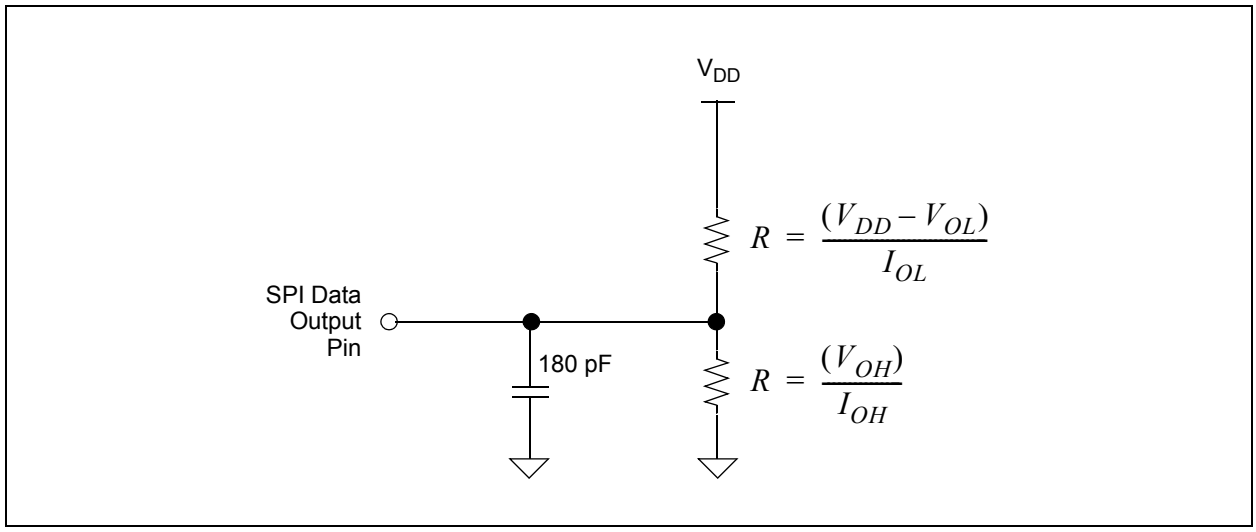



***FIGURE 1-3:*** *SPI Output Pin Loading Circuit During SPI Testing.*

## 2.0 TYPICAL PERFORMANCE CURVES

| | |
|---|---|
| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range. |

**Note:** Unless otherwise specified, $DV_{DD}$, $AV_{DD}$ = 5V; $A_{GND}$, $D_{GND}$ = 0V; $V_{REF}$ = Internal, HPF = 1 (AC mode), MCLK = 3.58 MHz, CH1 input = 660 $mV_{P-P}$ at 50 Hz, CH0 amplitude sweeps at 50 Hz.

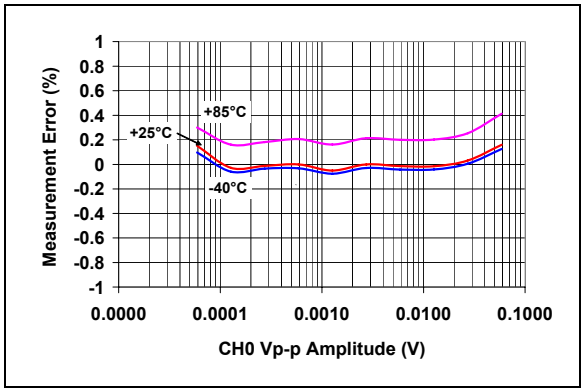



***FIGURE 2-1:*** *Active Power Measurement Error (Gain = 8 PF = 1).*

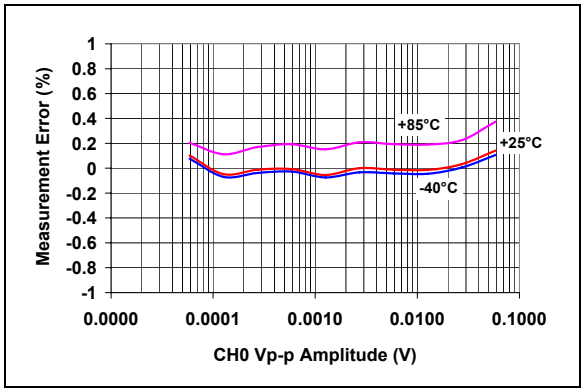



***FIGURE 2-4:*** *Active Power Measurement Error (Gain = 8, PF = 0.5).*

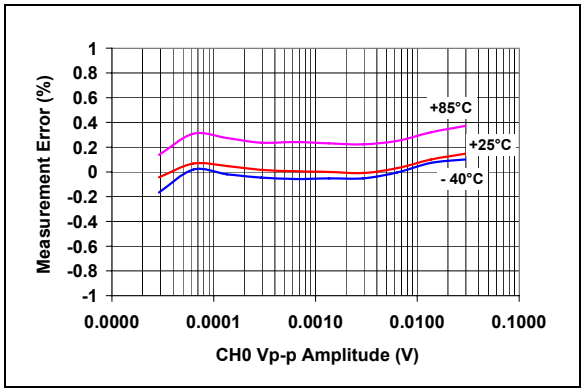



***FIGURE 2-2:*** *Active Power Measurement Error (Gain = 16, PF = 1).*

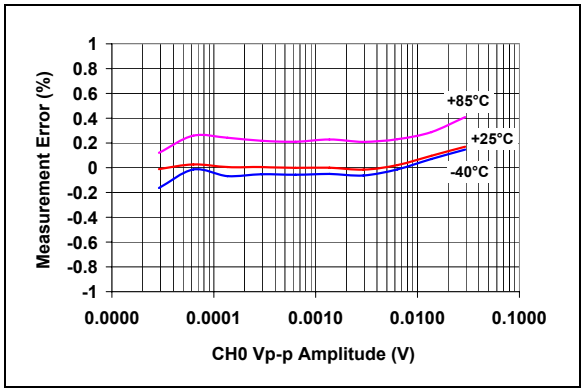



***FIGURE 2-5:*** *Active Power Measurement Error (Gain = 16, PF = 0.5).*

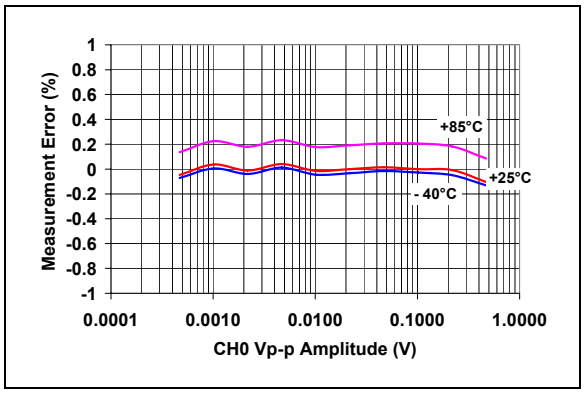



***FIGURE 2-3:*** *Active Power Measurement Error (Gain = 2, PF = 1).*

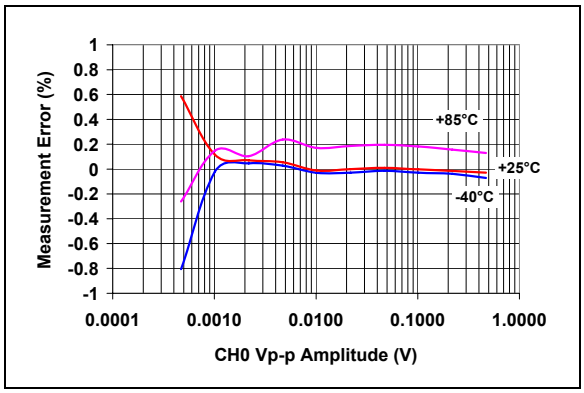



***FIGURE 2-6:*** *Active Power Measurement Error (Gain =2, PF = 0.5).*

**Note:** Unless otherwise specified, $DV_{DD}$, $AV_{DD}$ = 5V; $A_{GND}$, $D_{GND}$ = 0V; $V_{REF}$ = Internal, HPF = 1 (AC mode), MCLK = 3.58 MHz, CH1 input = 660 $mV_{P-P}$ at 50 Hz, CH0 amplitude sweeps at 50 Hz.

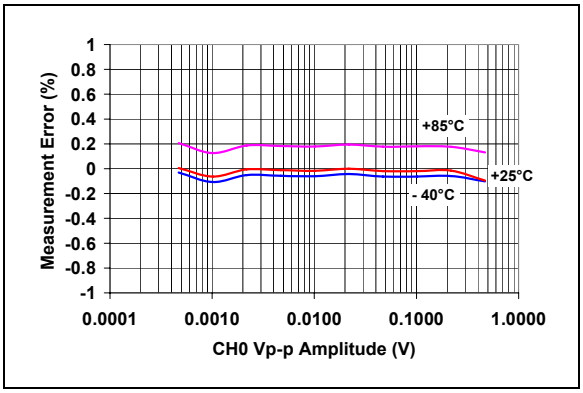



***FIGURE 2-7:*** *Active Power Measurement Error (Gain = 1, PF = 1).*

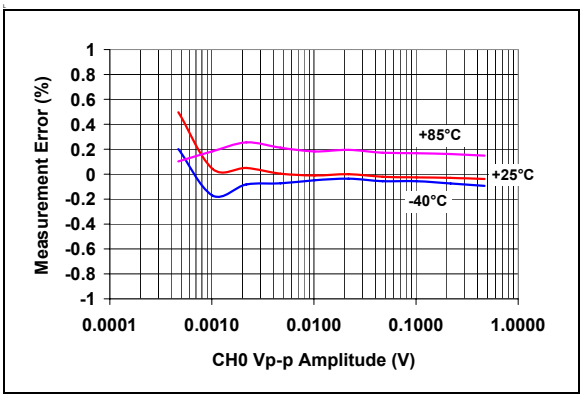



***FIGURE 2-8:*** *Active Power Measurement Error (Gain = 1, PF = 0.5).*

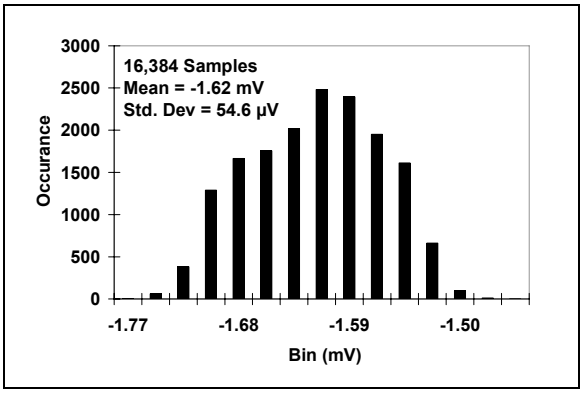



***FIGURE 2-9:*** *Channel 0 Offset Error (DC Mode, HPF off, G = 1, PF = 1).*

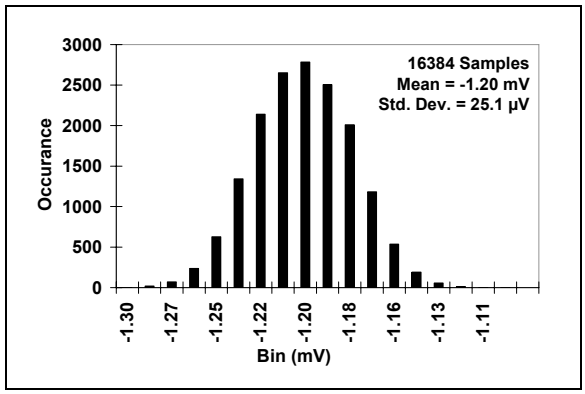



***FIGURE 2-10:*** *Channel 0 Offset Error (DC Mode, HPF off, G = 2, PF = 1).*

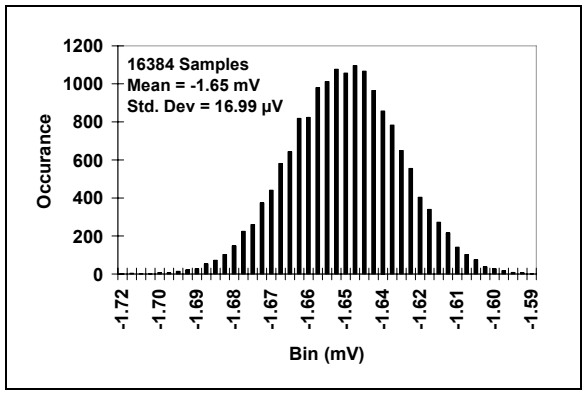



***FIGURE 2-11:*** *Channel 0 Offset Error (DC Mode, HPF off, G = 8, PF = 1).*

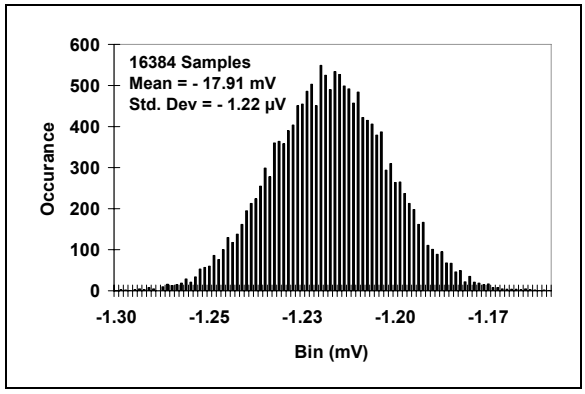



***FIGURE 2-12:*** *Channel 0 Offset Error (DC Mode, HPF Off, G = 16, PF = 1).*

**Note:** Unless otherwise specified, $DV_{DD}$, $AV_{DD}$ = 5V; $A_{GND}$, $D_{GND}$ = 0V; $V_{REF}$ = Internal, HPF = 1 (AC mode), MCLK = 3.58 MHz, CH1 input = 660 $mV_{P-P}$ at 50 Hz, CH0 amplitude sweeps at 50 Hz.

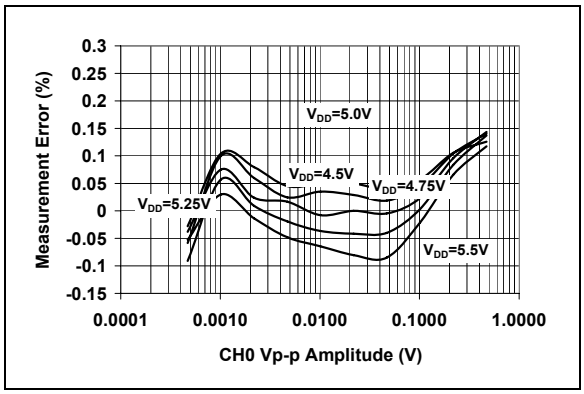



***FIGURE 2-13:*** *Active Power Measurement Error over $V_{DD}$, Internal $V_{REF}$ (G = 16, PF = 1).*

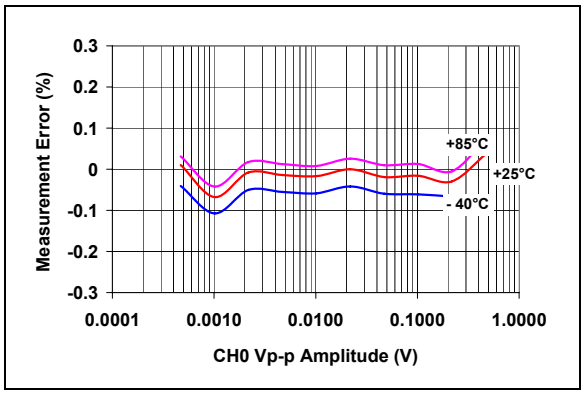



***FIGURE 2-16:*** *Active Power Measurement Error with External $V_{REF}$ (G = 1, PF = 1).*

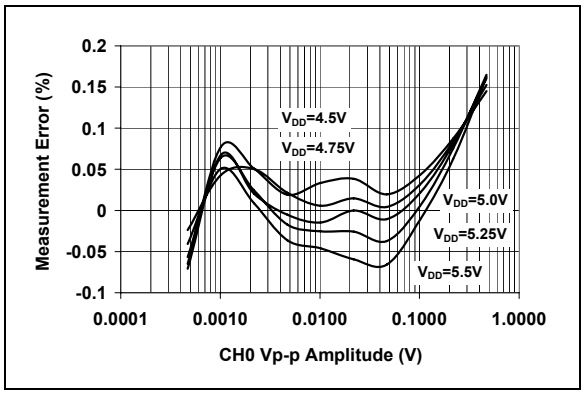



***FIGURE 2-14:*** *Active Power Measurement Error over $V_{DD}$, External $V_{REF}$ (G = 1, PF = 1).*

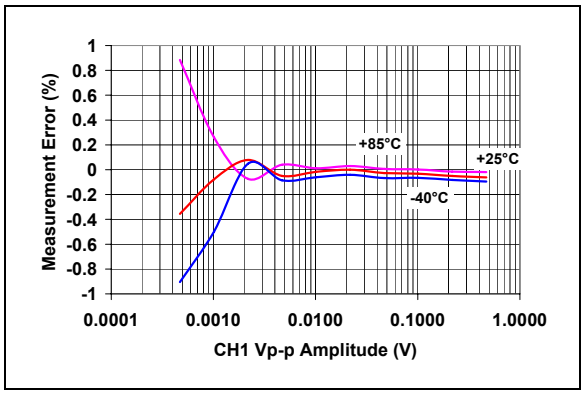



***FIGURE 2-17:*** *Active Power Measurement Error with External $V_{REF}$ (G = 1, PF = 0.5).*

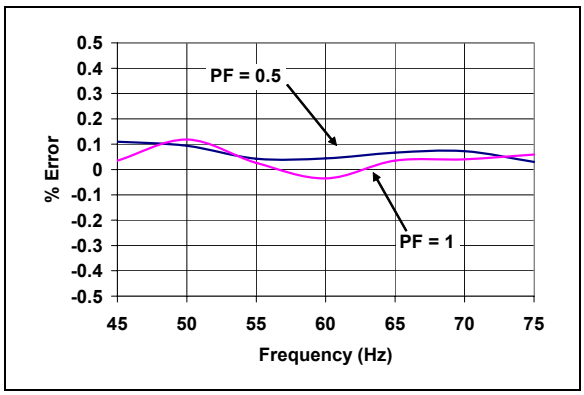



***FIGURE 2-15:*** *Active Power Measurement Error vs. Input Frequency (G = 16).*

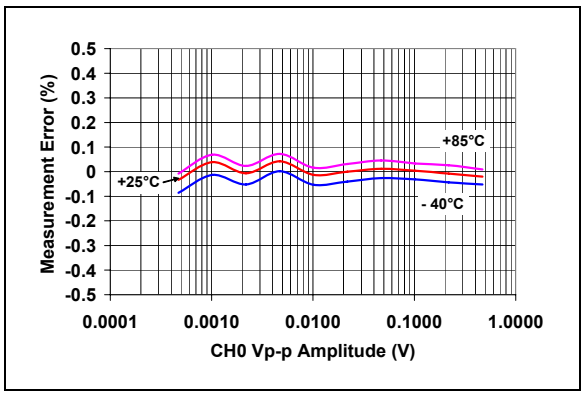



***FIGURE 2-18:*** *Active Power Measurement Error with External $V_{REF}$ (G = 2, PF = 1).*

**Note:** Unless otherwise specified, $DV_{DD}$, $AV_{DD}$ = 5V; $A_{GND}$, $D_{GND}$ = 0V; $V_{REF}$ = Internal, HPF = 1 (AC mode), MCLK = 3.58 MHz, CH1 input = 660 $mV_{P-P}$ at 50 Hz, CH0 amplitude sweeps at 50 Hz.

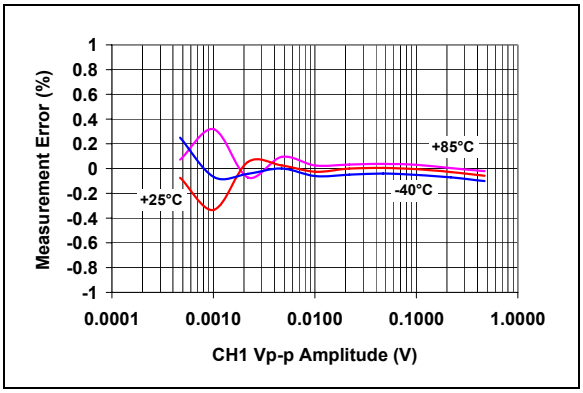



***FIGURE 2-19:*** *Active Power Measurement Error with External $V_{REF}$ (G = 2, PF = 0.5).*

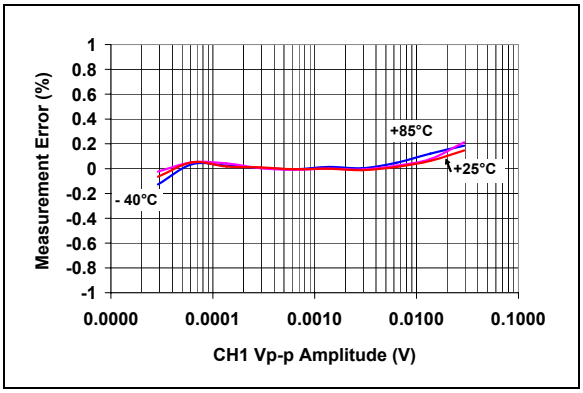



***FIGURE 2-22:*** *Active Power Measurement Error with External $V_{REF}$ (G = 16, PF = 1).*

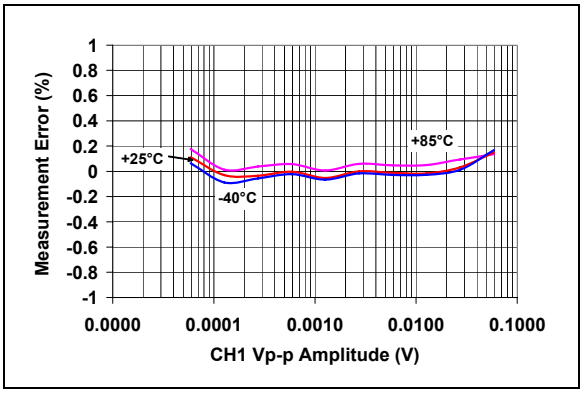



***FIGURE 2-20:*** *Active Power Measurement Error with External $V_{REF}$ (G = 8, PF = 1).*

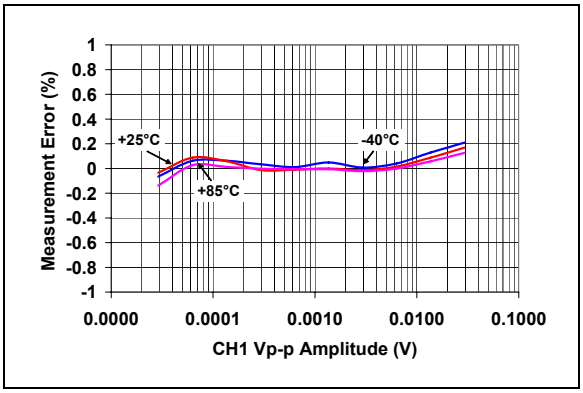



***FIGURE 2-23:*** *Active Power Measurement Error with External $V_{REF}$ (G =16, PF = 0.5).*

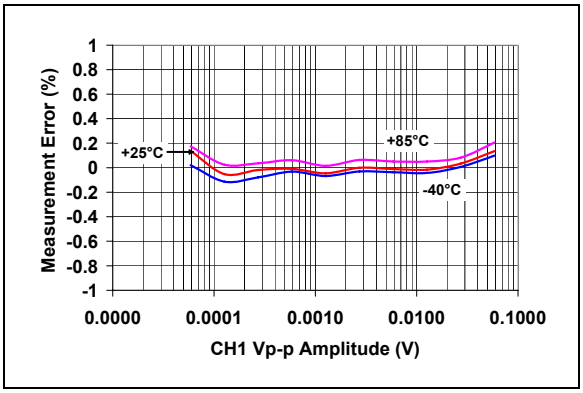



***FIGURE 2-21:*** *Active Power Measurement Error with External $V_{REF}$ (G = 8, PF = 0.5).*

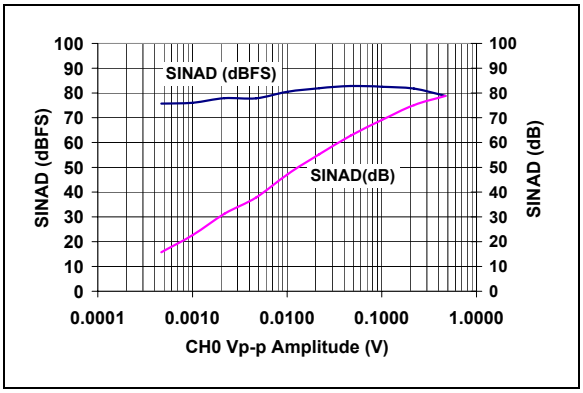



***FIGURE 2-24:*** *Signal-to-Noise and Distortion Ratio vs. Input Signal Amplitude (G = 1).*

**Note:** Unless otherwise specified, $DV_{DD}$, $AV_{DD}$ = 5V; $A_{GND}$, $D_{GND}$ = 0V; $V_{REF}$ = Internal, HPF = 1 (AC mode), MCLK = 3.58 MHz, CH1 input = 660 $mV_{P-P}$ at 50 Hz, CH0 amplitude sweeps at 50 Hz.

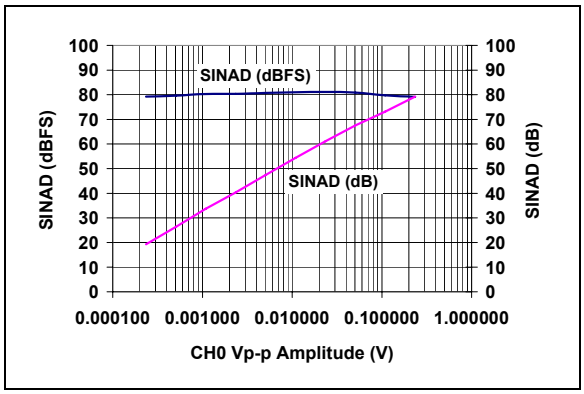



***FIGURE 2-25:*** *Signal-to-Noise and Distortion Ratio vs. Input Signal Amplitude (G = 2).*

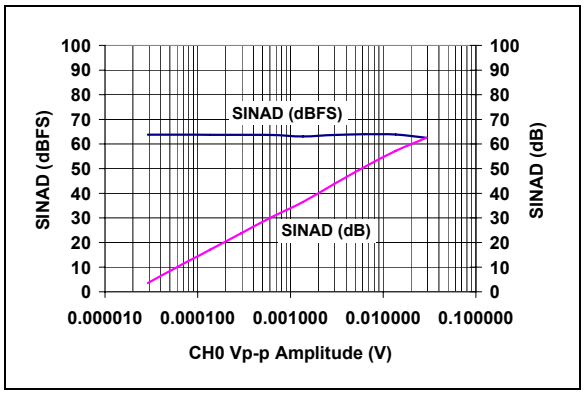



***FIGURE 2-27:*** *Signal-to-Noise and Distortion Ratio vs. Input Signal Amplitude (G = 16).*

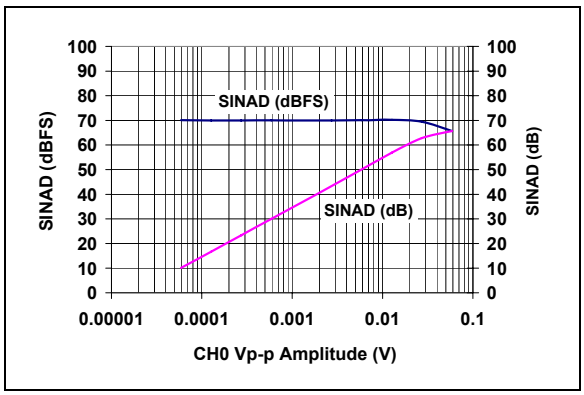



***FIGURE 2-26:*** *Signal-to-Noise and Distortion Ratio vs. Input Signal Amplitude (G = 8).*

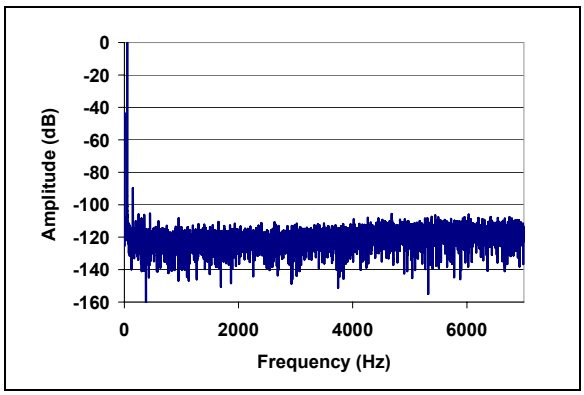



***FIGURE 2-28:*** *Frequency Spectrum, 50 Hz Input Signal.*

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | $DV_{DD}$ | Digital Power Supply Pin |
| 2 | HPF | High-Pass Filters Control Logic Pin |
| 3 | $AV_{DD}$ | Analog Power Supply Pin |
| 4 | NC | No Connect |
| 5 | CH0+ | Non-Inverting Analog Input Pin for Channel 0 (Current Channel) |
| 6 | CH0- | Inverting Analog Input Pin for Channel 0 (Current Channel) |
| 7 | CH1- | Inverting Analog Input Pin for Channel 1 (Voltage Channel) |
| 8 | CH1+ | Non-Inverting Analog Input Pin for Channel 1 (Voltage Channel) |
| 9 | $\overline{MCLR}$ | Master Clear Logic Input Pin |
| 10 | REFIN/OUT | Voltage Reference Input/Output Pin |
| 11 | $A_{GND}$ | Analog Ground Pin, Return Path for internal analog circuitry |
| 12 | SCK / F2 | Serial Clock or Frequency Control for $HF_{OUT}$ Logic Input Pin |
| 13 | SDI / F1 | Serial Data Input or Frequency Control for $F_{OUT0/1}$ Logic Input Pin |
| 14 | $\overline{CS}$ / F0 | Chip Select or Frequency Control for $F_{OUT0/1}$ Logic Input Pin |
| 15 | G1 | Gain Control Logic Input Pin |
| 16 | G0 | Gain Control Logic Input Pin |
| 17 | OSC1 | Oscillator Crystal Connection Pin or Clock Input Pin |
| 18 | OSC2 | Oscillator Crystal Connection Pin or Clock Output Pin |
| 19 | NC | No Connect |
| 20 | SDO / NEG | Serial Data Out or Negative Power Logic Output Pin |
| 21 | $D_{GND}$ | Digital Ground Pin, Return Path for Internal Digital Circuitry |
| 22 | $HF_{OUT}$ | High-Frequency Logic Output Pin (Intended for Calibration) |
| 23 | $F_{OUT1}$ | Differential Mechanical Counter Logic Output Pin |
| 24 | $F_{OUT0}$ | Differential Mechanical Counter Logic Output Pin |

### 3.1 Digital $V_{DD}$ ($DV_{DD}$)

$DV_{DD}$ is the power supply pin for the digital circuitry within the MCP3909.

This pin requires appropriate bypass capacitors and should be maintained to 5V ±10% for specified operation. Refer to **Section 6.0 "Applications Information"**.

### 3.2 High-Pass Filter Input Logic Pin (HPF)

HPF controls the state of the high-pass filter in both input channels. A logic '1' enables both filters, removing any DC offset coming from the system or the device. A logic '0' disables both filters allowing DC voltages to be measured.

### 3.3 Analog $V_{DD}$ ($AV_{DD}$)

$AV_{DD}$ is the power supply pin for the analog circuitry within the MCP3909.

This pin requires appropriate bypass capacitors and should be maintained to 5V ±10% for specified operation. Refer to **Section 6.0 "Applications Information"**.

### 3.4 Current Channel (CH0-, CH0+)

CH0- and CH0+ are the fully differential analog voltage input channels for the current measurement, containing a PGA for small-signal input, such as shunt current sensing. The linear and specified region of this channel is dependant on the PGA gain. This corresponds to a maximum differential voltage of ±470 mV/G and maximum absolute voltage, with respect to $A_{GND}$, of ±1V. Up to ±6V can be applied to these pins without the risk of permanent damage.

Refer to **Section 1.0 "Electrical Characteristics"**.

### 3.5 Voltage Channel (CH1-,CH1+)

CH1- and CH1+ are the fully differential analog voltage input channels for the voltage measurement. The linear and specified region of these channels have a maximum differential voltage of ±660 mV and a maximum absolute voltage of ±1V, with respect to $A_{GND}$. Up to ±6V can be applied to these pins without the risk of permanent damage.

Refer to **Section 1.0 "Electrical Characteristics"**.

### 3.6 Master Clear ($\overline{MCLR}$)

$\overline{MCLR}$ controls the reset for both delta-sigma ADCs, all digital registers, the SINC filters for each channel and all accumulators post multiplier. The $\overline{MCLR}$ pin is also used to change pin functionality and enter the serial interface mode. A logic '0' resets all registers and holds both ADCs in a Reset condition. The charge stored in both ADCs is flushed and their output is maintained to 0x0000h. The only block consuming power on the digital power supply during Reset is the oscillator circuit.

### 3.7 Reference (REFIN/OUT)

REFIN/OUT is the output for the internal 2.4V reference. This reference has a typical temperature coefficient of 15 ppm/°C and a tolerance of ±2%. In addition, an external reference can also be used by applying voltage to this pin within the specified range. This pin requires appropriate bypass capacitors to $A_{GND}$, even when using the internal reference only.

Refer to **Section 6.0 "Applications Information"**.

### 3.8 Analog Ground ($A_{GND}$)

$A_{GND}$ is the ground connection to internal analog circuitry (ADCs, PGA, band gap reference, POR). To ensure accuracy and noise cancellation, this pin must be connected to the same ground as $D_{GND}$, preferably with a star connection. If an analog ground plane is available, it is recommended that this device be tied to this plane of the PCB. This plane should also reference all other analog circuitry in the system.

### 3.9 Serial Clock Input or F2 Frequency Control Pin

This dual function pin can act as either the serial clock input for SPI communication or the F2 selection for the high-frequency output and low-frequency output pin ranges, changing the value of the constants $F_C$ and $H_{FC}$ used in the device transfer function. $F_C$ and $H_{FC}$ are the frequency constants that define the period of the output pulses for the device.

### 3.10 Serial Data Input or F1 Frequency Control Pin

This dual function pin can act as either the serial data input for SPI communication or the F1 selection for the high-frequency output and low-frequency output pin ranges, changing the value of the constants $F_C$ and $H_{FC}$ used in the device transfer function. $F_C$ and $H_{FC}$ are the frequency constants that define the period of the output pulses for the device.

### 3.11 Chip Select ($\overline{CS}$) or F0 Frequency Control Pin

This dual function pin can act as either the chip select for SPI communication or the F0 selection for the high-frequency output and low-frequency output pin ranges by changing the value of the constants $F_C$ and $H_{FC}$ used in the device transfer function. $F_C$ and $H_{FC}$ are the frequency constants that define the period of the output pulses for the device.

### 3.12 Gain Control Logic Pins (G1, G0)

G1 and G0 select the PGA gain (G) on Channel 0 from four different values: 1, 2, 8 and 16.

### 3.13 Oscillator (OSC1, OSC2)

OSC1 and OSC2 provide the master clock for the device. A resonant crystal or clock source with a similar sinusoidal waveform must be placed across these pins to ensure proper operation. The typical clock frequency specified is 3.579545 MHz. However, the clock frequency can be within the range of 1 MHz to 4 MHz without disturbing measurement error. Appropriate load capacitance should be connected to these pins for proper operation.

A full-swing, single-ended clock source may be connected to OSC1 with proper resistors in series to ensure no ringing of the clock source due to fast transient edges.

### 3.14 Serial Data Output or Negative Power Output Logic Pin (NEG)

This dual function pin can act as either the serial data output for SPI communication or NEG. NEG detects the phase difference between the two channels and will go to a logic '1' state when the phase difference is greater than 90° (i.e., when the measured real power is negative). The output state is synchronous with the rising-edge of $HF_{OUT}$ and maintains the logic '1' until the real power becomes positive again and $HF_{OUT}$ shows a pulse.

### 3.15 Ground Connection ($D_{GND}$)

$D_{GND}$ is the ground connection to internal digital circuitry (SINC filters, multiplier, HPF, LPF, digital-to-frequency converter and oscillator). To ensure accuracy and noise cancellation, $D_{GND}$ must be connected to the same ground as $A_{GND}$, preferably with a star connection. If a digital ground plane is available, it is recommended that this device be tied to this plane of the Printed Circuit Board (PCB). This plane should also reference all other digital circuitry in the system.

### 3.16 High-Frequency Output ($HF_{OUT}$)

$HF_{OUT}$ is the high-frequency output of the device and supplies the instantaneous real-power information. The output is a periodic pulse output, with its period proportional to the measured real power, and to the $HF_C$ constant defined by F0, F1 and F2 pin logic states. This output is the preferred output for calibration due to faster output frequencies, giving smaller calibration times. Since this output gives instantaneous real power, the $2\omega$ ripple on the output should be noted. However, the average period will show minimal drift.

### 3.17 Frequency Output ($F_{OUT0}$, $F_{OUT1}$)

$F_{OUT0}$ and $F_{OUT1}$ are the frequency outputs of the device that supply the average real-power information. The outputs are periodic pulse outputs, with its period proportional to the measured real power, and to the $F_C$ constant, defined by F0 and F1 pin logic states. These pins include high-output drive capability for direct use of electromechanical counters and 2-phase stepper motors. Since this output supplies average real power, any $2\omega$ ripple on the output pulse period is minimal.

## 4.0 DEVICE OVERVIEW

The MCP3909 is an energy metering IC that serves two distinct functions that can operate simultaneously:

- Active Power Pulse Output
- Waveform Output via SPI Interface

For the active power output, the device supplies a frequency output proportional to active (real) power, and higher frequency output proportional to the instantaneous power for meter calibration.

For the waveform output, it can be used serially to gather 16-bit voltage channel and current channel A/D data, or 20-bit wide multiplier output data. Both channels use 16-bit, second-order, delta-sigma ADCs that oversample the input at a frequency equal to MCLK/4, allowing for wide dynamic range input signals.

A Programmable Gain Amplifier (PGA) increases the usable range on the current input channel (Channel 0). Figure 4-1 represents the simplified block diagram of the MCP3909, detailing its main signal processing blocks.

Two digital high-pass filters cancel the system offset on both channels such that the real-power calculation does not include any circuit or system offset. After being high-pass filtered, the voltage and current signals are multiplied to give the instantaneous power signal. This signal does not contain the DC offset components, such that the averaging technique can be efficiently used to give the desired active-power output.

### 4.1 Active Power

The instantaneous power signal contains the active-power information; it is the DC component of the instantaneous power. The averaging technique can be used with both sinusoidal and non-sinusoidal waveforms, as well as for all power factors. The instantaneous power is thus low-pass filtered in order to produce the instantaneous real-power signal.

A digital-to-frequency converter accumulates the instantaneous active real power information to produce output pulses with a frequency proportional to the average real power. The low-frequency pulses present at the $F_{OUT0}$ and $F_{OUT1}$ outputs are designed to drive electromechanical counters and two-phase stepper motors displaying the real-power energy consumed. Each pulse corresponds to a fixed quantity of real energy, selected by the F2, F1 and F0 logic settings. The $HF_{OUT}$ output has a higher frequency setting and less integration period such that it can represent the instantaneous real-power signal. Due to the shorter accumulation time, it enables the user to proceed to faster calibration under steady load conditions (see **Section 4.8 "Active Power $F_{OUT0/1}$ and $HF_{OUT}$ Output Frequencies"**).

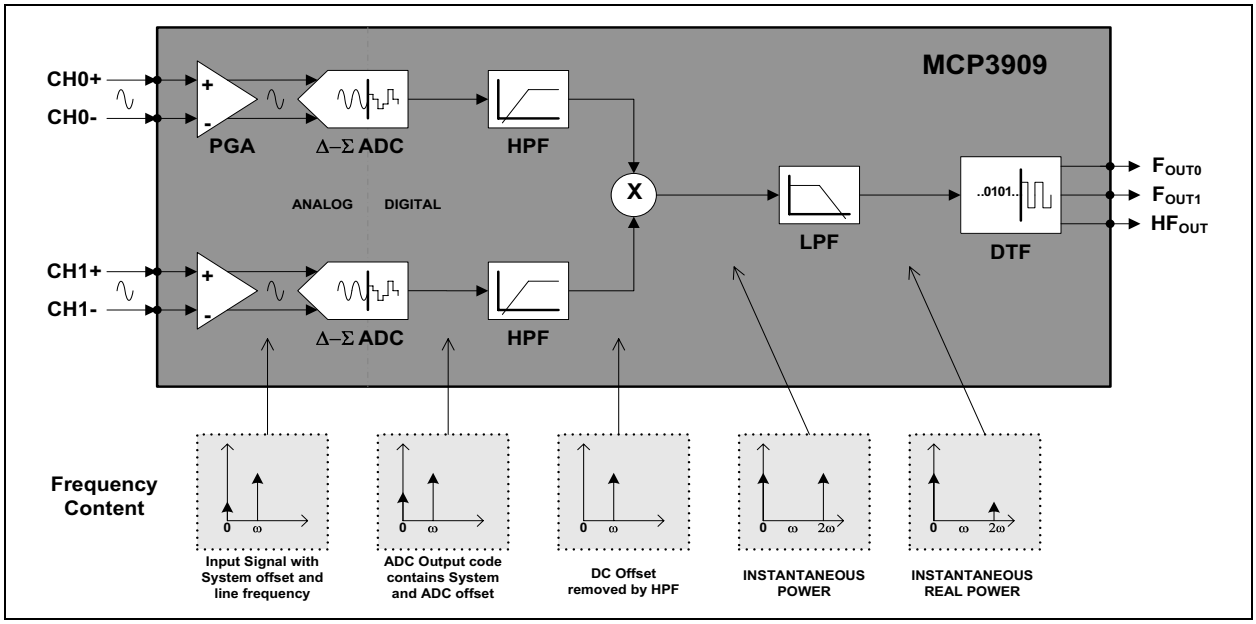



***FIGURE 4-1:*** *Active Power Signal Flow with Frequency Contents.*

## 4.2 Analog Inputs

The MCP3909 analog inputs can be connected directly to the current and voltage transducers (such as shunts or current transformers). Each input pin is protected by specialized ESD structures that are certified to pass 4 kV HBM and 400V MM contact charge. These structures also allow up to ±6V continuous voltage to be present at their inputs without the risk of permanent damage.

Both channels have fully differential voltage inputs for better noise performance. The absolute voltage at each pin relative to $A_{GND}$ should be maintained in the ±1V range during operation in order to ensure the measurement error performance. The common-mode signals should be adapted to respect both the previous conditions and the differential input voltage range. For best performance, the common-mode signals should be referenced to $A_{GND}$.

The current channel comprises a PGA on the front-end to allow for smaller signals to be measured without additional signal conditioning. The maximum differential voltage specified on Channel 0 is equal to ±470 mV/Gain (see Table 4-1). The maximum peak voltage specified on Channel 1 is equal to ±660 mV.

**TABLE 4-1: GAIN SELECTIONS**

| G1 | G0 | CH0 Gain | Maximum CH0 Voltage |
|---|---|---|---|
| 0 | 0 | 1 | ±470 mV |
| 0 | 1 | 2 | ±235 mV |
| 1 | 0 | 8 | ±60 mV |
| 1 | 1 | 16 | ±30 mV |

## 4.3 16-Bit Delta-Sigma A/D Converters

The ADCs used in the MCP3909 for both current and voltage channel measurements are delta-sigma ADCs. They comprise a second-order, delta-sigma modulator using a multi-bit DAC and a third-order SINC filter. The delta-sigma architecture is very appropriate for the applications targeted by the MCP3909 because it is a waveform-oriented converter architecture that can offer both high linearity and low distortion performance throughout a wide input dynamic range. It also creates minimal requirements for the anti-aliasing filter design. The multi-bit architecture used in the ADC minimizes quantization noise at the output of the converters without disturbing the linearity.

Both ADCs have a 16-bit resolution, allowing wide input dynamic range sensing. The oversampling ratio of both converters is 64. Both converters are continuously converting during normal operation. When the $\overline{MCLR}$ pin is low, both converters will be in Reset and output code 0x0000h. If the voltage at the inputs of the ADC is larger than the specified range, the linearity is no longer specified. However, the converters will continue to produce output codes until their saturation point is reached. The DC saturation point is around 700 mV for Channel 0 and 1V for Channel 1, using internal voltage reference. The output code will be locked past the saturation point to the maximum output code.

The clocking signals for the ADCs are equally distributed between the two channels in order to minimize phase delays to less than 1 MCLK period (see **Section 3.2 "High-Pass Filter Input Logic Pin (HPF)"**). The SINC filters main notch is positioned at MCLK/256 (14 kHz with MCLK = 3.58 MHz), allowing the user to be able to measure wide harmonic content on either channel. The data ready signals used for synchronization of the part with a MCU will come at a rate of MCLK/256 and a pipeline delay of 3 data readys is required to settle the SINC 3rd order digital filter. The magnitude response of the SINC filter is shown in Figure 4-2.

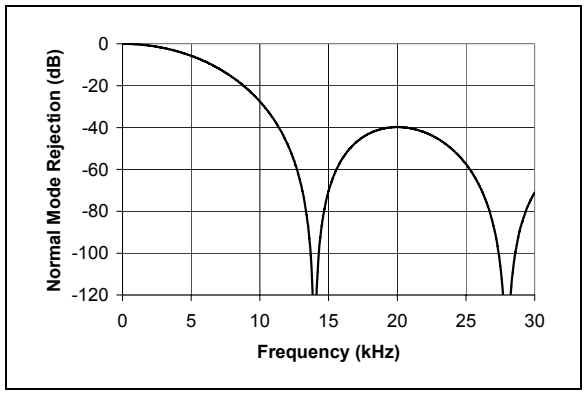



***FIGURE 4-2:*** *SINC Filter Magnitude Response (MCLK = 3.58 MHz).*

## 4.4 Ultra-Low Drift $V_{REF}$

The MCP3909 contains an internal voltage reference source specially designed to minimize drift over temperature. This internal $V_{REF}$ supplies reference voltage to both current and voltage channels ADCs. The typical value of this voltage reference is 2.4V ±100 mV. The internal reference has a very low typical temperature coefficient of ±15 ppm/°C, allowing the output frequencies to have minimal variation with respect to temperature since they are proportional to $(1/V_{REF})^2$.

The output pin for the voltage reference is REFIN/OUT. Appropriate bypass capacitors must be connected to the REFIN/OUT pin for proper operation (see **Section 6.0 "Applications Information"**). The voltage reference source impedance is typically 4 kΩ, which enables this voltage reference to be overdriven by an external voltage reference source.

If an external voltage reference source is connected to the REFIN/OUT pin, the external voltage will be used as the reference for both current and voltage channel ADCs. The voltage across the source resistor will then

be the difference between the internal and external voltage. The allowed input range for the external voltage source goes from 2.2V to 2.6V for accurate measurement error. A $V_{REF}$ value outside of this range will cause additional heating and power consumption due to the source resistor, which might affect measurement error.

## 4.5 Power-On Reset (POR)

The MCP3909 contains an internal POR circuit that monitors analog supply voltage $AV_{DD}$ during operation. This circuit ensures correct device startup at system power-up and system power-down events. The POR circuit has built-in hysteresis and a timer to give a high degree of immunity to potential ripple and noise on the power supplies, allowing proper settling of the power supply during power-up. A 0.1 µF decoupling capacitor should be mounted as close as possible to the $AV_{DD}$ pin, providing additional transient immunity (see **Section 6.0 "Applications Information"**).

The threshold voltage is typically set at 4V, with a tolerance of about ±5%. If the supply voltage falls below this threshold, the MCP3909 will be held in a Reset condition (equivalent to applying logic '0' on the $\overline{MCLR}$ pin). The typical hysteresis value is approximately 200 mV in order to prevent glitches on the power supply.

Once a power-up event has occurred, an internal timer prevents the part from outputting any pulse for approximately 1s (with MCLK = 3.58 MHz), thereby preventing potential metastability due to intermittent resets caused by an unsettled regulated power supply. Figure 4-3 illustrates the different conditions for a power-up and a power-down event in the typical conditions.

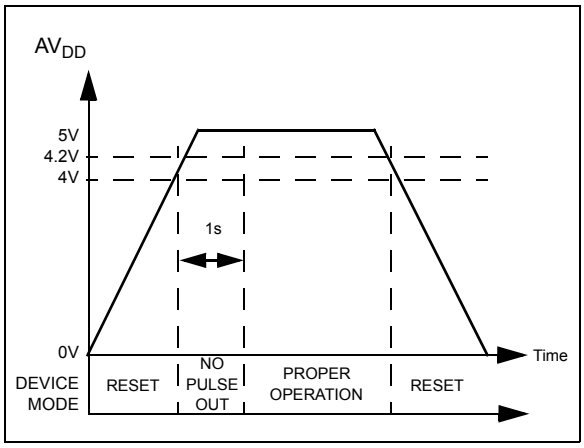



***FIGURE 4-3:*** *Power-on Reset Operation.*

## 4.6 High-Pass Filters and Multiplier

The active real-power value is extracted from the DC instantaneous power. Therefore, any DC offset component present on Channel 0 and Channel 1 affects the DC component of the instantaneous power and will cause the real-power calculation to be erroneous. In order to remove DC offset components from the instantaneous power signal, a high-pass filter has been introduced on each channel. Since the high-pass filtering introduces phase delay, identical high-pass filters are implemented on both channels. The filters are clocked by the same digital signal, ensuring a phase difference between the two channels of less than one MCLK period. Under typical conditions (MCLK = 3.58 MHz), this phase difference is less than 0.005°, with a line frequency of 50 Hz. The cut-off frequency of the filter (4.45 Hz) has been chosen to induce minimal gain error at typical line frequencies, allowing sufficient settling time for the desired applications. The two high-pass filters can be disabled by applying logic '0' to the HPF pin.

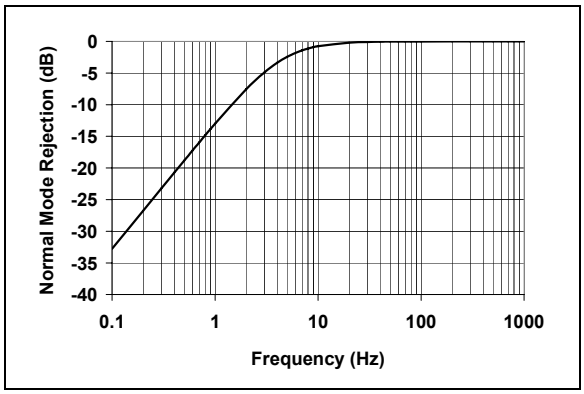



***FIGURE 4-4:*** *HPF Magnitude Response (MCLK = 3.58 MHz).*

The multiplier output gives the product of the two high-pass filtered channels, corresponding to instantaneous real power. Multiplying two sine wave signals by the same ω frequency gives a DC component and a 2ω component. The instantaneous power signal contains the real power of its DC component, while also containing 2ω components coming from the line frequency multiplication. These 2ω components come for the line frequency (and its harmonics) and must be removed in order to extract the real-power information. This is accomplished using the low-pass filter and DTF converter.

## 4.7 Active Power Low-Pass Filter and DTF Converter

For the active power signal calculation, the MCP3909 uses a digital low-pass filter. This low-pass filter is a first-order IIR filter, which is used to extract the active real-power information (DC component) from the instantaneous power signal. The magnitude response of this filter is detailed in Figure 4-5. Due to the fact that the instantaneous power signal has harmonic content (coming from the 2ω components of the inputs), and

since the filter is not ideal, there will be some ripple at the output of the low-pass filter at the harmonics of the line frequency.

The cut-off frequency of the filter (8.9 Hz) has been chosen to have sufficient rejection for commonly-used line frequencies (50 Hz and 60 Hz). With a standard input clock (MCLK = 3.58 MHz) and a 50 Hz line frequency, the rejection of the 2ω component (100 Hz) will be more than 20 dB. This equates to a 2ω component containing 10 times less power than the main DC component (i.e., the average active real power).

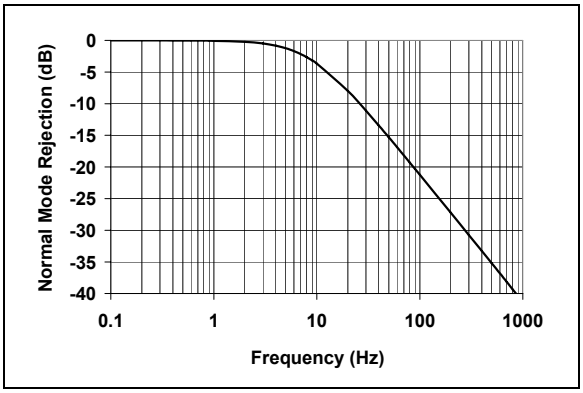



***FIGURE 4-5:*** *LPF1 Magnitude Response (MCLK = 3.58 MHz).*

The output of the low-pass filter is accumulated in the digital-to-frequency converter. This accumulation is compared to a different digital threshold for $F_{OUT0/1}$ and $HF_{OUT}$, representing a quantity of real energy measured by the part. Every time the digital threshold on $F_{OUT0/1}$ or $HF_{OUT}$ is crossed, the part will output a pulse (See **Section 4.8 "Active Power $F_{OUT0/1}$ and $HF_{OUT}$ Output Frequencies"**).

The equivalent quantity of real energy required to output a pulse is much larger for the $F_{OUT0/1}$ outputs than the $HF_{OUT}$. This is such that the integration period for the $F_{OUT0/1}$ outputs is much larger. This larger integration period acts as another low-pass filter so that the output ripple due to the 2ω components is minimal. However, these components are not totally removed, since realized low-pass filters are never ideal. This will create a small jitter in the output frequency. Averaging the output pulses with a counter or a MCU in the application will then remove the small sinusoidal content of the output frequency and filter out the remaining 2ω ripple.

$HF_{OUT}$ is intended to be used for calibration purposes due to its instantaneous power content. The shorter integration period of $HF_{OUT}$ demands that the 2ω component be given more attention. Since a sinusoidal signal average is zero, averaging the $HF_{OUT}$ signal in steady-state conditions will give the proper real energy value.

## 4.8 Active Power $F_{OUT0/1}$ and $HF_{OUT}$ Output Frequencies

The thresholds for the accumulated energy are different for $F_{OUT0/1}$ and $HF_{OUT}$ (i.e., they have different transfer functions). The $F_{OUT0/1}$ allowed output frequencies are quite low in order to allow superior integration time (see **Section 4.7 "Active Power Low-Pass Filter and DTF Converter"**). The $F_{OUT0/1}$ output frequency can be calculated with the following equation:

**EQUATION 4-1: $F_{OUT}$ FREQUENCY OUTPUT EQUATION**

$$F_{OUT}(Hz) = \frac{8.06 \times V_0 \times V_1 \times G \times F_C}{(V_{REF})^2}$$

Where:

- $V_0$ = the RMS differential voltage on Channel 0
- $V_1$ = the RMS differential voltage on Channel 1
- G = the PGA gain on Channel 0 (current channel)
- $F_C$ = the frequency constant selected
- $V_{REF}$ = the voltage reference

For a given DC input V, the DC and RMS values are equivalent. For a given AC input signal with amplitude of V, the equivalent RMS value is V/ sqrt(2), assuming purely sinusoidal signals. Note that since the real power is the product of two RMS inputs, the output frequencies of AC signals are half of the DC inputs ones, again assuming purely sinusoidal AC signals. The constant $F_C$ depends on the $F_{OUT0}$ and $F_{OUT1}$ digital settings. Table 4-2 shows $F_{OUT0/1}$ output frequencies for the different logic settings.

**TABLE 4-2: ACTIVE POWER OUTPUT FREQUENCY CONSTANT $F_C$ FOR FOUT0/1 ($V_{REF}$ = 2.4V)**

| F1 | F0 | $F_C$ (Hz) | $F_C$ (Hz) (MCLK = 3.58 MHz) | $F_{OUT}$ Frequency (Hz) with Full-Scale DC Inputs | $F_{OUT}$ Frequency (Hz) with Full-Scale AC Inputs |
|---|---|---|---|---|---|
| 0 | 0 | MCLK/$2^{21}$ | 1.71 | 0.74 | 0.37 |
| 0 | 1 | MCLK/$2^{20}$ | 3.41 | 1.48 | 0.74 |
| 1 | 0 | MCLK/$2^{19}$ | 6.83 | 2.96 | 1.48 |
| 1 | 1 | MCLK/$2^{18}$ | 13.66 | 5.93 | 2.96 |

The high-frequency output $HF_{OUT}$ has lower integration times and, thus, higher frequencies. The output frequency value can be calculated with the following equation:

**EQUATION 4-2: ACTIVE POWER $HF_{OUT}$ FREQUENCY OUTPUT EQUATION**

$$HF_{OUT}(Hz) = \frac{8.06 \times V_0 \times V_1 \times G \times HF_C}{(V_{REF})^2}$$

Where:

- $V_0$ = the RMS differential voltage on Channel 0
- $V_1$ = the RMS differential voltage on Channel 1
- G = the PGA gain on Channel 0 (current channel)
- $HF_C$ = the frequency constant selected
- $V_{REF}$ = the voltage reference

The constant $HF_C$ depends on the $F_{OUT0}$ and $F_{OUT1}$ digital settings with the Table 4-3.

The detailed timings of the output pulses are described in the **Timing Characteristics** table (see **Section 1.0 "Electrical Characteristics"** and Figure 1-1).

### 4.8.1 MINIMAL OUTPUT FREQUENCY FOR NO-LOAD THRESHOLD

The MCP3909 also includes, on each output frequency, a no-load threshold circuit that will eliminate any creep effects in the meter. The outputs will not show any pulse if the output frequency falls below the no-load threshold. This threshold only applies to the pulse outputs and does not gate any serial data coming from either the A/D output or the multiplier output. The minimum output frequency on $F_{OUT0/1}$ and $HF_{OUT}$ is equal to 0.0015% of the maximum output frequency (respectively $F_C$ and $HF_C$) for each of the F2, F1 and F0 selections (see Table 4-2 and Table 4-3); except when F2, F1, F0 = 011. In this last configuration, the no-load threshold feature is disabled. The selection of $F_C$ will determine the start-up current load. In order to respect the IEC standards requirements, the meter will have to be designed to allow start-up currents compatible with the standards by choosing the FC value matching these requirements. For additional applications information on no-load threshold, startup current and other meter design points, refer to AN994, *"IEC Compliant Active Energy Meter Design Using The MCP3905/6*", (DS00994).

**TABLE 4-3: OUTPUT FREQUENCY CONSTANT $HF_C$ FOR $HF_{OUT}$ ($V_{REF}$ = 2.4V)**

| F2 | F1 | F0 | $HF_C$ | $HF_C$ (Hz) | $HF_C$ (Hz) (MCLK = 3.58 MHz) | $HF_{OUT}$ Frequency (Hz) with full-scale AC Inputs |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 64 x $F_C$ | MCLK/$2^{15}$ | 109.25 | 27.21 |
| 0 | 0 | 1 | 32 x $F_C$ | MCLK/$2^{15}$ | 109.25 | 27.21 |
| 0 | 1 | 0 | 16 x $F_C$ | MCLK/$2^{15}$ | 109.25 | 27.21 |
| 0 | 1 | 1 | 2048 x $F_C$ | MCLK/$2^7$ | 27968.75 | 6070.12 |
| 1 | 0 | 0 | 128 x $F_C$ | MCLK/$2^{16}$ | 219.51 | 47.42 |
| 1 | 0 | 1 | 64 x $F_C$ | MCLK/$2^{16}$ | 219.51 | 47.42 |
| 1 | 1 | 0 | 32 x $F_C$ | MCLK/$2^{16}$ | 219.51 | 47.42 |
| 1 | 1 | 1 | 16 x $F_C$ | MCLK/$2^{16}$ | 219.51 | 47.42 |

## 5.0 SERIAL INTERFACE DESCRIPTION

### 5.1 Dual Functionality Pin And Serial Interface Overview

The MCP3909 device contains three serial modes that are accessible by changing the pin functionality of the NEG, F2, F1, and F0 pins to SDO, SCK, SDI and $\overline{CS}$, respectively.

These modes are entered by giving the MCP3909 device a serial command on these pins during a time window after device reset or POR. During this window of time, F2 acts as SCK, F1 acts as SDI and F0 acts as $\overline{CS}$. Once a serial mode has been entered, the device must be reset to disable mode functionality, or change to another serial mode. This is done by using MCLR pin or power on reset event.

During serial mode entry and the three serial modes, data is clocked into the device on the rising edge of SCK and out of the device on the falling edge of SCK.

The SPI data can be access at up to 20 MHz. This speed enables quick data retrieval in between conversion times. For 3-phase metering applications with multiple ADCs, this fast communication is essential to allow for power calculation windows between conversions, as shown in Figure 5-3.

After a serial mode has been entered, all blocks of the MCP3909 device are still operational. The PGA, A/D converters, HPF, multiplier, LPF, and other digital sections are still functional, allowing the device to have true dual functionality in energy metering systems.

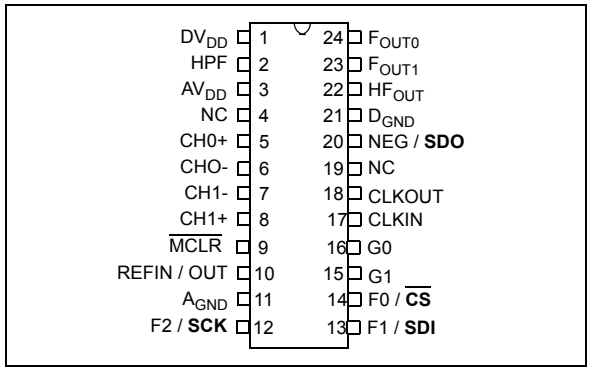



***FIGURE 5-1:*** *Dual Functionality Pins for the MCP3909.*

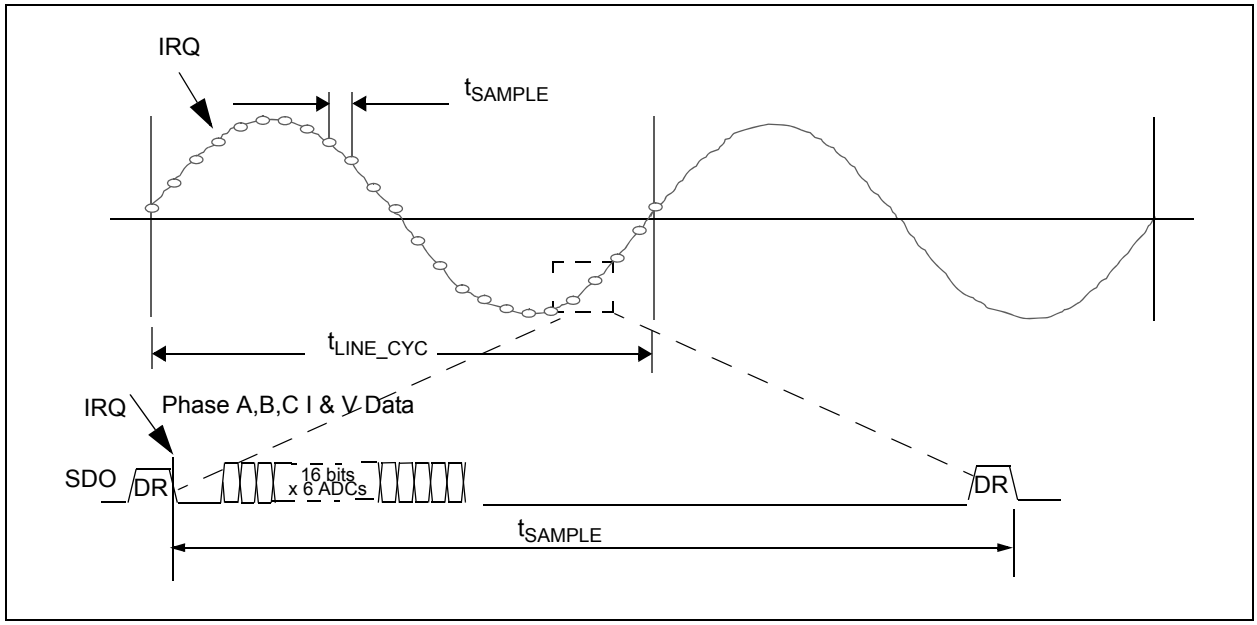



***FIGURE 5-2:*** *Data Access between Data Ready Pulses using SPI Interface for a 3-phase System.*

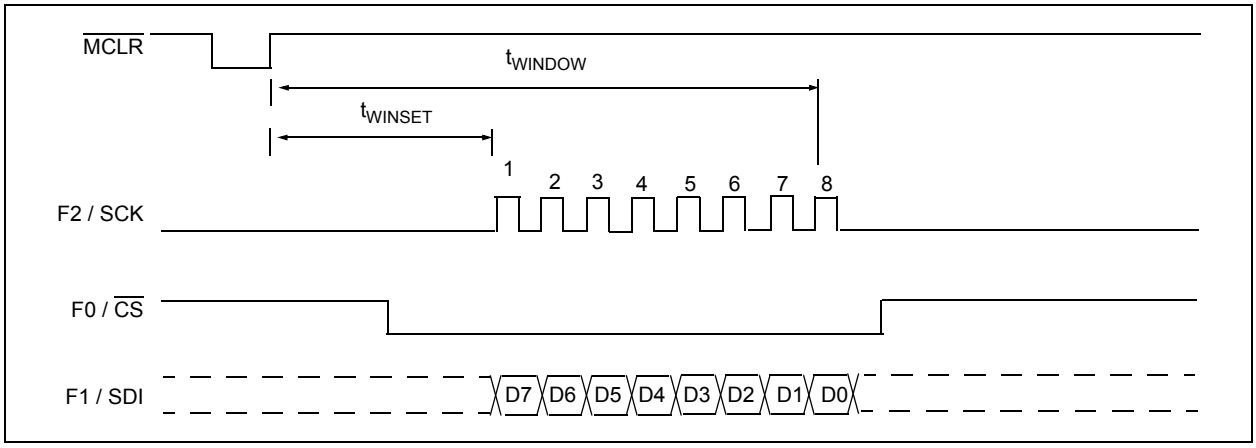



***FIGURE 5-3:*** *Dual Functionality Pin Serial Mode Entry Protocol.*

## 5.2 Serial Mode Entry Codes

The MCP3909 devices contains three different serial modes with data presented in 2's complement coding.

- Multiplier Output
- Dual Channel Output
- Filter Input

After entering any of these modes the active power calculation block is still functional and presents output pulses on $F_{OUT0}$, $F_{OUT1}$, and $HF_{OUT}$. For this reason, the F2, F1, F0 output frequency selection constant can be changed with multiple command bytes for serial mode entry.

The command bytes to enter these modes are described in Table 5-1.

**TABLE 5-1: ENTRY CODES**

| Command D7.....D0 | Serial Mode | Internal State of F2, F1, F0 Constants Frequency Selection During Serial Mode (1) | | |
|---|---|---|---|---|
| | | F2 | F1 | F0 |
| 1 0 1 0 0 0 0 1 | Multiplier Output | 0 | F1 pin | 1 |
| 1 0 1 0 1 0 0 1 | Multiplier Output | 1 | F1 pin | 1 |
| 1 0 1 0 0 1 0 0 | Dual Channel Output Pre HPF1 | 0 | F1 pin | 1 |
| 1 0 1 0 1 1 0 0 | Dual Channel Output Post HPF1 | 1 | F1 pin | 1 |
| 1 0 1 0 1 0 1 0 | Filter Input | 1 | 0 | F0 pin |
| 1 0 1 0 1 1 1 0 | Filter Input | 1 | 1 | F0 pin |
| 1 0 1 0 0 0 1 0 | Filter Input | 0 | 0 | F0 pin |
| 1 0 1 0 0 1 1 0 | Filter Input | 0 | 1 | F0 pin |

**Note 1:** The active power frequency outputs $F_{OUT0}$, $F_{OUT1}$, and $HF_{OUT}$ remain active after serial mode entry. Leaving the SDI (F1) and $\overline{CS}$ (F0) pins at a known state after serial communication will control the frequency selection. The HPF pin controls the state of the HPF for the multiplier mode output and the output pulses from the active power D to F block.

## 5.3 Multiplier Output Mode

Multiplier mode allows the user to retrieve the output of the multiplier on the MCP3909 device. Data is presented in a 20 bit (19 bit + sign) protocol, MSB first. A data ready flag (DR) is output for every MCLK/256 clock cycles and a new multiplier output value is ready. If the multiplier value is not clocked out of the device it will be over-written. Data is clocked out on the rising edge of SCK.

$$Multiplier\ Code = \frac{(CH0^{+} - CH0^{-})(CH1^{+} - CH1^{-})}{V_{REF}\,2} \bullet 524288 \bullet 8.06 \bullet G$$

**TABLE 5-2: MULTIPLIER OUTPUT MODE CODING**

| Binary | Decimal |
|---|---|
| 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | +524287 |
| 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 | +524286 |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0 |
| 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | -1 |
| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 | -524287 |
| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | -524288 |

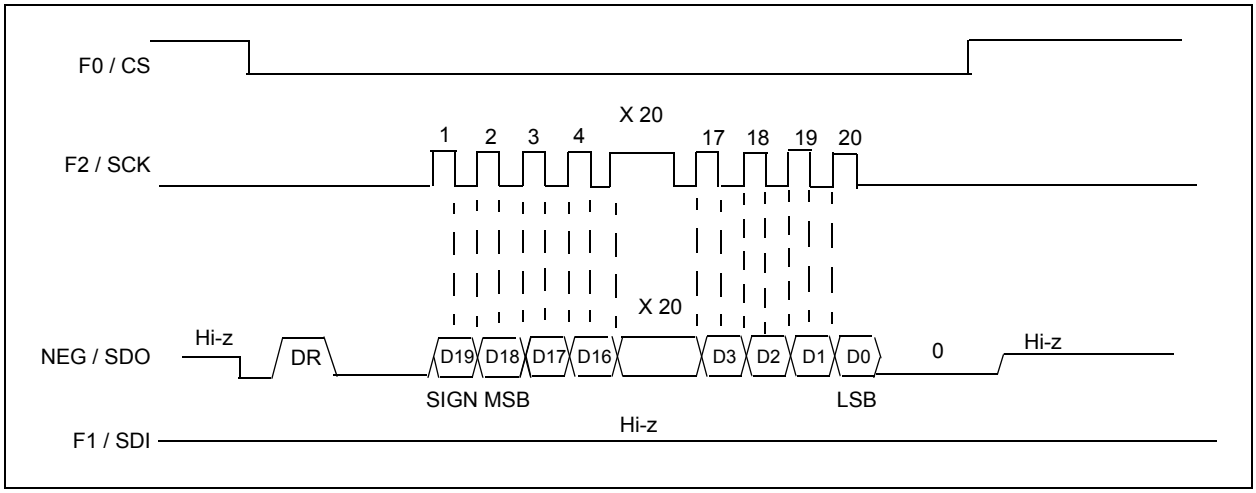



***FIGURE 5-4:*** *Multiplier Output Mode.*

## 5.4 Dual Channel Output Mode

This mode allows the user to retrieve the individual channel information from the ADC outputs. The ADC outputs of both channels are synchronized together and their data ready is represented by the data ready pulse on SDO. If the ADC output values are not clocked out of the device, they will be over-written. A 32-bit data word is given, each channel is 16 bits (15 bits + sign), presented in 2's complement coding. Channel 1 comes first then channel 0.

A data ready flag (DR) is output for every MCLK / 256 clock cycles and a new filter output value is ready. If the dual channel output values are not clocked, and is not clocked out of the device, they will be over-written.

The following formulas relate the channel input voltages to their respective output code. The code locks to +32767 on the positive side, and to -32768 on the negative side.

$$Channel\ 0\ Code = \left(\frac{(V_{IN+} - V_{IN-})}{V_{REF}}\right) \times 32768 \times \left(\sqrt{8.06 \times \frac{0.66}{0.47}}\right) \times PGA$$

$$Channel\ 1\ Code = \frac{(V_{IN+} - V_{IN-})}{V_{REF}} \times 32768 \times \left(\sqrt{8.06 \times \frac{0.47}{0.66}}\right)$$

**TABLE 5-3: CHANNEL OUTPUT MODE CODING**

| Binary | Decimal |
|---|---|
| 0 111 1111 1111 1111 | + 32,767 |
| 0 111 1111 1111 1110 | + 32,766 |
| 0 000 0000 0000 0000 | 0 |
| 1 111 1111 1111 1111 | -1 |
| 1 000 0000 0000 0001 | - 32,767 |
| 1 000 0000 0000 0000 | - 32,768 |

## 5.5 High-Pass Filter Control

There are two options for the channel output data. The first options collects the channel data pre-high pass filter, or the output of the SINC filter of the delta sigma modulator. The second option collects the channel data post high pass filter. It is important to note that the HPF pin controls the state of the high pass filter for this second option. If the HPF pin is low, the post high pass filter mode will output all zero's. This HPF pin must be high to access the post HPF data in the channel output mode.

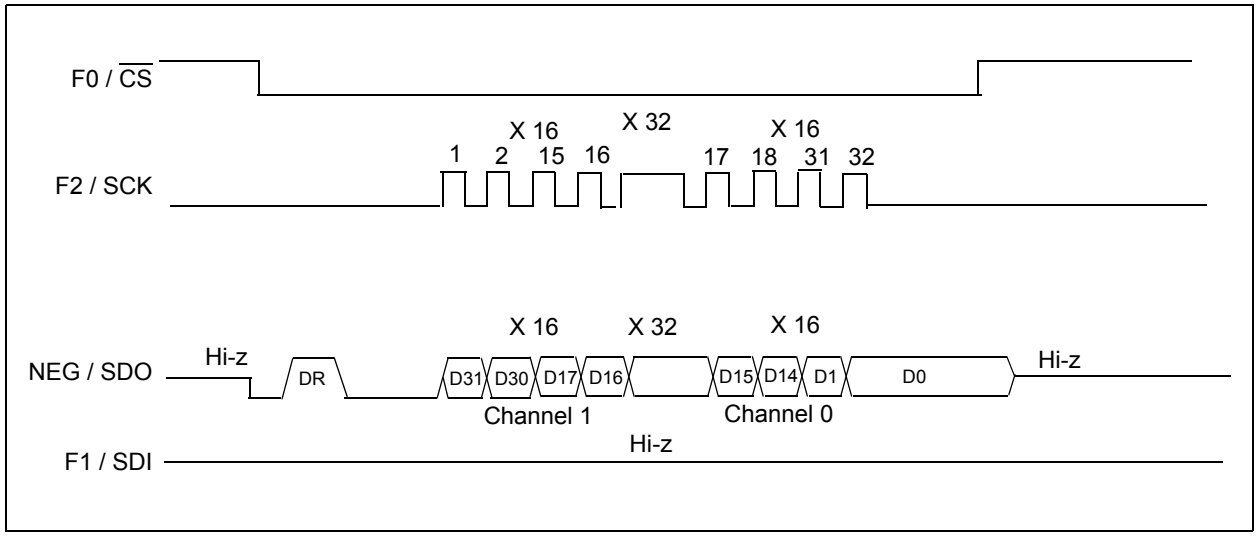



***FIGURE 5-5:*** *Dual Channel Output Mode.*

## 5.6 Filter Input Mode

The filter input mode allows the user to feed the MCP3909 device an input to the LPF1. Data is received MSB first. The MCP3909 will treat this data as if it were the output of the multiplier and will LPF and D-F the result as normal, giving the resulting output frequency on $HF_{OUT}$, $F_{OUT0}$ and $F_{OUT1}$. See Tables 4-2 and 4-3 for transfer functions of the output frequencies.

When using filter input mode, the user must wait for the data ready flag (DR) to appear on SDO before attempting to clock in data to the device. The user can not access either the multiplier output or the dual channel output while in this mode.

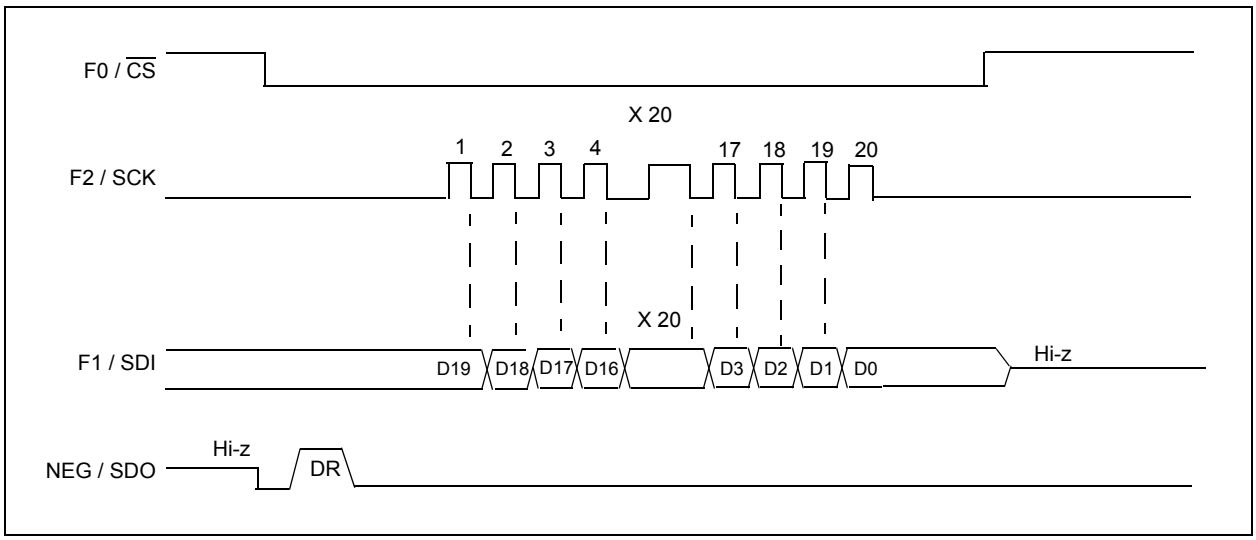



***FIGURE 5-6:*** *Filter Input Mode.*

## 5.7 Using the MCP3909 with Microcontroller (MCU) SPI Ports

With microcontroller SPI ports, it is required to send groups of eight bits. It is also required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge, or vice versa depending on the mode.

### 5.7.1 SPI MODE DEFINITIONS

The following table represents the standard SPI mode terminology, the respective PIC bit settings, and a description of compatibility for the MCP3909 device.

The MCP3909 works in SPI mode 0,1 mode, that is the data is clocked out of the part on the **rising** edge and clocked in on the **falling** edge of SCK.

**TABLE 5-4: SPI MODE COMPATIBILITY**

| Standard SPI Mode Terminology | PIC Control Bits State | | MCP3909 Compatibility | Description |
|---|---|---|---|---|
| | CKP | CKE | | |
| 0,0 | 0 | 1 | — | Idle state for clock is low level, transmit (from PIC) occurs from active to idle clock state |
| 0,1 | 0 | 0 | √ | Idle state for clock is low level, transmit (from PIC) occurs from idle to active clock state |
| 1,0 | 1 | 1 | — | Idle state for clock is high level, transmit (from PIC) occurs from active to idle clock state |
| 1,1 | 1 | 0 | — | Idle state for clock is high level, transmit (from PIC) occurs from idle to active clock state |

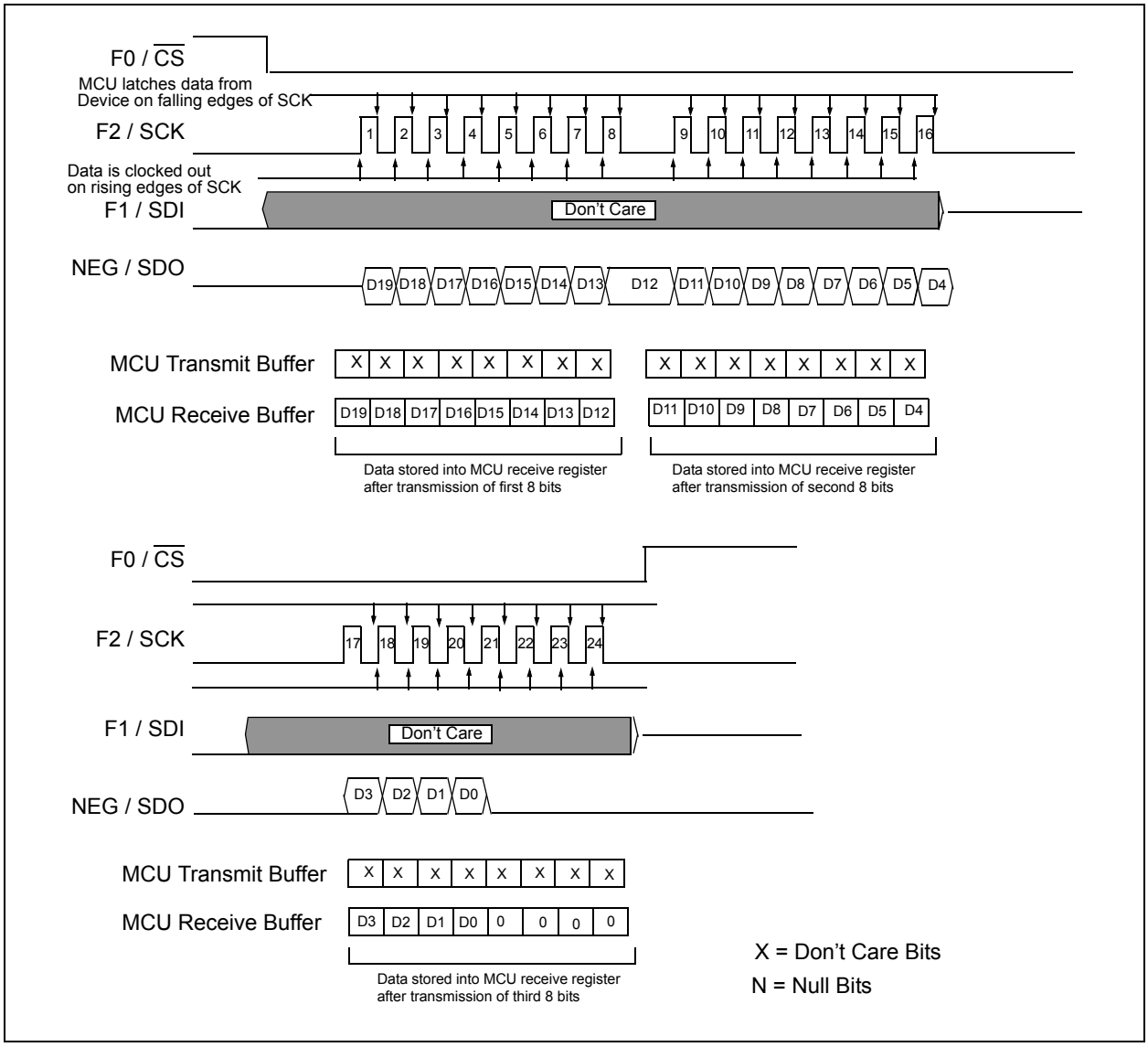



***FIGURE 5-7:*** *Multiplier Output Mode 1 SPI Communication using 8-bit segments (Mode 0,1: SCK idles low).*

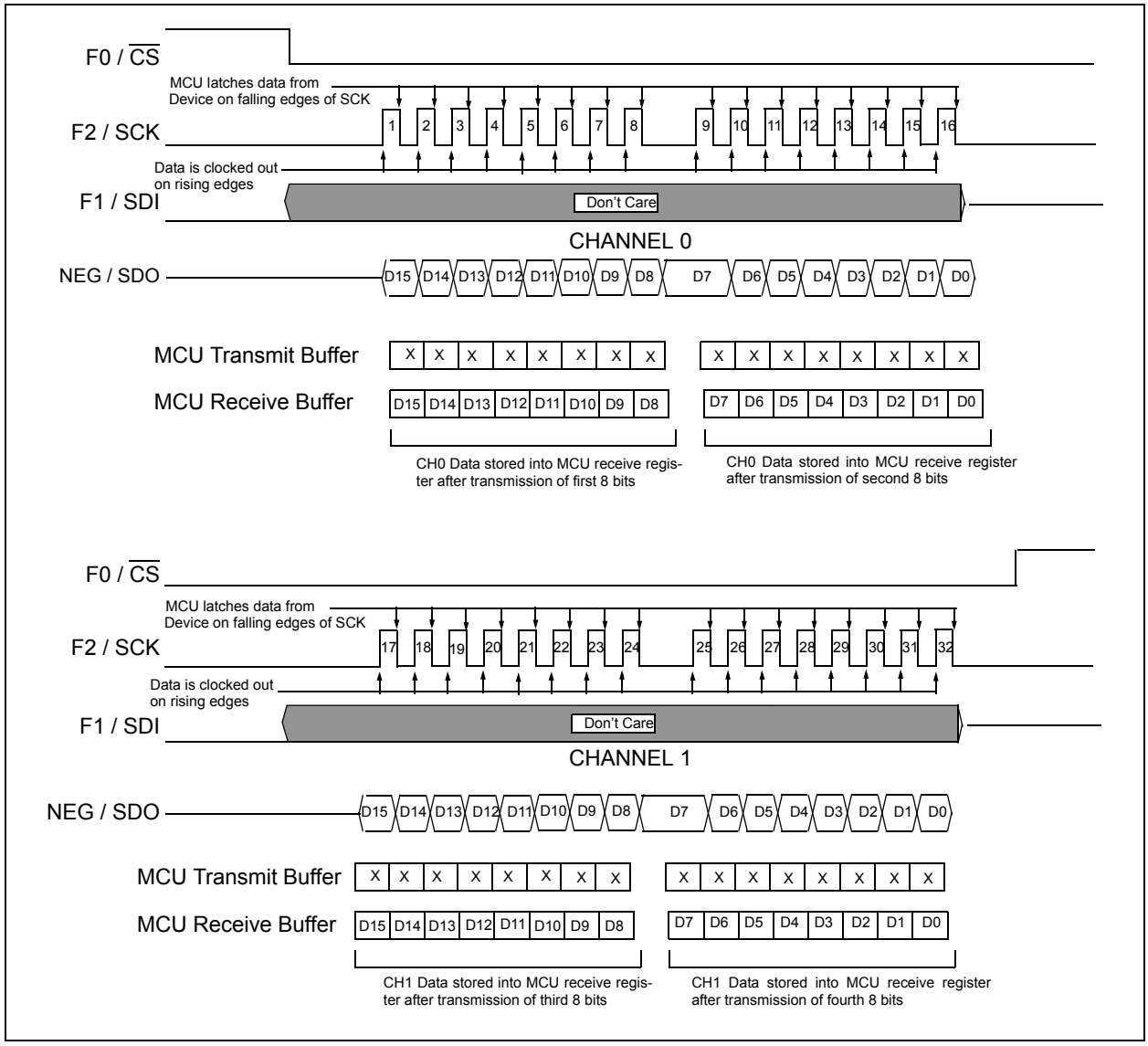



***FIGURE 5-8:*** *Dual Channel Output Mode SPI Communication using 8-bit segments (Mode 0,1: SCK idles low).*

## 6.0 APPLICATIONS INFORMATION

The following application figures represent meter designs using the MCP3909 device. Some of these applications ideas are available as fully function meter reference designs and demo boards. For complete schematic and for fully function meter designs, visit Microchip's web page for demo board and reference design availability.

### 6.1 Performing RMS, Apparent Power, and Active Power using MCP3909 Waveform data

Figure 6-1 represents power calculations from waveform data based on a PIC MCU and MCP3909 device. The PIC MCU accomplishes the following energy meter calculation outputs per phase, per line cycle:

- RMS Current
- RMS Voltage
- Active Power
- Apparent Power

Output registers for the power quantities and calibration registers for phase, offset, gain, and LSB adjustment are available through a serial interface to the PIC microcontroller. See Microchip's web page for firmware solution and demo board.

The example signal flow here shows 4 output power quantities and 6 calibration registers. For a 60 Hz design that is using 128 samples per line cycle for the power calculation the MCP3909 would have a new data ready pulse every 130 µs. The SPI communication to gather 16-bits x 2 channels at 10 MHz is approximately 3.2 µs, leaving ~125 µs for the power calculations before the next sample is ready.

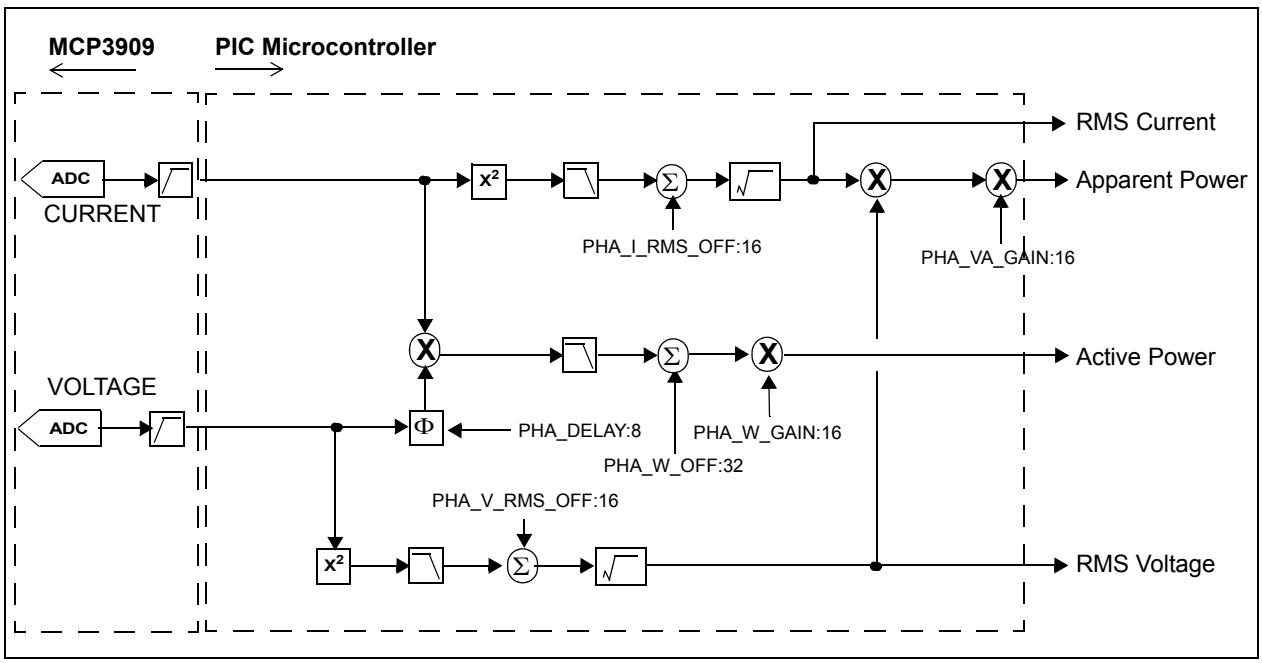



***FIGURE 6-1:*** *Power Calculations from Waveform sampling using PIC MCU. Register names shown are used on MCP3909 Energy Meter Reference Design.*

## 6.2 Achieving Line Cycle Sampling with Zero Blind Cycles

In most energy meter applications, it will be necessary to have $2^N$ samples for each 50 or 60 Hz line cycle, where N is typically 64, 128 or 256. Controlling the MCLK of the MCP3909 allows you to control the sample rate and ultimately the data ready (DR) pulses for coherent waveform sampling. The following scheme shows how the TIMER and COMPARATOR modules of the PIC MCU can be used to generate the clock for the MCP3909 from either a PLL internal MCLK. For class 0.2 or class 0.1 meter designs that require harmonic analysis using a PLL is recommended to shift sample rate with line cycle drift, e.g. line cycle changes from 60 Hz to 59.1 Hz. This is shown as option 1 in Figure 6-2.

A simpler lower cost option would be to choose a frequency that would give an integer number of line cycles for exactly 50 Hz (or 60 Hz). This is possible using a 39.3216 MHz crystal for the PIC18F device.

Figure 6-2 shows example clock frequencies to achieve 128 samples for each line cycle, 1.63 MHz for a 50 Hz line, or 1.96 MHz for a 60 Hz line. The MCP3909 clock can operate from 1 MHz to 4 MHz.

Using this approach, the PIC MCU can gather the waveform data immediately after the data ready pulse, at up to 10 MHz. The remainder of the time can be used to calculate the power measurements to achieve true line cycle sampling with zero blind cycles.

For more information and firmware, see the Microchip's web page for demo board information.

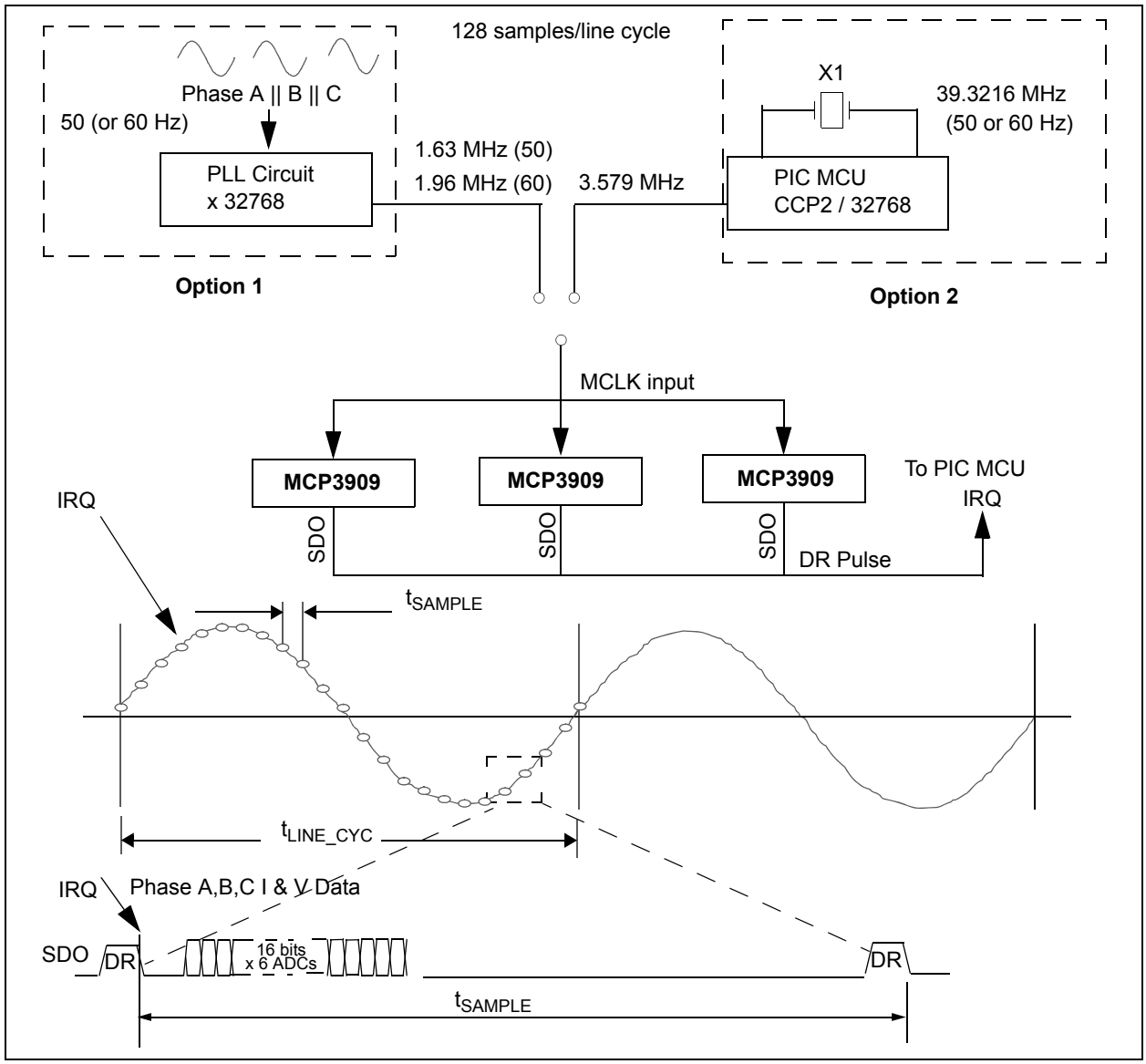



***FIGURE 6-2:*** *Using the PIC device to control the MCP3909 MCLK to achieve $2^N$ samples per line cycle, 3-phase sampling shown with 6 ADCs*

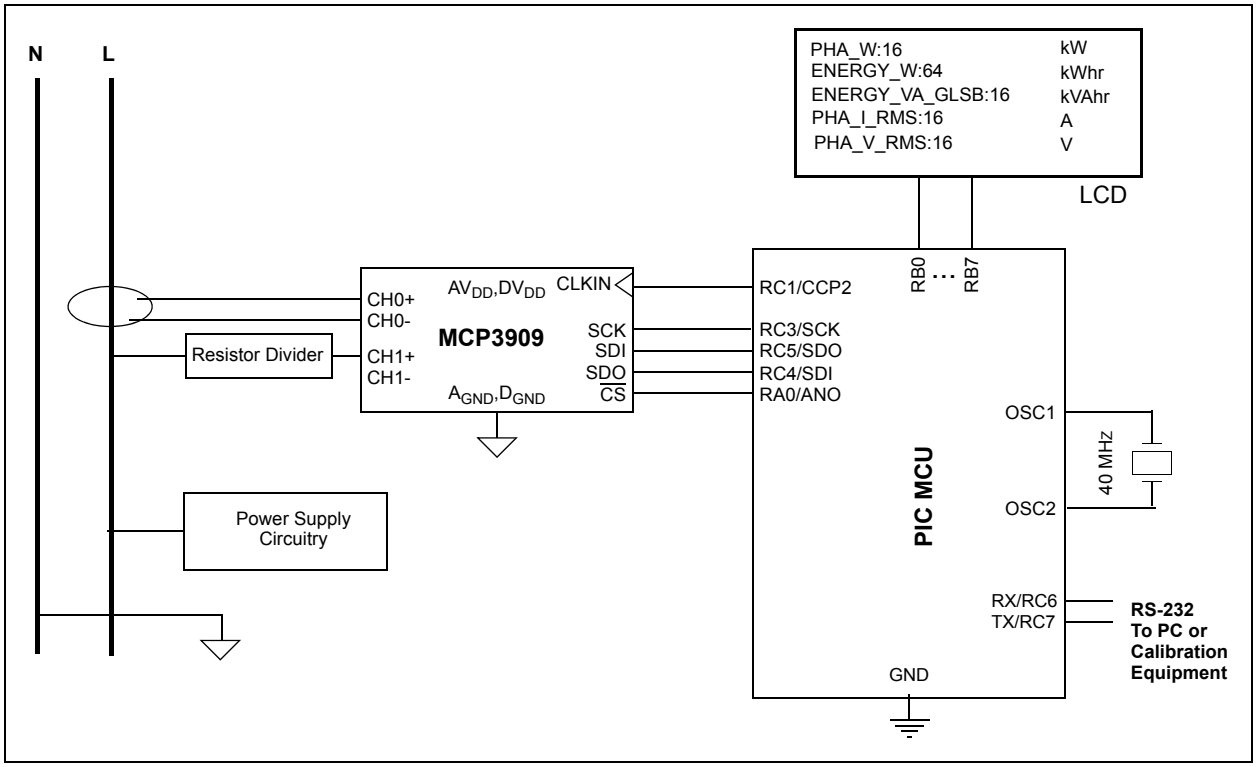



***FIGURE 6-3:*** *Simplified MCU Based Energy Meter.*

## 6.3 Meter Calibration

To achieve meter calibration the MCP3909 waveform samples are adjusted during the power calculations on the PIC MCU. In Figure 6-3, this interface is shown via RS-232 on the PIC microcontroller. This process is streamlined using calibration software available from Microchip's web site.

## 6.4 Analog Meter Design Tips

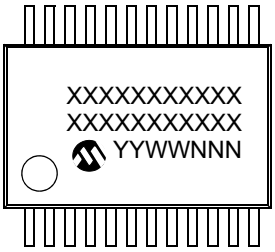
For analog design tips and PCB layout recommendations, refer to AN994, *"IEC Compliant Active Energy Meter Design Using The MCP390X"* (DS00994). This application note includes all required energy meter design information, including the following:

- Meter rating and current sense choices
- Shunt design
- PGA selection
- F2, F1, F0 selection
- Meter calibration
- Anti-aliasing filter design
- Compensation for parasitic shunt inductance
- EMC design
- Power supply design
- No-Load threshold
- Start-up current
- Accuracy Testing Results from MCP390X-based meter
- EMC Testing Results from MCP390X-based meter

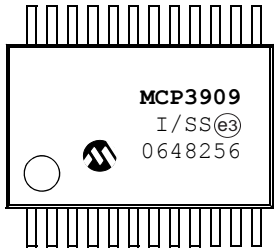
## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information

**24-Lead SSOP**




**Examples:**

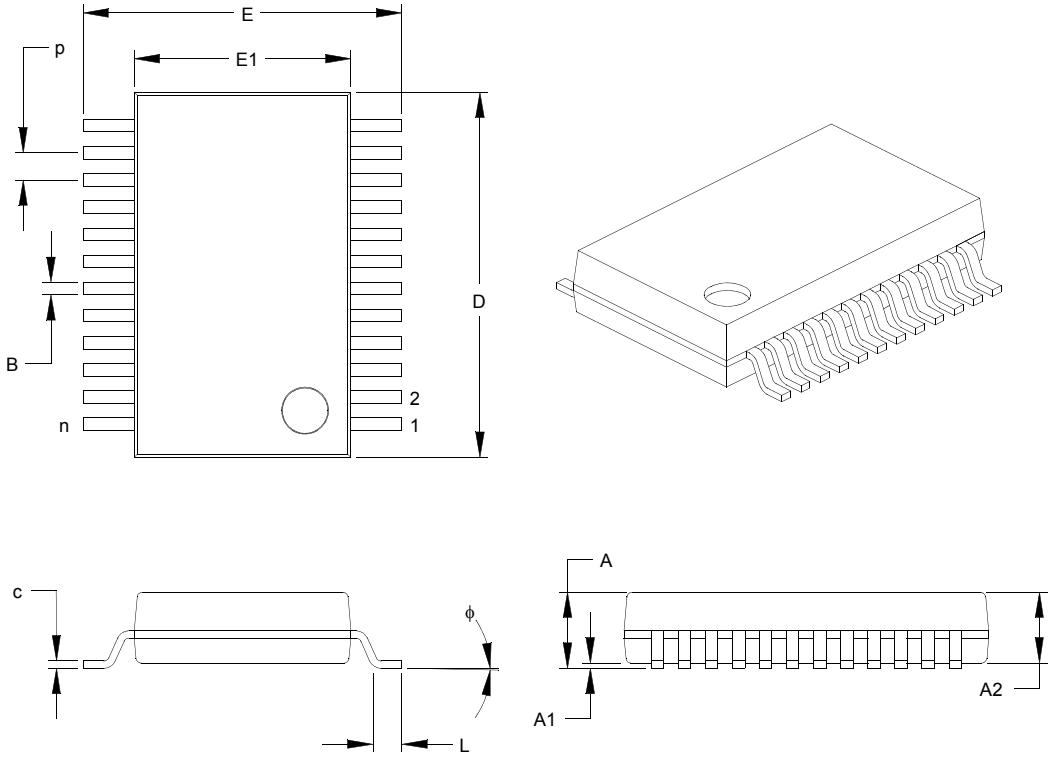



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 24-Lead Plastic Shrink Small Outline (SS) (SSOP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 24 | | | 24 | |
| Pitch | p | | .026 BSC. | | | 0.65 BSC. | |
| Overall Height | A | .068 | .073 | .078 | 1.73 | 1.86 | 1.99 |
| Molded Package Thickness | A2 | .066 | .068 | .070 | 1.68 | 1.73 | 1.78 |
| Standoff | A1 | .002 | .005 | .008 | 0.05 | 0.13 | 0.21 |
| Overall Width | E | .301 | .307 | .311 | 7.65 | 7.80 | 7.90 |
| Molded Package Width | E1 | .205 | .209 | .212 | 5.20 | 5.30 | 5.38 |
| Overall Length | D | .318 | .323 | .328 | 8.07 | 8.20 | 8.33 |
| Foot Length | L | .025 | .030 | .037 | 0.63 | 0.75 | 0.95 |
| Lead Thickness | c | .004 | .006 | – | 0.09 | 0.15 | – |
| Foot Angle | ϕ | 0° | 4° | 8° | 0° | 4° | 8° |
| Lead Width | B | .010 | – | .015 | 0.25 | – | 0.38 |

***** Controlling Parameter

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed.010" (0.254mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

JEDEC Equivalent: MO-150

Drawing No. C04-132

Revised 9-14-05

# APPENDIX A: REVISION HISTORY

## Revision A (December 2006)

- Original Release of this Document.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | –X | /XX |
|---|---|---|
| Device | Temperature Range | Package |

| | | |
|---|---|---|
| Device: | MCP3909: | Energy Metering IC |
| | MCP3909T: | Energy Metering IC (Tape and Reel) |
| Temperature Range: | I | = -40°C to +85°C |
| Package: | SS | = Plastic Shrink Small Outline (209 mil Body), 24-lead |

**Examples:**

a) MCP3909-I/SS: Energy Metering IC Industrial Temperature, 24LD SSOP.

b) MCP3909T-I/SS: Tape and Reel, Energy Metering IC Industrial Temperature, 24LD SSOP.

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



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