DATA SHEET

TDA6118JF
Video output amplifier

Product specification
Supersedes data of 2002 May 06

2004 Aug 26

Philips
Semiconductors

Video output amplifier TDA6118JF

FEATURES

- Bandwidth independent of gain
- Rise and fall times of 21 ns at 100 V (p-p)
- Very simple application
- Switchable gain of –50 and –80
- Switchable output black level of 126 V and 155 V
- Internal reference voltage
- Cathode current measurement output for black-current stabilization
- Thermal protection.

GENERAL DESCRIPTION

The TDA6118JF is a video output amplifier in a plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package (SOT111-1) using high-voltage DMOS technology, and is intended to drive the cathode of a colour CRT directly. To obtain maximum performance, the amplifier should be used with black-current control.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6118JF/N2/S1	DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1

BLOCK DIAGRAM

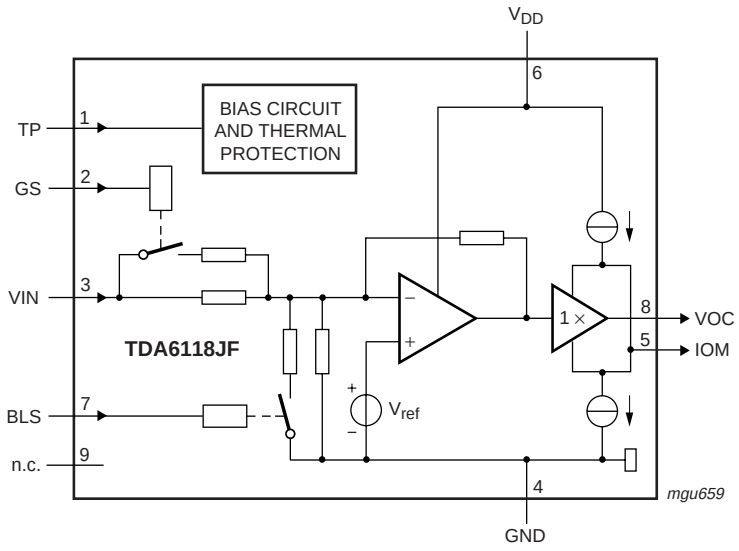


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TP	1	thermal protection input
GS	2	gain selection input
VIN	3	inverting input
GND	4	ground
IOM	5	black-current measurement output
V_{DD}	6	supply voltage (200 V)
BLS	7	black level selection input
VOC	8	cathode output
n.c.	9	not connected

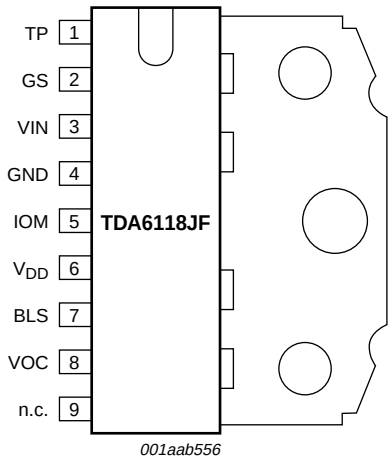


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are measured with respect to pin GND.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	250	V
V_n	voltage on pins				
	VOC		0	V_{DD}	V
	VIN, IOM, BLS and GS		0	12	V
	TP		0	24	V
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−20	+150	°C
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM)	−2000	+2000	V
		Machine Model (MM)	−300	+300	V

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

QUALITY SPECIFICATION

In accordance with the *"General Quality Specification For Integrated Circuits ("SNW-FQ-611)".*

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient		56	K/W
$R_{th(j-fin)}$	thermal resistance from junction to fin	note 1	12.2	K/W

Note

1. An external heatsink is necessary.

Thermal protection

The TDA6118JF is protected against overheating through a thermal protection circuit (see Fig.1). This circuit realizes a decrease of internal quiescent currents at high temperatures and limits the bandwidth and the static and dynamic power dissipation (see Fig.3).

Typical values for the bandwidth:

- 25 % decrease at T_{prot} = 145 °C
- 50 % decrease at T_{prot} = 155 °C.

Where T_{prot} is the temperature on the spot of the thermal protection circuit.

The equivalent thermal resistance network is given in Fig.4.

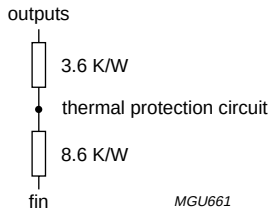
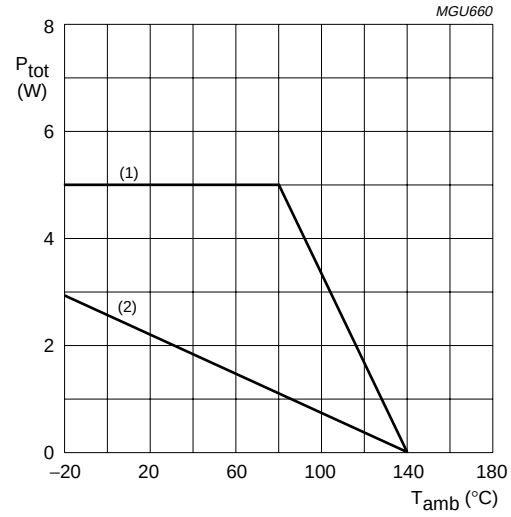


Fig.4 Equivalent thermal resistance network.



(1) Infinite heatsink.
(2) No heatsink.

Fig.3 Power derating curves.

CHARACTERISTICS

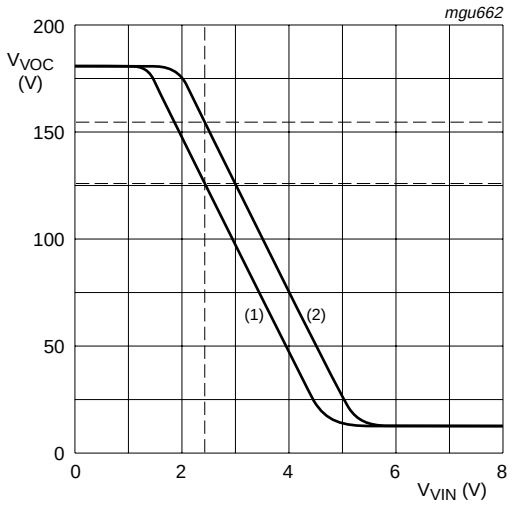
V_{DD} = 200 V; V_{VOC} = 100 V; V_{IOM} = 3.0 V; V_{GS} = 0 V; V_{BLS} = 0 V; $R_{th(fin-a)}$ = 18 K/W; T_{amb} = 25 °C; measured in test circuit of Fig.9; equivalent load of 10 pF which consists of parasitic and cathode capacitance; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_q	quiescent supply current		10	12.5	15	mA
PSRR	power supply rejection ratio	f_i < 50 kHz; note 1	–	54	–	dB
Operating range						
V_{DD}	supply voltage		180	–	210	V
T_j	junction temperature		–20	–	+140	°C
Input (pin VIN)						
R_i	input impedance	pin GS connected to ground	1060	1780	2500	Ω
		pin GS left open-circuit	670	1110	1550	Ω
Amplifier						
G	amplifier gain	pin GS connected to ground	–45	–50	–55	
		pin GS left open-circuit	–72	–80	–88	
B	bandwidth	V_{VOC} = 40 V (p-p) sine wave	–	22	–	MHz
		V_{VOC} = 100 V (p-p) sine wave	–	17	–	MHz
V_{ref}	internal reference voltage		–	2.4	–	V
Cathode output (pin VOC); see Figs 5 and 6						
V_{VOC}	DC output voltage	pin BLS connected to ground	115	126	137	V
		pin BLS left open-circuit	142	155	168	V
$V_{VOC(max)}$	maximum output voltage	V_{VIN} = 0 V	V_{DD} – 18	–	–	V
$V_{VOC(min)}$	minimum output voltage	V_{VIN} = 7 V; I_{VOC} = 0 mA	–	–	6	V
		V_{VIN} = 7 V; I_{VOC} = 7 mA	–	–	17	V
$\Delta V_{VOC(T)}$	output voltage variation with temperature	pin BLS left open-circuit; T_j = 0 °C to 100 °C	–	0.5	–	V/°C
$I_{VOC(max)}$	maximum output current	50 V < V_{VOC} < V_{DD} – 50 V	50	70	–	mA
Black-current measurement output (pin IOM)						
$I_{IOM(offset)}$	output offset current	I_{VOC} = 0 mA; V_{VIN} = 0 V to 5.5 V; V_{IOM} = 1.8 V to 6 V	–50	0	+50	μA
$\Delta I_{IOM}/\Delta I_{VOC}$	gain of I_{VOC} to I_{IOM} current transfer	–100 μA < I_{VOC} < 5 mA; V_{VIN} = 0 V to 5.5 V; V_{IOM} = 1.8 V to 6 V	0.9	1.0	1.1	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Cathode output timing (pin VOC); see Figs 7 and 8; note 2						
$t_{o(r)}$	output rise time	10 % to 90 % output	17	21	25	ns
$t_{o(f)}$	output fall time	90 % to 10 % output	17	21	25	ns
t_{PD}	propagation delay	50 % input to 50 % output	16	21	26	ns
t_{st}	settling time	50 % input to 100 % ± 2 % output	–	–	200	ns
O_v	overshoot voltage ratio		–	6	–	%

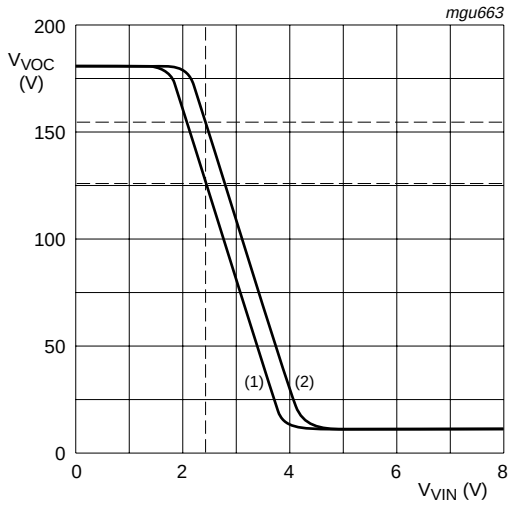
Notes

1. PSRR definition: ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.
2. Timing conditions: f_i < 1 MHz; $t_{i(r)} = t_{i(f)}$ = 15 ns; V_{VOC} = 100 V (p-p) square wave.



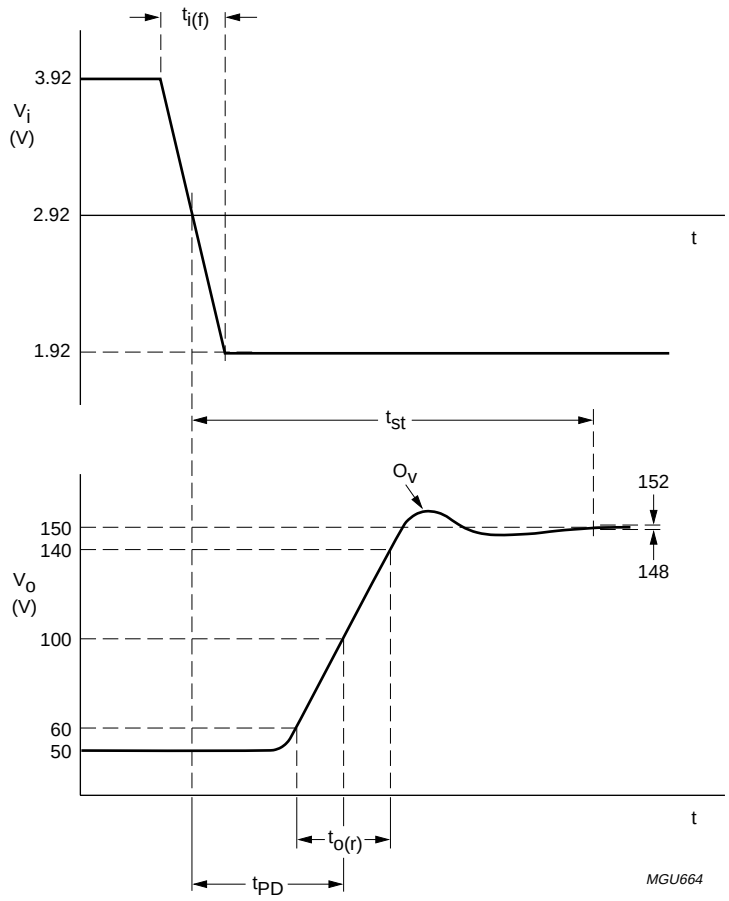
Pin GS connected to ground.
(1) Low black level output (pin BLS connected to ground).
(2) High black level output (pin BLS left open-circuit).

Fig.5 DC-to-DC transfer of input to output with low amplifier gain.



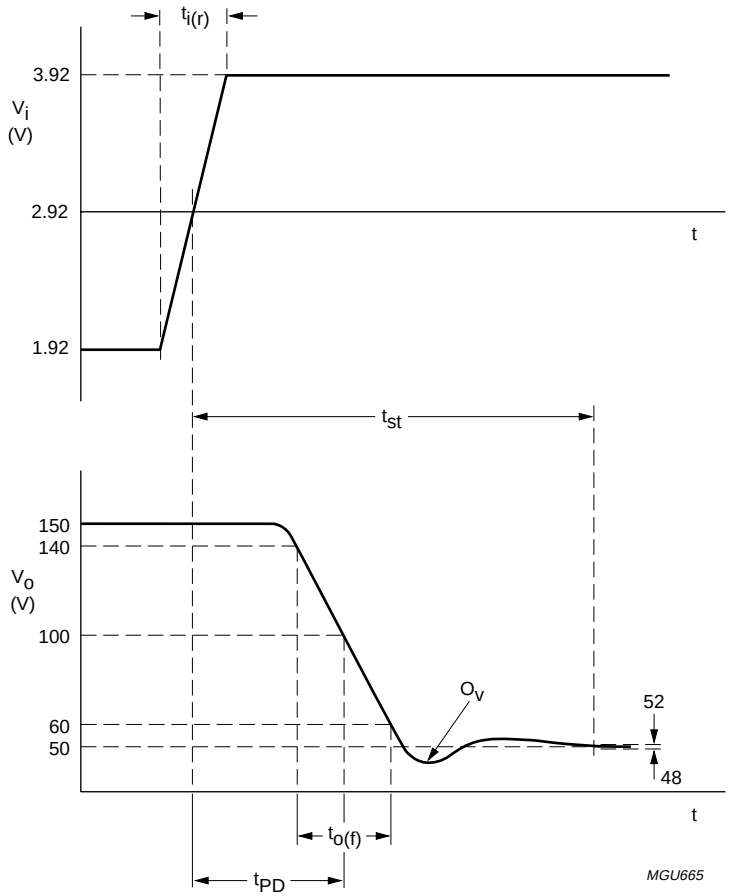
Pin GS left open-circuit.
(1) Low black level output (pin BLS connected to ground).
(2) High black level output (pin BLS left open-circuit).

Fig.6 DC-to-DC transfer of input to output with high amplifier gain.



Low amplifier gain and low black level output.

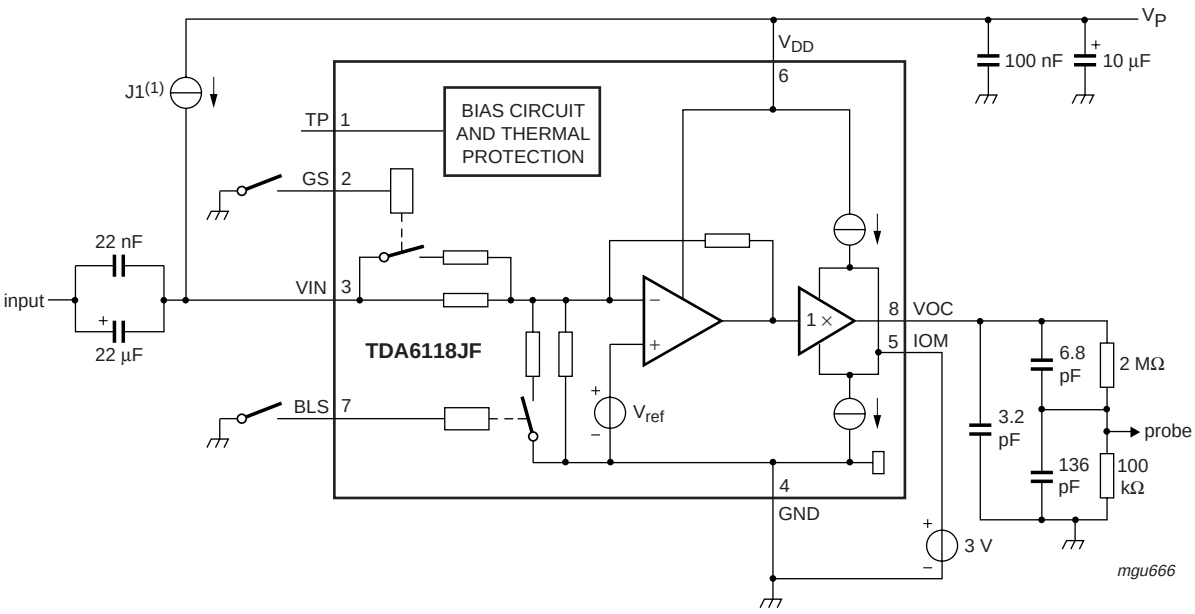
Fig.7 Rising edge of cathode output voltage as a function of AC input.



Low amplifier gain and low black level output.

Fig.8 Falling edge of cathode output voltage as a function of AC input.

APPLICATION AND TEST INFORMATION



(1) Current source J1 is to be tuned so that V_{VOC} is set to 100 V.

Fig.9 Test circuit.

External flashover protection

For sufficient flashover protection it is necessary to apply an external diode for each channel. See application note *"AN01031 (Application note TDA6118JF)"*.

To limit the diode current an external 220 Ω carbon high-voltage resistor in series with the external diode and a 2 kV spark gap are needed (for this resistor value, the CRT has to be connected to the main printed-circuit board).

V_{DD} must be decoupled to ground:

- With a capacitor ≥100 nF with good HF behaviour (e.g. foil); this capacitor must be placed as close as possible to pins V_{DD} and GND but definitely within 5 mm.
- With a capacitor >10 μF on the picture tube base print.

Switch-off behaviour

The switch-off behaviour of the TDA6118JF can be controlled due to the fact that the output pins are still under control of the input pins for low power supply voltages (approximately 30 V and higher).

Bandwidth

The addition of the flash resistor produces a decreased bandwidth and increases the rise and fall times. For further information see application note *"AN01031 (Application note TDA6118JF)"*.

Dissipation

Regarding the dissipation, distinction must be made between the static dissipation (independent of the frequency) and the dynamic dissipation (proportional to the frequency).

The static dissipation of the TDA6118JF is related to the voltage supply current. The static dissipation equals:

$$P_{stat} = V_{DD} \times I_q$$

Where:

V_{DD} = supply voltage

I_q = quiescent supply current.

The dynamic dissipation equals:

$$P_{dyn} = V_{DD} \times (C_L + C_{int}) \times f_i \times V_{VOC} \times \delta$$

Where:

C_L = load capacitance

C_{int} = internal load capacitance (≈ 4 pF)

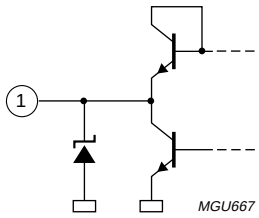
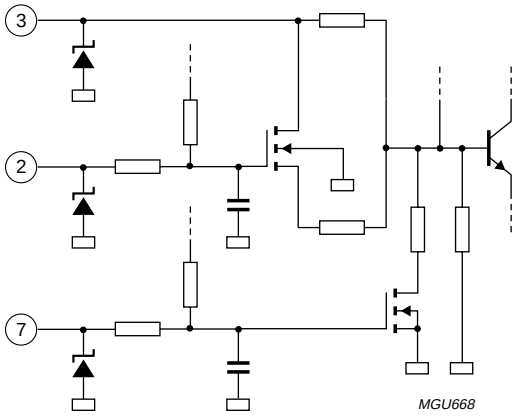
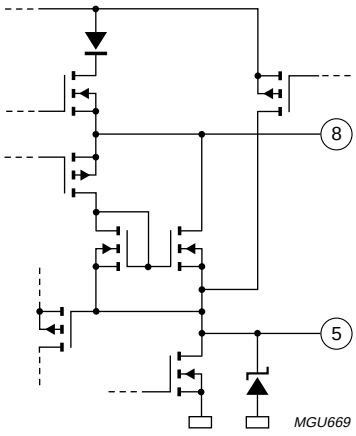
f_i = input frequency

V_{VOC} = output voltage (peak-to-peak value)

δ = non-blanking duty cycle.

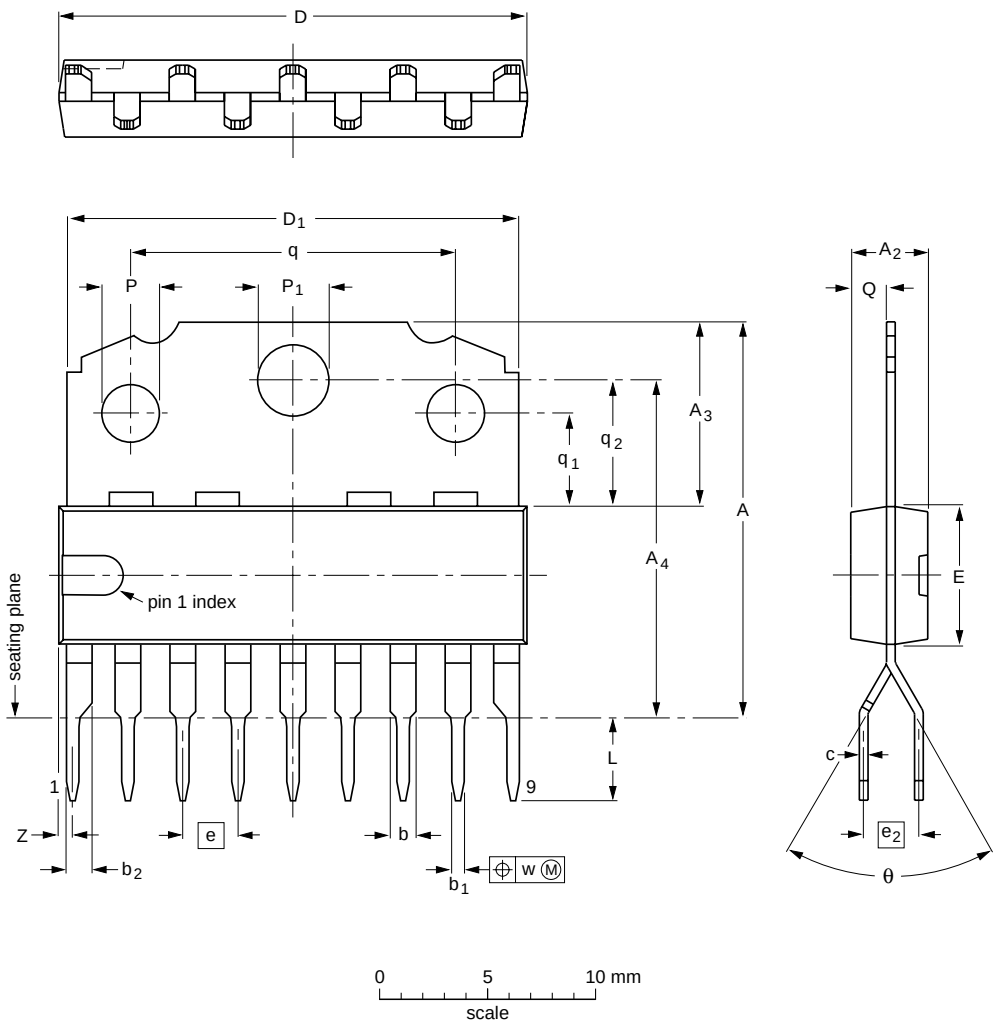
The IC must be mounted on the picture tube base print to minimize the load capacitance C_L.

INTERNAL PIN CONFIGURATION

PIN	SYMBOL	INTERNAL CIRCUIT
1	TP	
3	VIN	
2	GS	
7	BLS	
8	VOC	
5	IOM	
4	GND	connected to substrate
6	V_{DD}	connected to supply
9	n.c.	not connected

PACKAGE OUTLINE

DBS9MPF: plastic DIL-bent-SIL medium power package with fin; 9 leads **SOT111-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	$D^{(1)}$	D_1	$E^{(1)}$	e	e_2	L	P	P_1	Q	q	q_1	q_2	w	$Z^{(1)}$ max.	θ
mm	18.5 17.8	3.7	8.7 8.0	15.5 15.1	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1	65^o 55^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT111-1						~~95-03-11~~ 03-03-12

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
CPGA, HCPGA	–	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	–	not suitable

Notes

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
2. For PMFP packages hot bar soldering or manual soldering is suitable.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

SCA76

Printed in The Netherlands R24/02/pp15 Date of release: 2004 Aug 26 Document order number: 9397 750 13715

Let's make things better.

Philips
Semiconductors