

## 2.7V Dual Channel 12-Bit A/D Converter with SPI™ Serial Interface

### Features

- 12-bit resolution
- $\pm 1$  LSB max DNL
- $\pm 1$  LSB max INL (MCP3202-B)
- $\pm 2$  LSB max INL (MCP3202-C)
- Analog inputs programmable as single-ended or pseudo-differential pairs
- On-chip sample and hold
- SPI™ serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 100 ksp/s max. sampling rate at  $V_{DD} = 5V$
- 50 ksp/s max. sampling rate at  $V_{DD} = 2.7V$
- Low power CMOS technology
  - 500 nA typical standby current, 5  $\mu A$  max.
  - 550  $\mu A$  max. active current at 5V
- Industrial temp range: -40°C to +85°C
- 8-pin MSOP, PDIP, SOIC and TSSOP packages

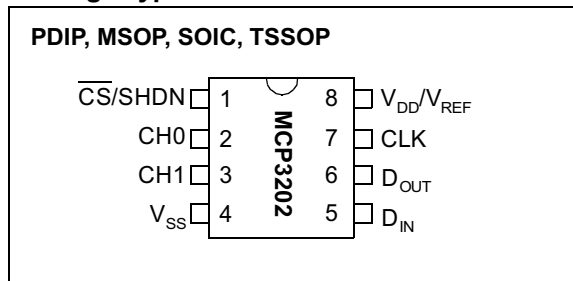
### Applications

- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

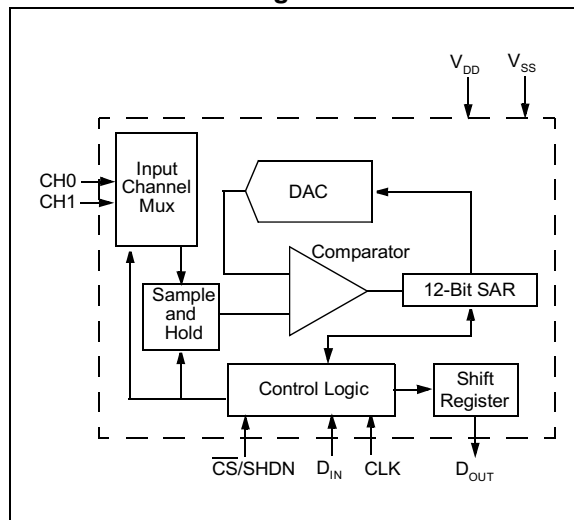
### Description

The Microchip Technology Inc. MCP3202 is a successive approximation 12-bit Analog-to-Digital (A/D) Converter with on-board sample and hold circuitry. The MCP3202 is programmable to provide a single pseudo-differential input pair or dual single-ended inputs. Differential Nonlinearity (DNL) is specified at  $\pm 1$  LSB, and Integral Nonlinearity (INL) is offered in  $\pm 1$  LSB (MCP3202-B) and  $\pm 2$  LSB (MCP3202-C) versions. Communication with the device is done using a simple serial interface compatible with the SPI protocol. The device is capable of conversion rates of up to 100 ksp/s at 5V and 50 ksp/s at 2.7V. The MCP3202 device operates over a broad voltage range (2.7V - 5.5V). Low current design permits operation with typical standby and active currents of only 500 nA and 375  $\mu A$ , respectively. The MCP3202 is offered in 8-pin MSOP, PDIP, TSSOP and 150 mil SOIC packages.

### Package Types



### Functional Block Diagram



# MCP3202

## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Maximum Ratings\*

$V_{DD}$ .....7.0V

All inputs and outputs w.r.t.  $V_{SS}$ ..... -0.6V to  $V_{DD}$  +0.6V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

ESD protection on all pins (HBM)..... > 4 kV

\*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## PIN FUNCTION TABLE

Name	Function
$V_{DD}/V_{REF}$	+2.7V to 5.5V Power Supply and Reference Voltage Input
CH0	Channel 0 Analog Input
CH1	Channel 1 Analog Input
CLK	Serial Clock
$D_{IN}$	Serial Data In
$D_{OUT}$	Serial Data Out
$\overline{CS}/SHDN$	Chip Select/Shutdown Input

## ELECTRICAL CHARACTERISTICS

All parameters apply at  $V_{DD} = 5.5V$ ,  $V_{SS} = 0V$ ,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $f_{SAMPLE} = 100$  ksp/s and  $f_{CLK} = 18 * f_{SAMPLE}$  unless otherwise noted.

Parameter	Sym	Min.	Typ.	Max.	Units	Conditions
<b>Conversion Rate:</b>						
Conversion Time	$t_{CONV}$	—	—	12	clock cycles	
Analog Input Sample Time	$t_{SAMPLE}$	1.5			clock cycles	
Throughput Rate	$f_{SAMPLE}$	—	—	100 50	ksp/s ksp/s	$V_{DD} = V_{REF} = 5V$ $V_{DD} = V_{REF} = 2.7V$
<b>DC Accuracy:</b>						
Resolution		12			bits	
Integral Nonlinearity	INL	—	$\pm 0.75$ $\pm 1$	$\pm 1$ $\pm 2$	LSB LSB	MCP3202-B MCP3202-C
Differential Nonlinearity	DNL	—	$\pm 0.5$	$\pm 1$	LSB	No missing codes over temperature
Offset Error		—	$\pm 1.25$	$\pm 3$	LSB	
Gain Error		—	$\pm 1.25$	$\pm 5$	LSB	
<b>Dynamic Performance:</b>						
Total Harmonic Distortion	THD	—	-82	—	dB	$V_{IN} = 0.1V$ to $4.9V @ 1$ kHz
Signal to Noise and Distortion (SINAD)	SINAD	—	72	—	dB	$V_{IN} = 0.1V$ to $4.9V @ 1$ kHz
Spurious Free Dynamic Range	SFDR	—	86	—	dB	$V_{IN} = 0.1V$ to $4.9V @ 1$ kHz
<b>Analog Inputs:</b>						
Input Voltage Range for CH0 or CH1 in Single-Ended Mode		$V_{SS}$	—	$V_{DD}$	V	
Input Voltage Range for IN+ in Pseudo-Differential Mode	IN+	IN-	—	$V_{DD} + IN-$		See Sections 3.1 and 4.1
Input Voltage Range for IN- in Pseudo-Differential Mode	IN-	$V_{SS} - 100$	—	$V_{SS} + 100$	mV	See Sections 3.1 and 4.1
Leakage Current		—	.001	$\pm 1$	$\mu A$	
Switch Resistance	$R_{SS}$	—	1 k	—	$\Omega$	See Figure 4-1

**Note 1:** This parameter is established by characterization and not 100% tested.

**2:** Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2 for more information.

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

All parameters apply at  $V_{DD} = 5.5V$ ,  $V_{SS} = 0V$ ,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $f_{SAMPLE} = 100$  ksp/s and  $f_{CLK} = 18 \cdot f_{SAMPLE}$  unless otherwise noted.

Parameter	Sym	Min.	Typ.	Max.	Units	Conditions
Sample Capacitor	$C_{SAMPLE}$	—	20	—	pF	See Figure 4-1
<b>Digital Input/Output:</b>						
Data Coding Format		Straight Binary				
High Level Input Voltage	$V_{IH}$	$0.7 V_{DD}$	—	—	V	
Low Level Input Voltage	$V_{IL}$	—	—	$0.3 V_{DD}$	V	
High Level Output Voltage	$V_{OH}$	4.1	—	—	V	$I_{OH} = -1$ mA, $V_{DD} = 4.5V$
Low Level Output Voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 1$ mA, $V_{DD} = 4.5V$
Input Leakage Current	$I_{LI}$	-10	—	10	$\mu A$	$V_{IN} = V_{SS}$ or $V_{DD}$
Output Leakage Current	$I_{LO}$	-10	—	10	$\mu A$	$V_{OUT} = V_{SS}$ or $V_{DD}$
Pin Capacitance (All Inputs/Outputs)	$C_{IN}, C_{OUT}$	—	—	10	pF	$V_{DD} = 5.0V$ (Note 1) $T_{AMB} = 25^{\circ}C$ , $f = 1$ MHz
<b>Timing Parameters:</b>						
Clock Frequency	$f_{CLK}$	—	—	1.8 0.9	MHz MHz	$V_{DD} = 5V$ (Note 2) $V_{DD} = 2.7V$ (Note 2)
Clock High Time	$t_{HI}$	250	—	—	ns	
Clock Low Time	$t_{LO}$	250	—	—	ns	
CS Fall To First Rising CLK Edge	$t_{SUCS}$	100	—	—	ns	
Data Input Setup Time	$t_{SU}$	—	—	50	ns	
Data Input Hold Time	$t_{HD}$	—	—	50	ns	
CLK Fall To Output Data Valid	$t_{DO}$	—	—	200	ns	See Test Circuits, Figure 1-2
CLK Fall To Output Enable	$t_{EN}$	—	—	200	ns	See Test Circuits, Figure 1-2
CS Rise To Output Disable	$t_{DIS}$	—	—	100	ns	See Test Circuits, Figure 1-2 <b>Note 1</b>
CS Disable Time	$t_{CSH}$	500	—	—	ns	
$D_{OUT}$ Rise Time	$t_R$	—	—	100	ns	See Test Circuits, Figure 1-2 <b>Note 1</b>
$D_{OUT}$ Fall Time	$t_F$	—	—	100	ns	See Test Circuits, Figure 1-2 <b>Note 1</b>
<b>Power Requirements:</b>						
Operating Voltage	$V_{DD}$	2.7	—	5.5	V	
Operating Current	$I_{DD}$	—	375	550	$\mu A$	$V_{DD} = 5.0V$ , $D_{OUT}$ unloaded
Standby Current	$I_{DDs}$	—	0.5	5	$\mu A$	$CS = V_{DD} = 5.0V$
<b>Temperature Ranges:</b>						
Specified Temperature Range	$T_A$	-40	—	+85	$^{\circ}C$	
Operating Temperature Range	$T_A$	-40	—	+85	$^{\circ}C$	
Storage Temperature Range	$T_A$	-65	—	+150	$^{\circ}C$	
<b>Thermal Package Resistance:</b>						
Thermal Resistance, 8L-PDIP	$\theta_{JA}$	—	85	—	$^{\circ}C/W$	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	163	—	$^{\circ}C/W$	
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	206	—	$^{\circ}C/W$	
Thermal Resistance, 8L-TSSOP	$\theta_{JA}$	—	—	—	$^{\circ}C/W$	

**Note 1:** This parameter is established by characterization and not 100% tested.

**2:** Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2 for more information.

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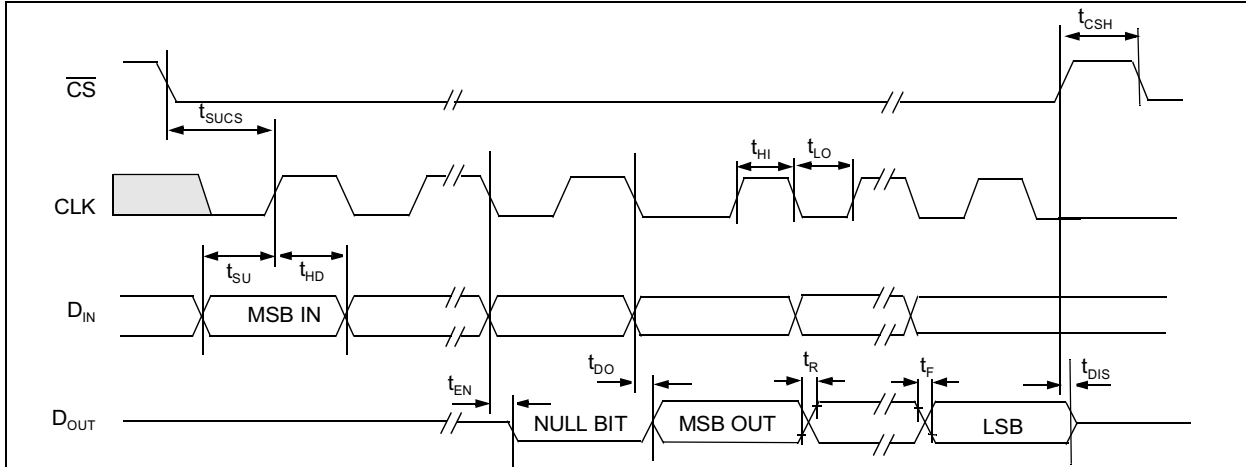


FIGURE 1-1: Serial Timing.

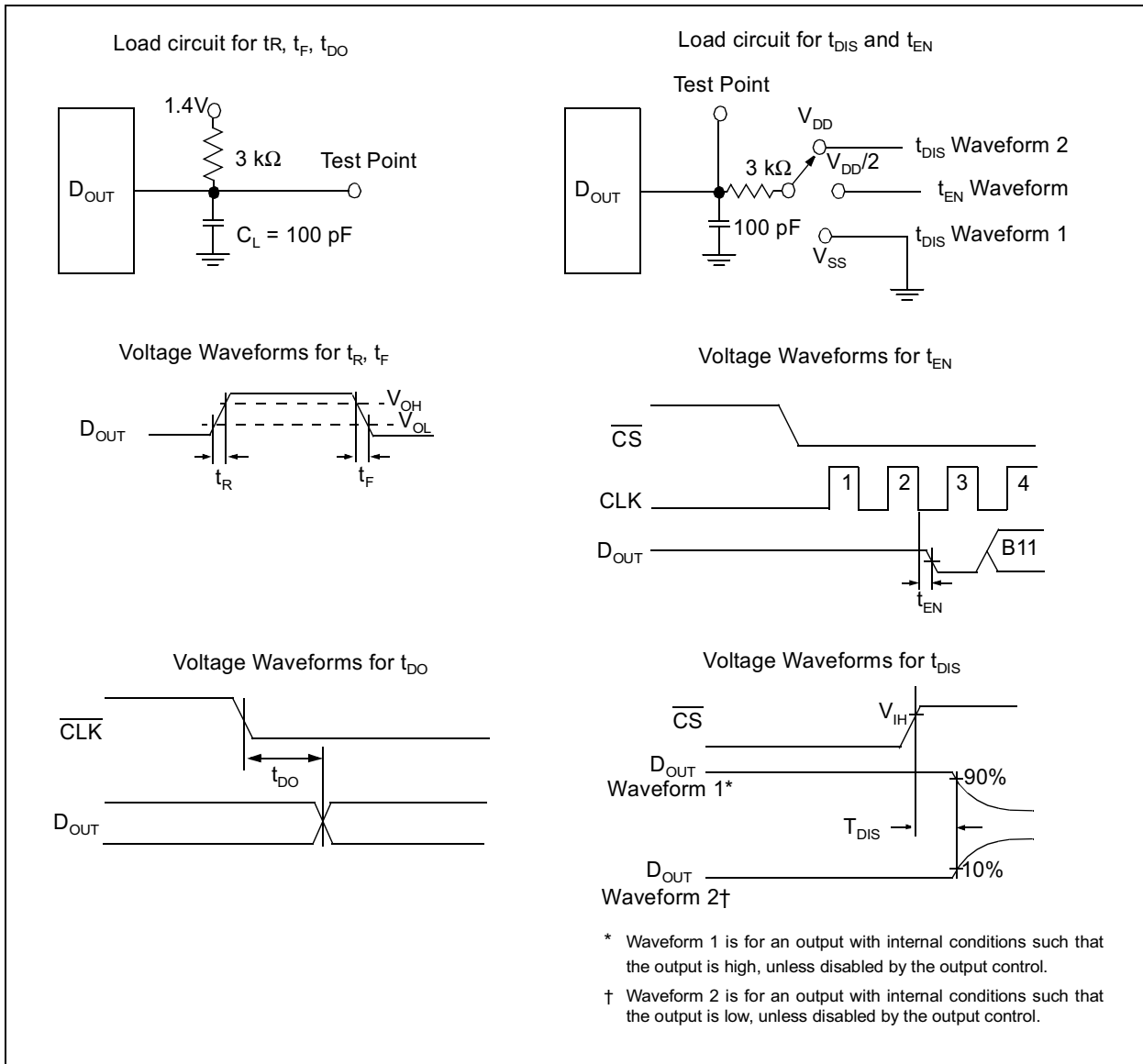
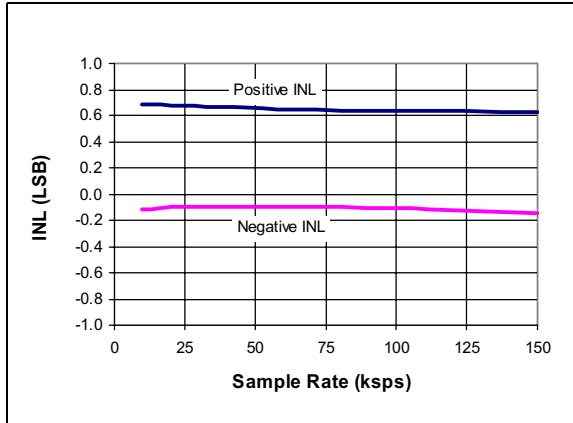


FIGURE 1-2: Test Circuits.

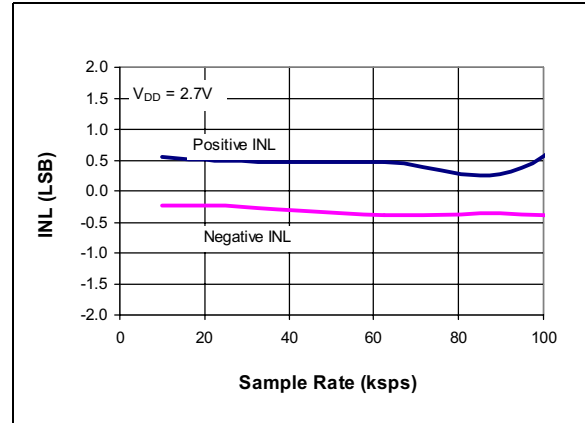
## 2.0 TYPICAL PERFORMANCE CHARACTERISTICS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

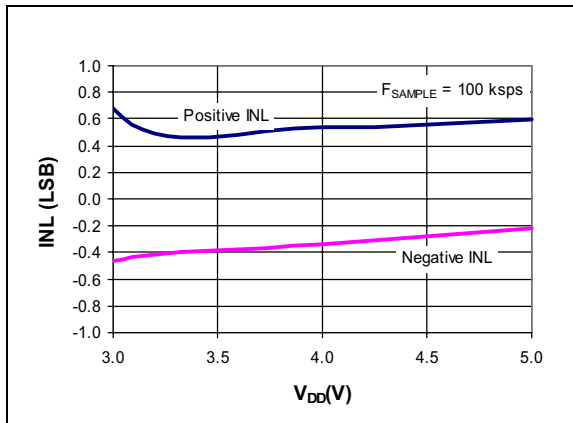
**Note:** Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  kpsps,  $f_{CLK} = 18 * f_{SAMPLE}$ ,  $T_A = 25^{\circ}C$



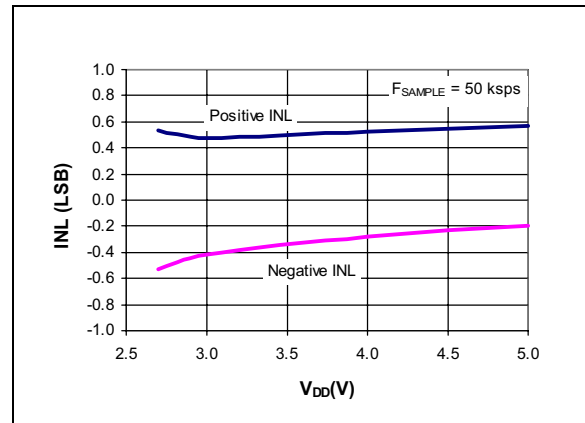
**FIGURE 2-1:** Integral Nonlinearity (INL) vs. Sample Rate.



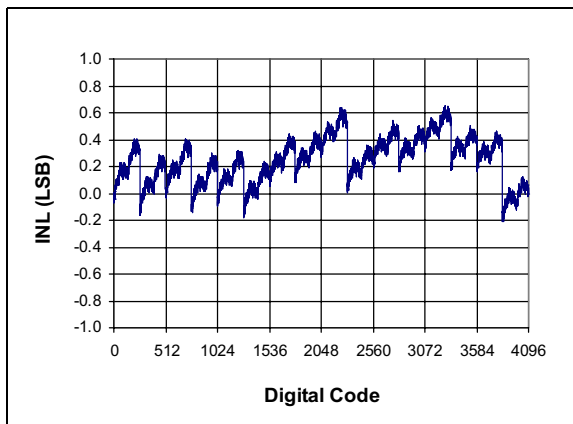
**FIGURE 2-4:** Integral Nonlinearity (INL) vs. Sample Rate ( $V_{DD} = 2.7V$ ).



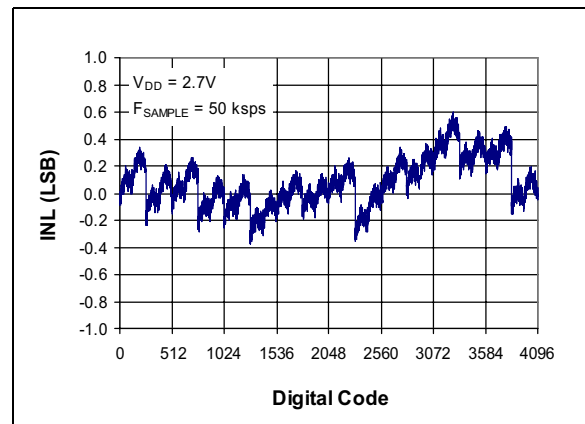
**FIGURE 2-2:** Integral Nonlinearity (INL) vs.  $V_{DD}$ .



**FIGURE 2-5:** Integral Nonlinearity (INL) vs.  $V_{DD}$ .



**FIGURE 2-3:** Integral Nonlinearity (INL) vs. Code (Representative Part).



**FIGURE 2-6:** Integral Nonlinearity (INL) vs. Code (Representative Part,  $V_{DD} = 2.7V$ ).

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Note: Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  ksp/s,  $f_{CLK} = 18 * f_{SAMPLE}$ ,  $T_A = 25^{\circ}C$

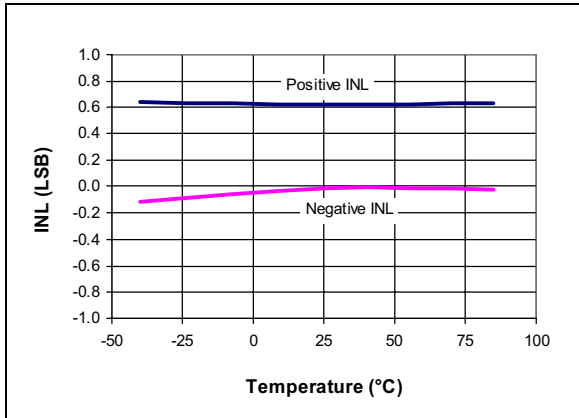


FIGURE 2-7: Integral Nonlinearity (INL) vs. Temperature.

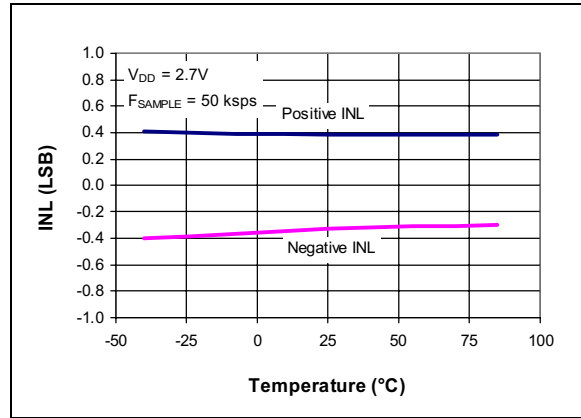


FIGURE 2-10: Integral Nonlinearity (INL) vs. Temperature ( $V_{DD} = 2.7V$ ).

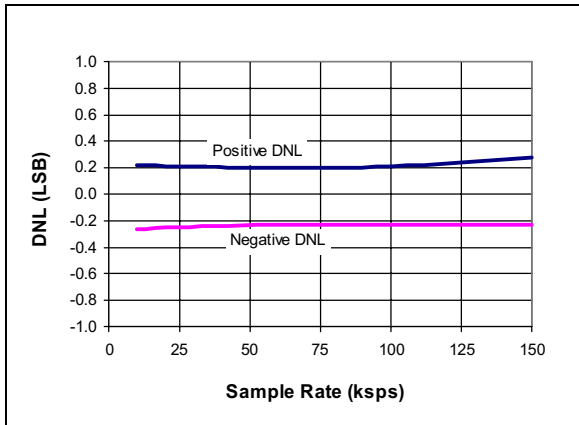


FIGURE 2-8: Differential Nonlinearity (DNL) vs. Sample Rate.

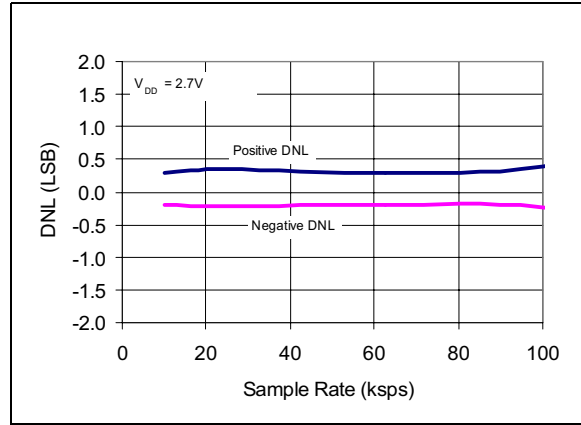


FIGURE 2-11: Differential Nonlinearity (DNL) vs. Sample Rate ( $V_{DD} = 2.7V$ ).

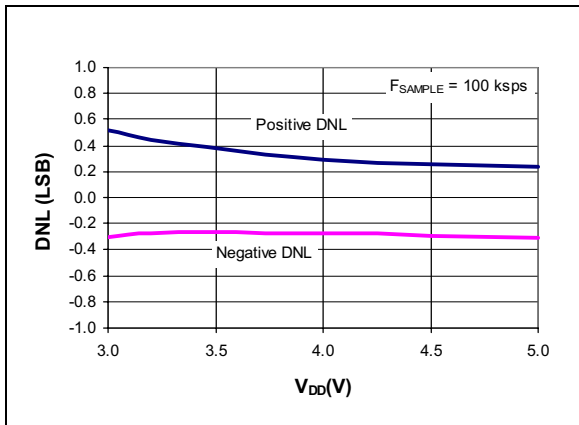


FIGURE 2-9: Differential Nonlinearity (DNL) vs.  $V_{DD}$ .

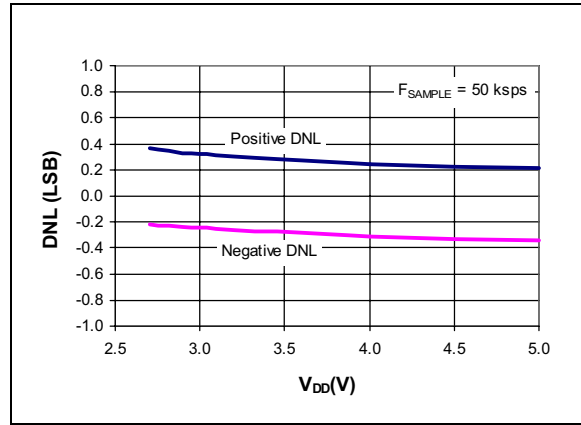
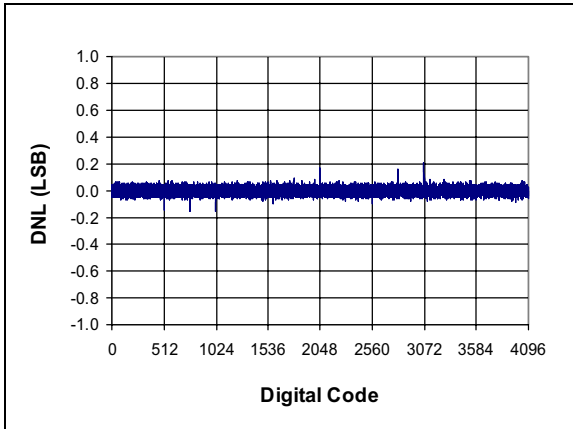
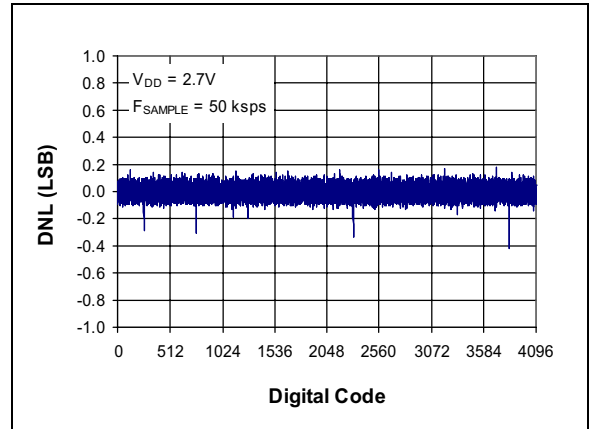


FIGURE 2-12: Differential Nonlinearity (DNL) vs.  $V_{DD}$ .

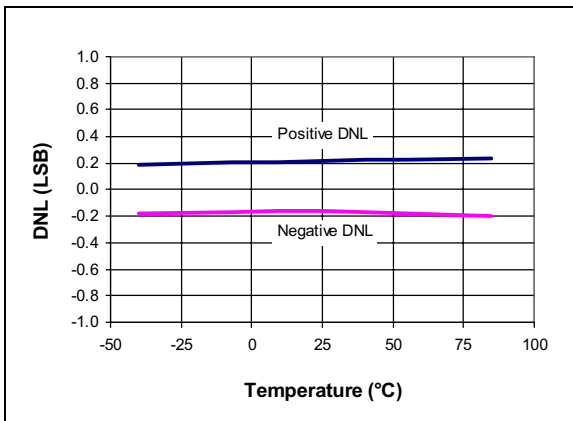
**Note:** Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  ksp/s,  $f_{CLK} = 18 * f_{SAMPLE}$ ,  $T_A = 25^{\circ}C$



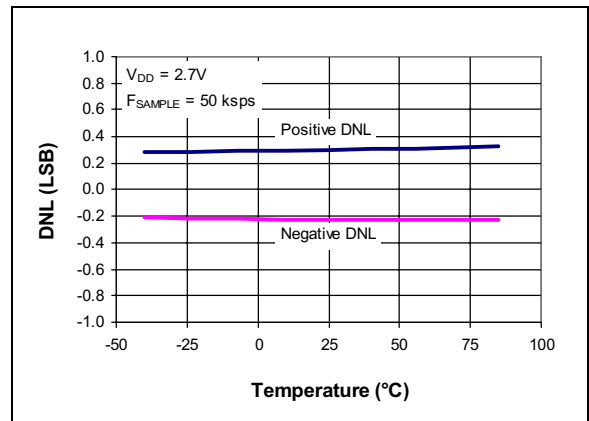
**FIGURE 2-13:** Differential Nonlinearity (DNL) vs. Code (Representative Part).



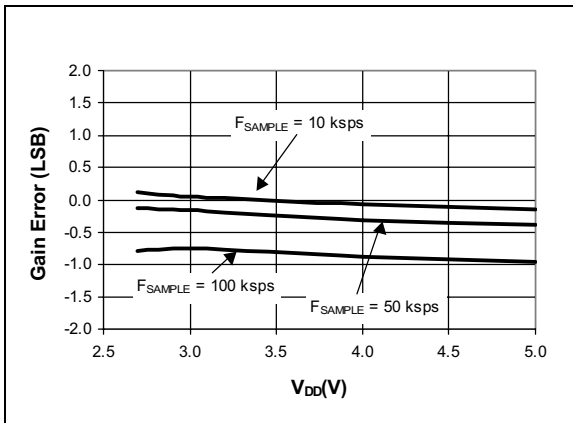
**FIGURE 2-16:** Differential Nonlinearity (DNL) vs. Code (Representative Part,  $V_{DD} = 2.7V$ ).



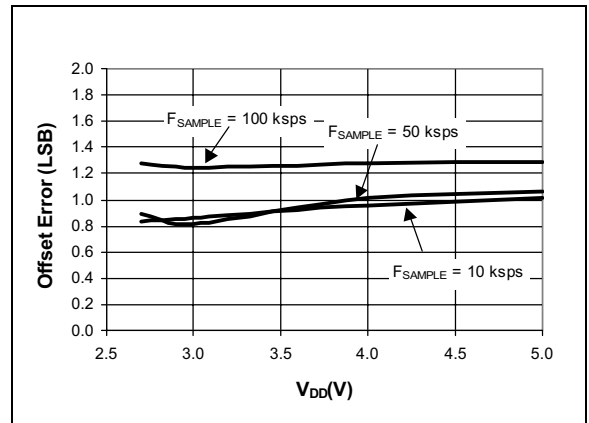
**FIGURE 2-14:** Differential Nonlinearity (DNL) vs. Temperature.



**FIGURE 2-17:** Differential Nonlinearity (DNL) vs. Temperature ( $V_{DD} = 2.7V$ ).



**FIGURE 2-15:** Gain Error vs.  $V_{DD}$ .



**FIGURE 2-18:** Offset Error vs.  $V_{DD}$ .

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Note: Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  ksp/s,  $f_{CLK} = 18 * f_{SAMPLE}$ ,  $T_A = 25^{\circ}C$

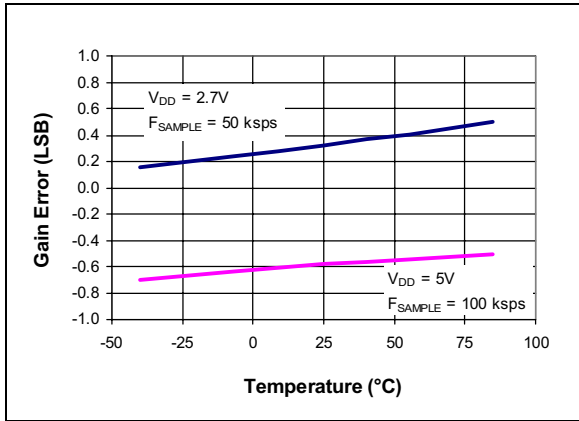


FIGURE 2-19: Gain Error vs. Temperature.

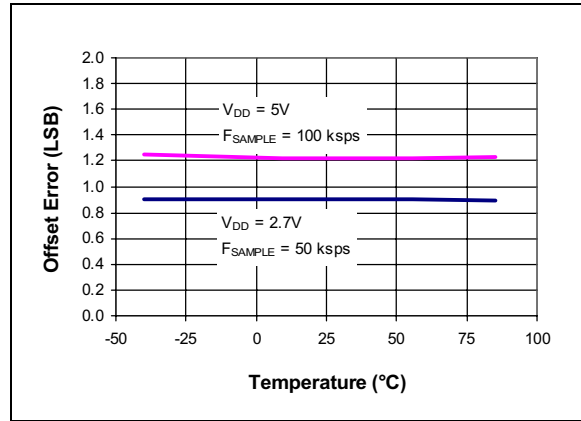


FIGURE 2-22: Offset Error vs. Temperature.

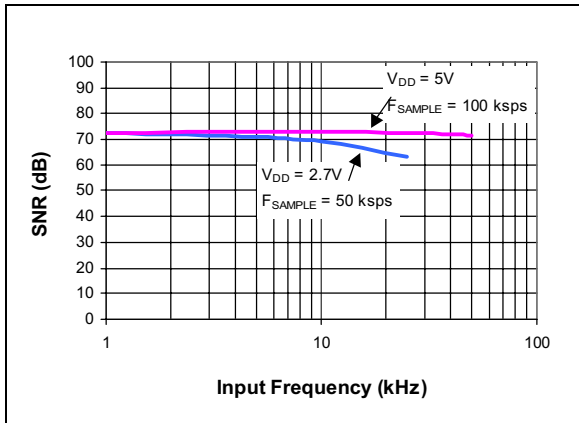


FIGURE 2-20: Signal to Noise Ratio (SNR) vs. Input Frequency.

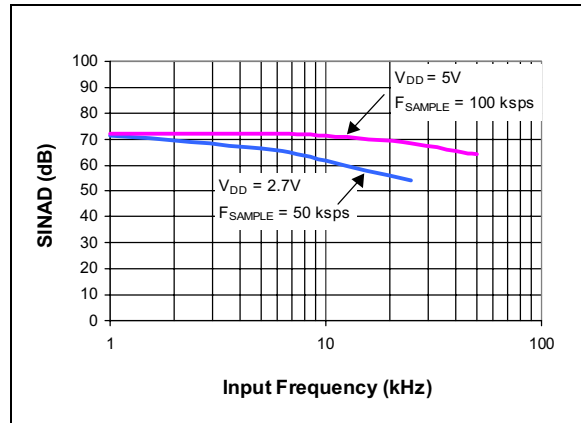


FIGURE 2-23: Signal to Noise and Distortion (SINAD) vs. Input Frequency.

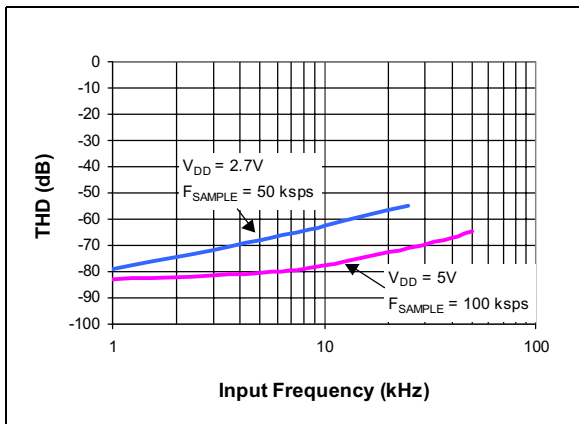


FIGURE 2-21: Total Harmonic Distortion (THD) vs. Input Frequency.

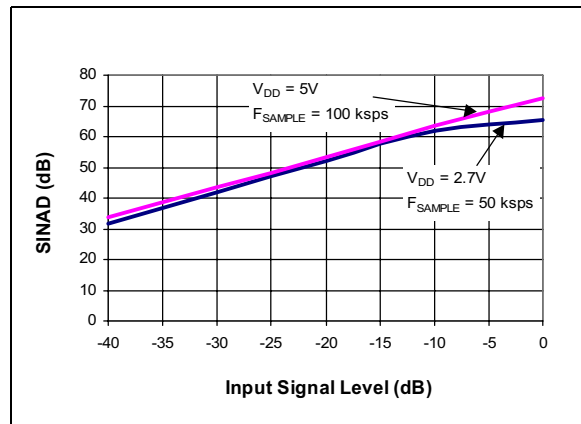
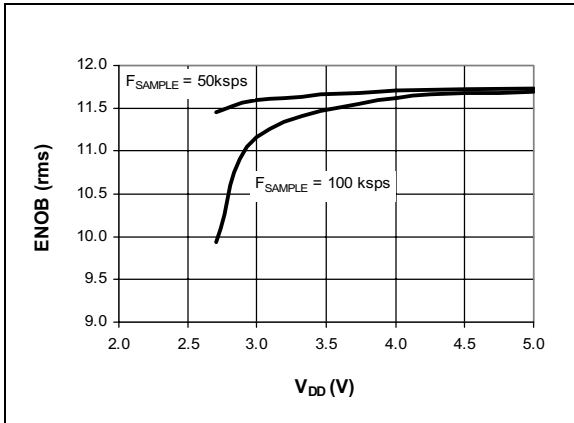


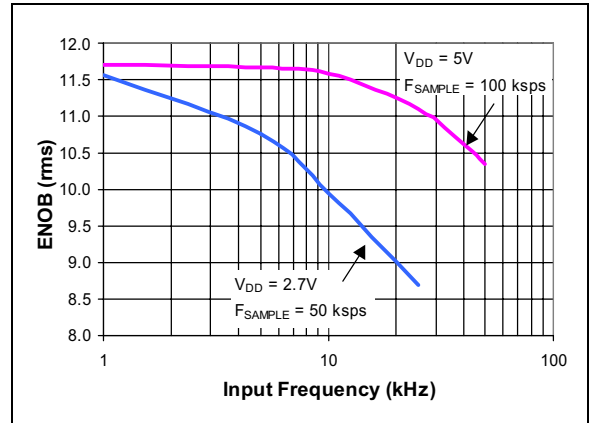
FIGURE 2-24: Signal to Noise and Distortion (SINAD) vs. Signal Level.



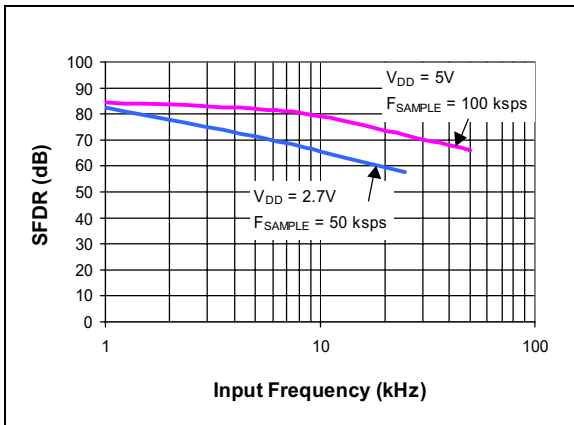
**Note:** Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  ksp/s,  $f_{CLK} = 18 \cdot f_{SAMPLE}$ ,  $T_A = 25^\circ C$



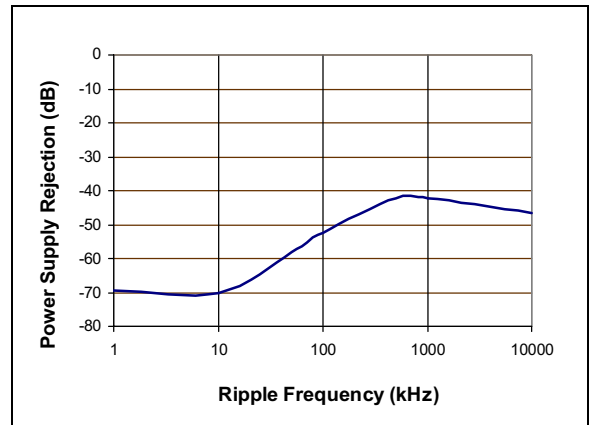
**FIGURE 2-25:** Effective Number of Bits (ENOB) vs.  $V_{DD}$ .



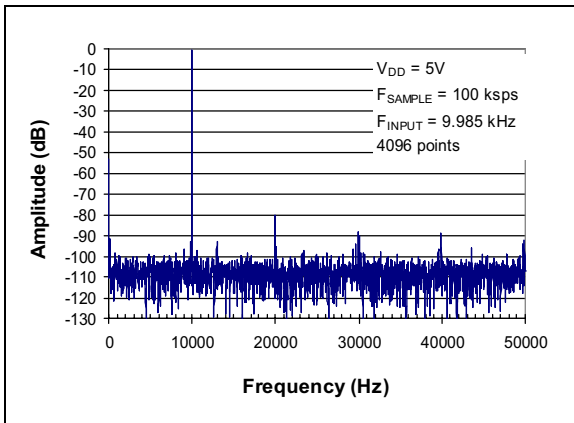
**FIGURE 2-28:** Effective Number of Bits (ENOB) vs. Input Frequency.



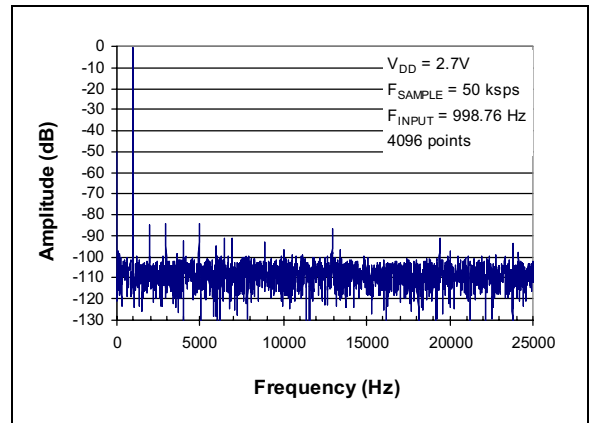
**FIGURE 2-26:** Spurious Free Dynamic Range (SFDR) vs. Input Frequency.



**FIGURE 2-29:** Power Supply Rejection (PSR) vs. Ripple Frequency.



**FIGURE 2-27:** Frequency Spectrum of 10 kHz input (Representative Part).



**FIGURE 2-30:** Frequency Spectrum of 1 kHz input (Representative Part,  $V_{DD} = 2.7V$ ).

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Note: Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  ksp/s,  $f_{CLK} = 18 * f_{SAMPLE}$ ,  $T_A = 25^{\circ}C$

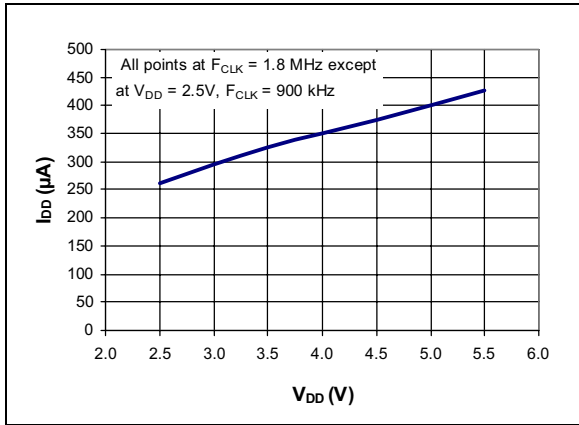


FIGURE 2-31:  $I_{DD}$  vs.  $V_{DD}$ .

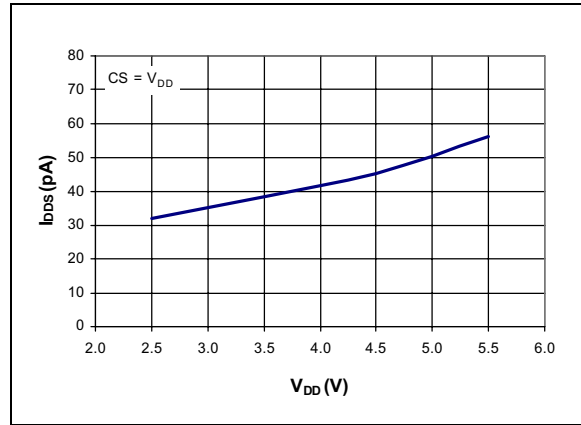


FIGURE 2-34:  $I_{DDS}$  vs.  $V_{DD}$ .

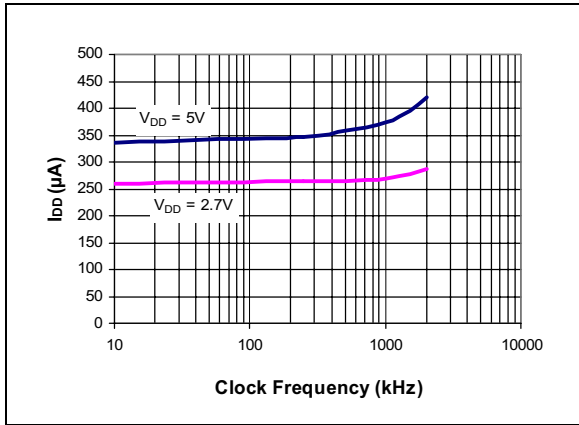


FIGURE 2-32:  $I_{DD}$  vs. Clock Frequency.

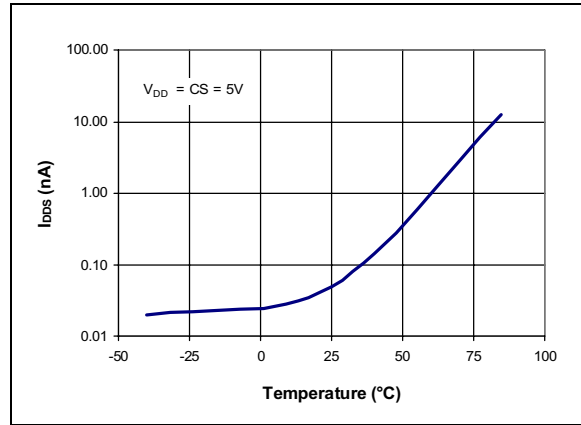


FIGURE 2-35:  $I_{DDS}$  vs. Temperature.

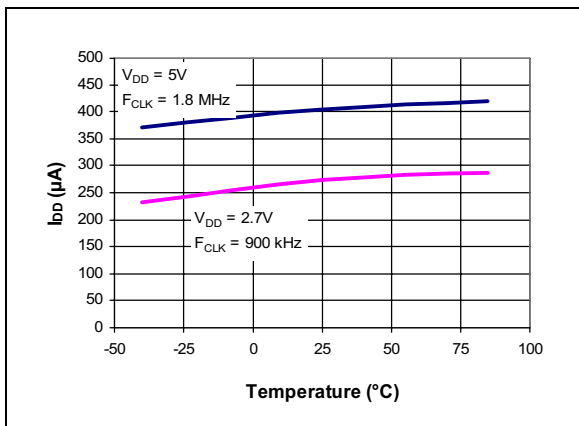


FIGURE 2-33:  $I_{DD}$  vs. Temperature.

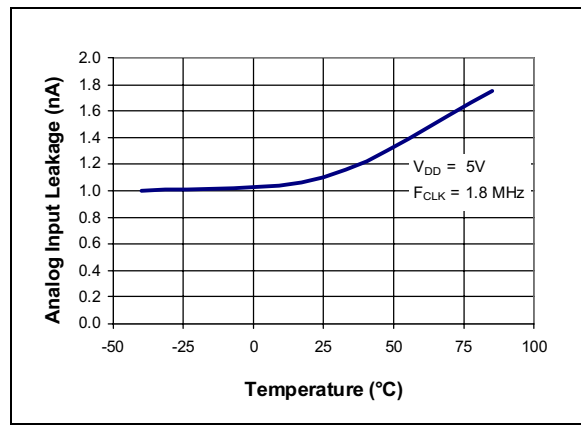


FIGURE 2-36: Analog Input leakage current vs. Temperature.

## 3.0 PIN DESCRIPTIONS

### 3.1 CH0/CH1

Analog inputs for channels 0 and 1 respectively. These channels can be programmed to be used as two independent channels in single ended-mode or as a single pseudo-differential input where one channel is IN+ and one channel is IN-. See Section 5.0 for information on programming the channel configuration.

### 3.2 Chip Select/Shutdown ( $\overline{\text{CS}}/\text{SHDN}$ )

The  $\overline{\text{CS}}/\text{SHDN}$  pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The  $\overline{\text{CS}}/\text{SHDN}$  pin must be pulled high between conversions.

### 3.3 Serial Clock (CLK)

The SPI clock pin is used to initiate a conversion and to clock out each bit of the conversion as it takes place. See Section 6.2 for constraints on clock speed.

### 3.4 Serial Data Input (DIN)

The SPI port serial data input pin is used to clock in input channel configuration data.

### 3.5 Serial Data Output (DOUT)

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

## 4.0 DEVICE OPERATION

The MCP3202 A/D Converter employs a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the second rising edge of the serial clock after the start bit has been received. Following this sample time, the input switch of the converter opens and the device uses the collected charge on the internal sample and hold capacitor to produce a serial 12-bit digital output code. Conversion rates of 100 ksp/s are possible on the MCP3202. See Section 6.2 for information on minimum clock rates. Communication with the device is done using a 3-wire SPI-compatible interface.

## 4.1 Analog Inputs

The MCP3202 device offers the choice of using the analog input channels configured as two single-ended inputs or a single pseudo-differential input. Configuration is done as part of the serial command before each conversion begins. When used in the pseudo-differential mode, CH0 and CH1 are programmed as the IN+ and IN- inputs as part of the command string transmitted to the device. The IN+ input can range from IN- to  $V_{\text{REF}}$  ( $V_{\text{DD}} + \text{IN-}$ ). The IN- input is limited to  $\pm 100$  mV from the  $V_{\text{SS}}$  rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

For the A/D Converter to meet specification, the charge holding capacitor ( $C_{\text{SAMPLE}}$ ) must be given enough time to acquire a 12-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

In this diagram, it is shown that the source impedance ( $R_{\text{S}}$ ) adds to the internal sampling switch ( $R_{\text{SS}}$ ) impedance, directly affecting the time that is required to charge the capacitor,  $C_{\text{SAMPLE}}$ . Consequently, larger source impedances increase the offset, gain, and integral linearity errors of the conversion.

Ideally, the impedance of the signal source should be near zero. This is achievable with an operational amplifier such as the MCP601 which has a closed loop output impedance of tens of ohms. The adverse effects of higher source impedances are shown in Figure 4-2.

When operating in the pseudo-differential mode, if the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than  $\{[V_{\text{DD}} + (\text{IN-})] - 1 \text{ LSB}\}$ , then the output code will be FFFh. If the voltage level at IN- is more than 1 LSB below  $V_{\text{SS}}$ , then the voltage level at the IN+ input will have to go below  $V_{\text{SS}}$  to see the 000h output code. Conversely, if IN- is more than 1 LSB above  $V_{\text{SS}}$ , then the FFFh code will not be seen unless the IN+ input level goes above  $V_{\text{DD}}$  level.

## 4.2 Digital Output Code

The digital output code produced by an A/D Converter is a function of the input signal and the reference voltage. For the MCP3202,  $V_{\text{DD}}$  is used as the reference voltage. As the  $V_{\text{DD}}$  level is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D Converter is shown below.

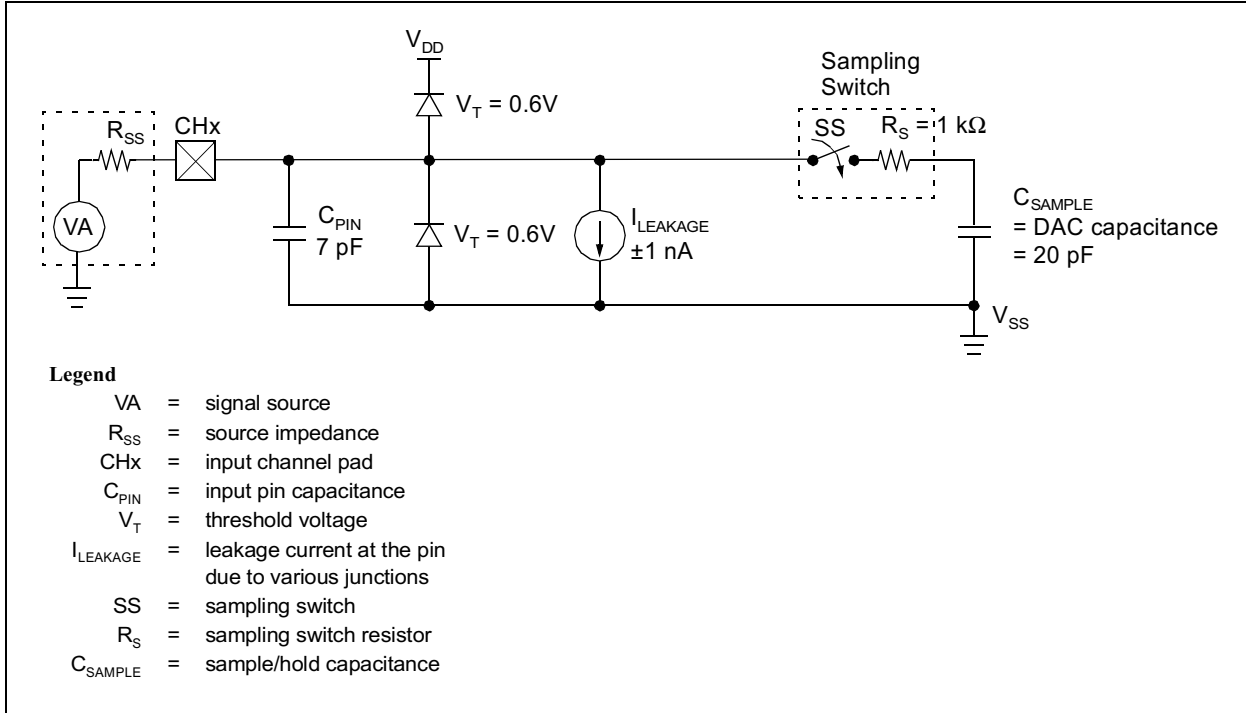
$$\text{Digital Output Code} = \frac{4096 \cdot V_{\text{IN}}}{V_{\text{DD}}}$$

where:

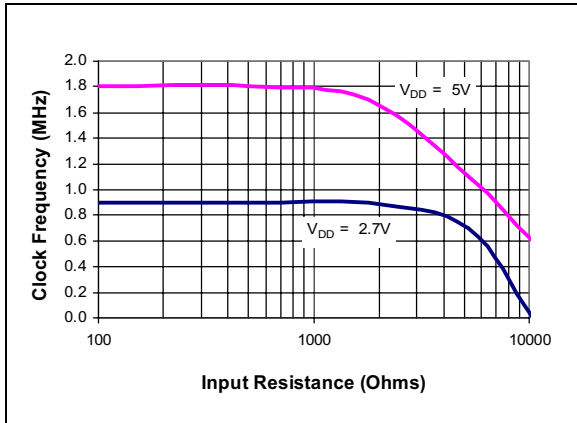
$V_{\text{IN}}$  = analog input voltage

$V_{\text{DD}}$  = supply voltage

# MCP3202



**FIGURE 4-1:** Analog Input Model.



**FIGURE 4-2:** Maximum Clock Frequency vs. Input Resistance ( $R_S$ ) to maintain less than a 0.1 LSB deviation in INL from nominal conditions.

## 5.0 SERIAL COMMUNICATIONS

### 5.1 Overview

Communication with the MCP3202 is done using a standard SPI-compatible serial interface. Initiating communication with the device is done by bringing the  $\overline{CS}$  line low. See Figure 5-1. If the device was powered up with the  $\overline{CS}$  pin low, it must be brought high and back low to initiate communication. The first clock received with  $\overline{CS}$  low and  $D_{IN}$  high will constitute a start bit. The SGL/DIFF bit and the ODD/SIGN bit follow the start bit and are used to select the input channel configuration. The SGL/DIFF is used to select single ended or pseudo-differential mode. The ODD/SIGN bit selects which channel is used in single ended mode, and is used to determine polarity in pseudo-differential mode. Following the ODD/SIGN bit, the MSBF bit is transmitted to and is used to enable the LSB first format for the device. If the MSBF bit is high, then the data will come from the device in MSB first format and any further clocks with  $\overline{CS}$  low will cause the device to output zeros. If the MSBF bit is low, then the device will output the converted word LSB first after the word has been transmitted in the MSB first format. See Figure 5-2. Table 5-1 shows the configuration bits for the MCP3202. The device will begin to sample the analog input on the second rising edge of the clock, after the start bit has been received. The sample period will end on the falling edge of the third clock following the start bit.

On the falling edge of the clock for the MSBF bit, the device will output a low null bit. The next sequential 12 clocks will output the result of the conversion with MSB first as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 12 data bits have been transmitted and the device continues to receive clocks while the  $\overline{CS}$  is held low, (and MSBF = 1), the device will output the conversion result LSB first as shown in Figure 5-2. If more clocks are provided to the device while  $\overline{CS}$  is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If necessary, it is possible to bring  $\overline{CS}$  low and clock in leading zeros on the  $D_{IN}$  line before the start bit. This is often done when dealing with microcontroller-based SPI ports that must send 8 bits at a time. Refer to Section 6.1 for more details on using the MCP3202 devices with hardware SPI ports.

	Config Bits		Channel Selection		GND
	Sgl/Diff	Odd/sign	0	1	
Single Ended Mode	1	0	+	-	-
	1	1	-	+	-
Pseudo-Differential Mode	0	0	IN+	IN-	
	0	1	IN-	IN+	

TABLE 5-1: Configuration Bits for the MCP3202.

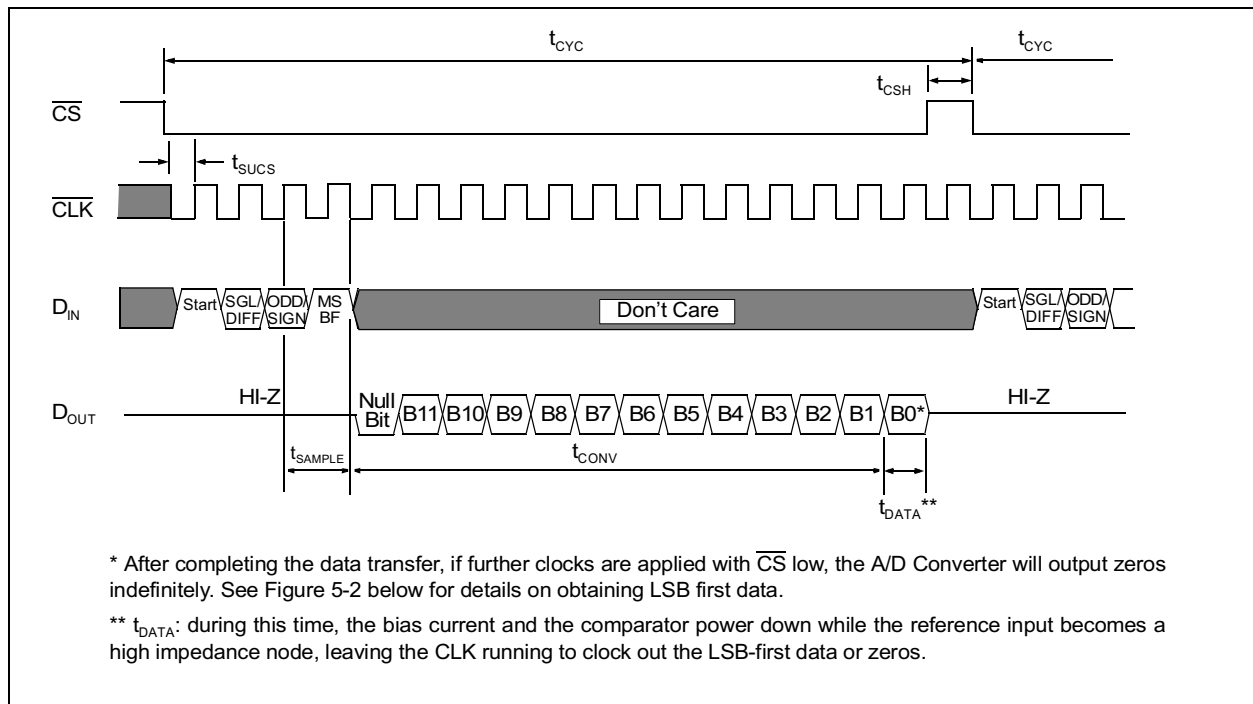


FIGURE 5-1: Communication with the MCP3202 using MSB first format only.

# MCP3202

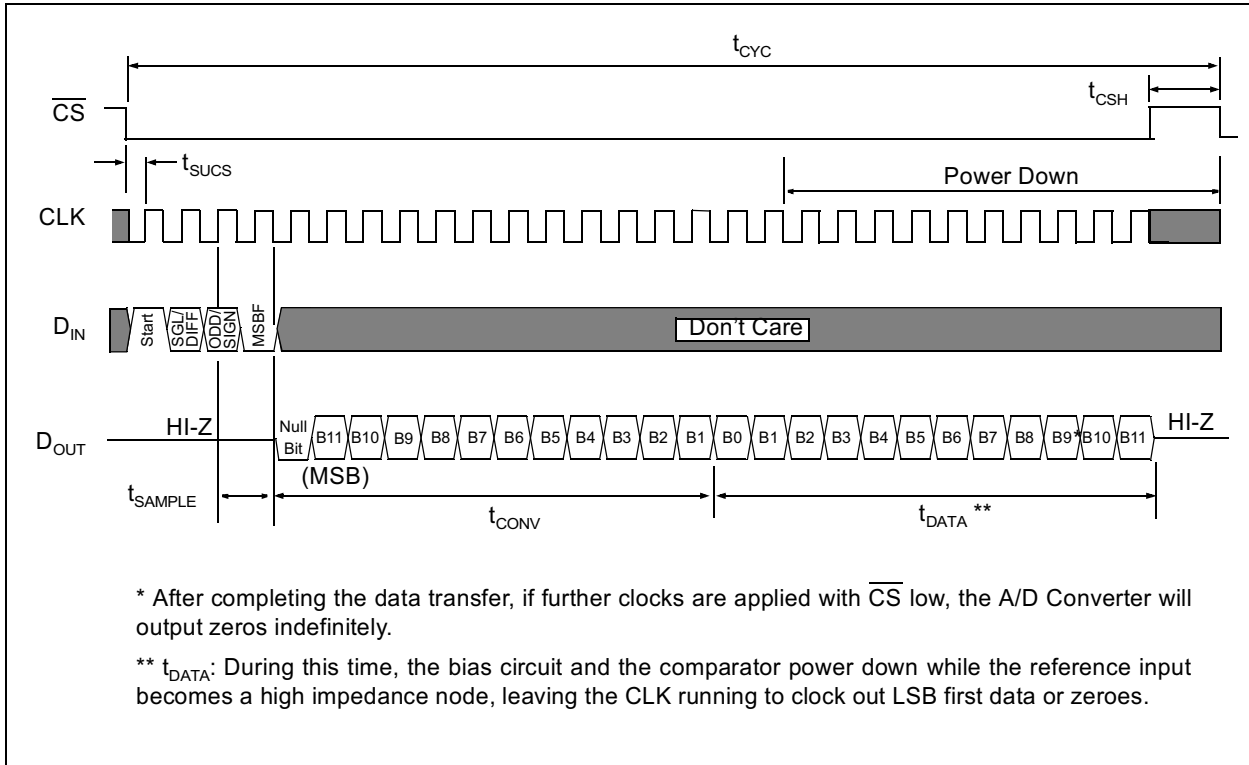


FIGURE 5-2: Communication with MCP3202 using LSB first format.

## 6.0 APPLICATIONS INFORMATION

### 6.1 Using the MCP3202 with Microcontroller (MCU) SPI Ports

With most microcontroller SPI ports, it is required to send groups of eight bits. It is also required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge. Depending on how communication routines are used, it is very possible that the number of clocks required for communication will not be a multiple of eight. Therefore, it may be necessary for the MCU to send more clocks than are actually required. This is usually done by sending 'leading zeros' before the start bit, which are ignored by the device. As an example, Figure 6-1 and Figure 6-2 show how the MCP3202 can be interfaced to a MCU with a hardware SPI port. Figure 6-1 depicts the operation shown in SPI Mode 0,0, which requires that the SCLK from the MCU idles

in the 'low' state, while Figure 6-2 shows the similar case of SPI Mode 1,1 where the clock idles in the 'high' state.

As shown in Figure 6-1, the first byte transmitted to the A/D Converter contains seven leading zeros before the start bit. Arranging the leading zeros this way produces the output 12 bits to fall in positions easily manipulated by the MCU. The MSB is clocked out of the A/D Converter on the falling edge of clock number 12. After the second eight clocks have been sent to the device, the MCU receive buffer will contain three unknown bits (the output is at high impedance until the null bit is clocked out), the null bit and the highest order four bits of the conversion. After the third byte has been sent to the device, the receive register will contain the lowest order eight bits of the conversion results. Easier manipulation of the converted data can be obtained by using this method.

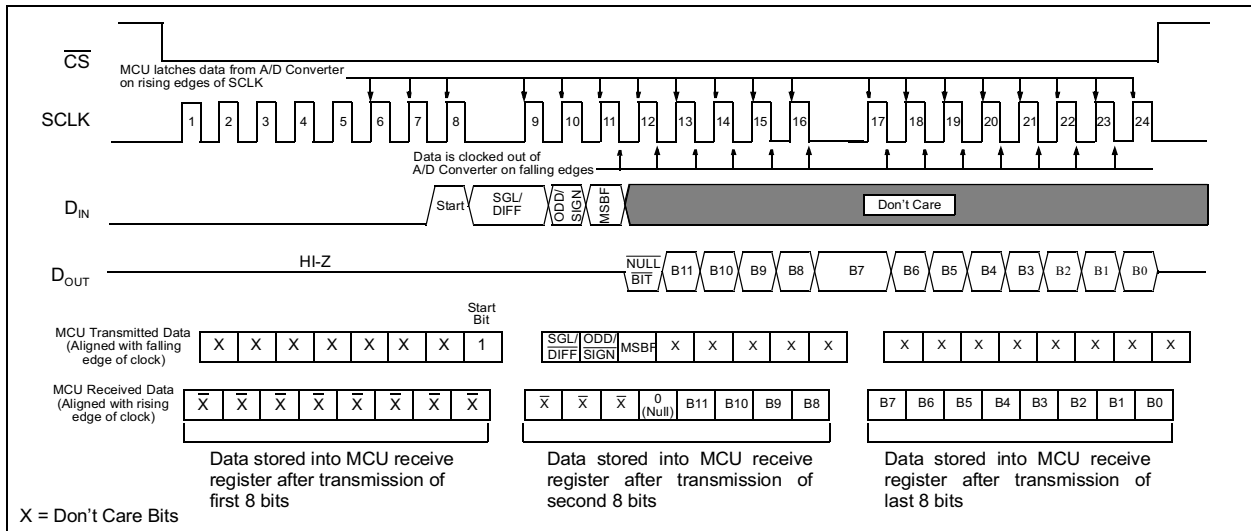


FIGURE 6-1: SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).

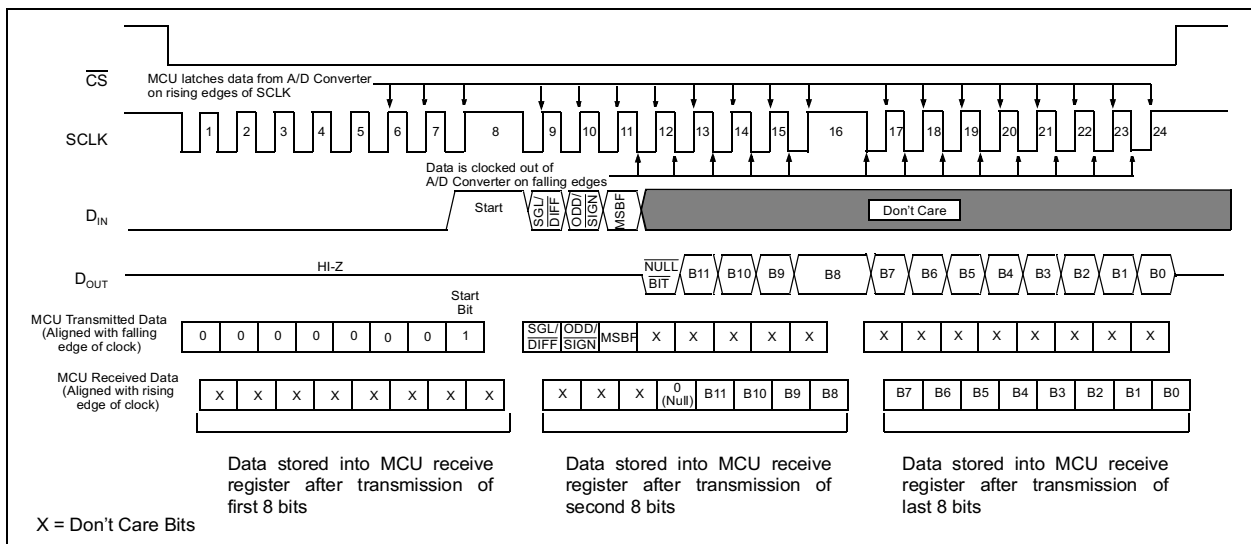


FIGURE 6-2: SPI Communication using 8-bit segments (Mode 1,1: SCLK idles high).

# MCP3202

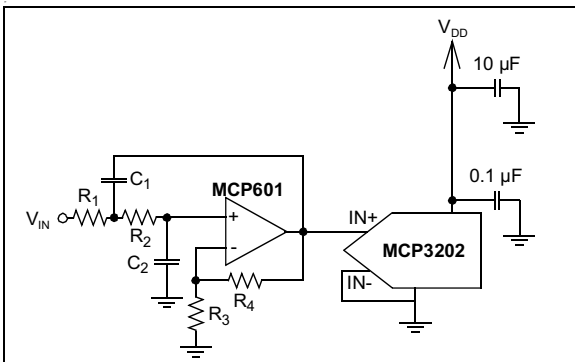
## 6.2 Maintaining Minimum Clock Speed

When the MCP3202 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample cap while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample capacitor for at least 1.2 ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 12 data bits have been clocked out must not exceed 1.2 ms (effective clock frequency of 10 kHz). Failure to meet this criteria may induce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D Converter does not require a constant clock speed or duty cycle, as long as all timing specifications are met.

## 6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D Converter is not a low impedance source, it will have to be buffered or inaccurate conversion results may occur. It is also recommended that a filter be used to eliminate any signals that may be aliased back into the conversion results. This is illustrated in Figure 6-3 below where an op amp is used to drive the analog input of the MCP3202. This amplifier provides a low impedance output for the converter input and a low pass filter, which eliminates unwanted high frequency noise.

Low pass (anti-aliasing) filters can be designed using Microchip's interactive FilterLab™ software. FilterLab will calculate capacitor and resistor values, as well as, determine the number of poles that are required for the application. For more information on filtering signals, see the application note AN699 "Anti-Aliasing Analog Filters for Data Acquisition Systems."



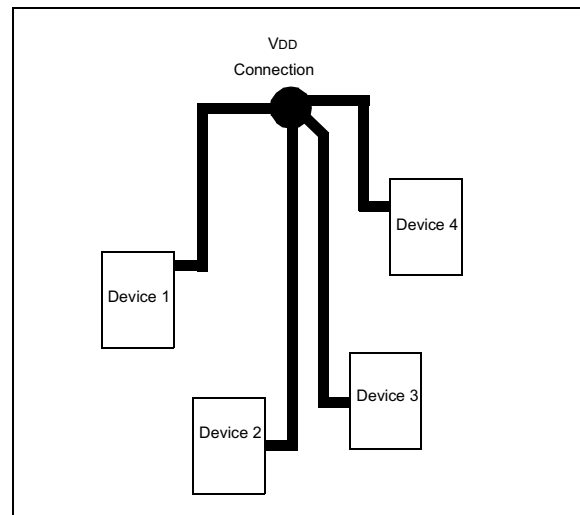
**FIGURE 6-3:** The MCP601 Operational Amplifier is used to implement a 2nd order anti-aliasing filter for the signal being converted by the MCP3202.

## 6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 0.1 µF is recommended.

Digital and analog traces should be separated as much as possible on the board and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V<sub>DD</sub> connections to devices in a "star" configuration can also reduce noise by eliminating current return paths and associated errors. See Figure 6-4. For more information on layout tips when using A/D Converters, refer to AN688 "Layout Tips for 12-Bit A/D Converter Applications".



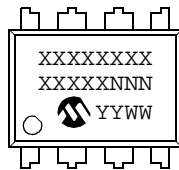
**FIGURE 6-4:** V<sub>DD</sub> traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.



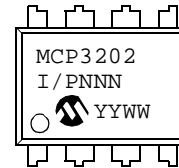
## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information

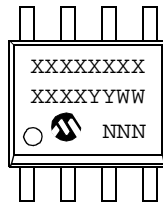
8-Lead PDIP (300 mil)



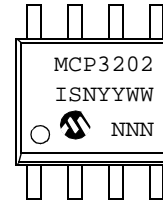
Example:



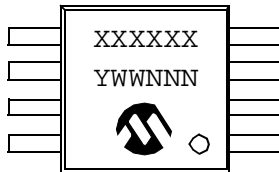
8-Lead SOIC (150 mil)



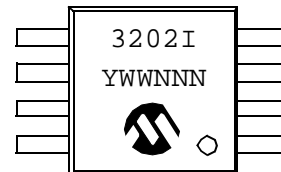
Example:



8-Lead MSOP



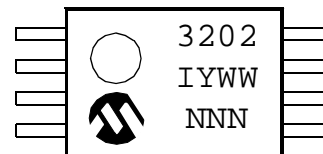
Example:



8-Lead TSSOP



Example:



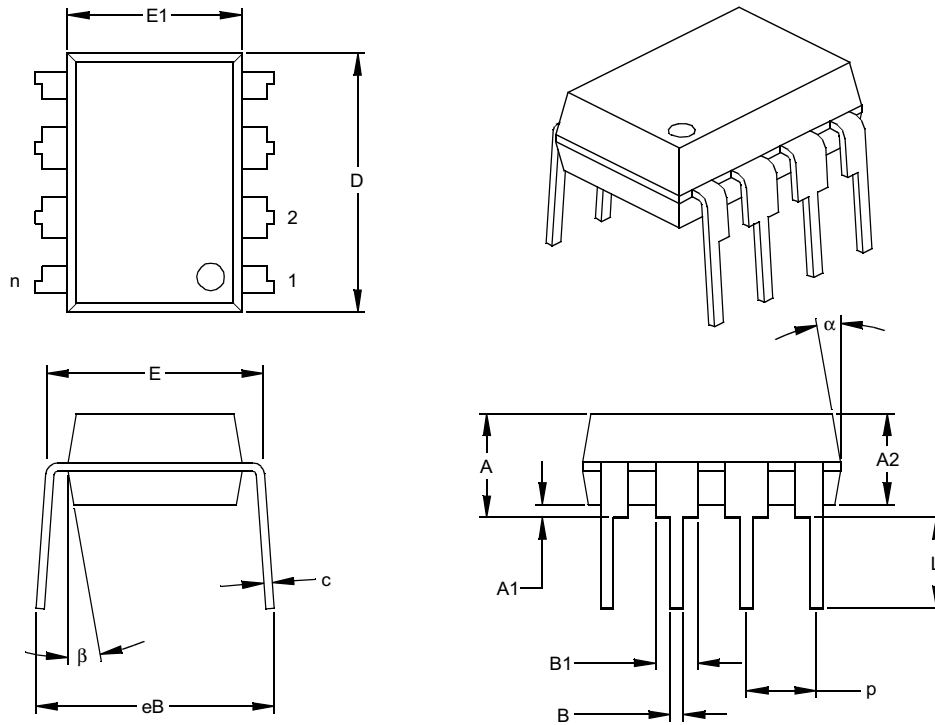
<b>Legend:</b>	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.
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\* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code.

# MCP3202

## 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

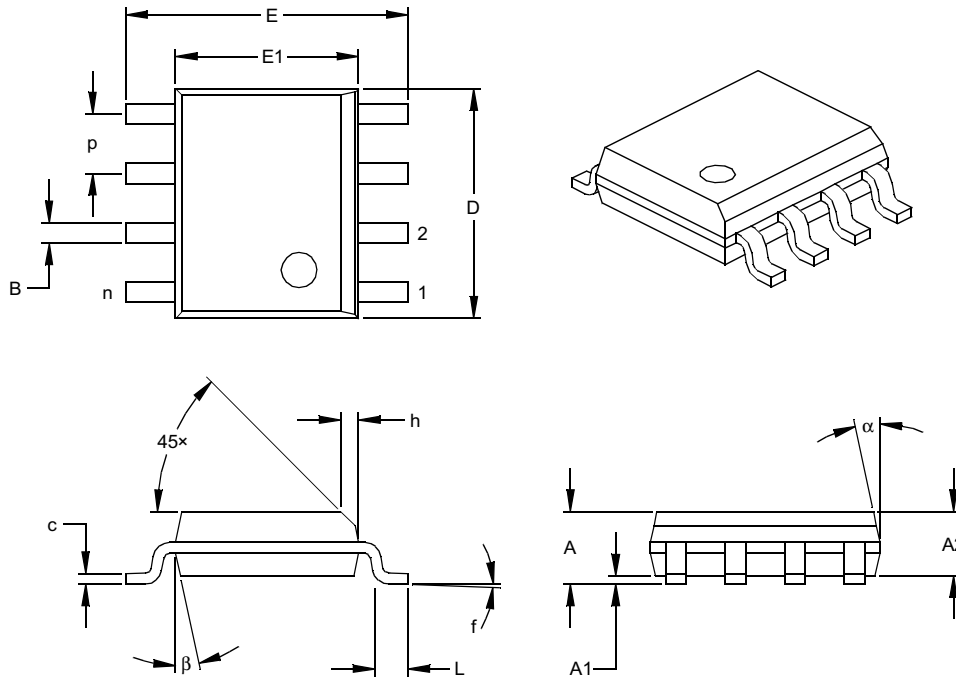
### Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter  
 § Significant Characteristic

**Notes:**

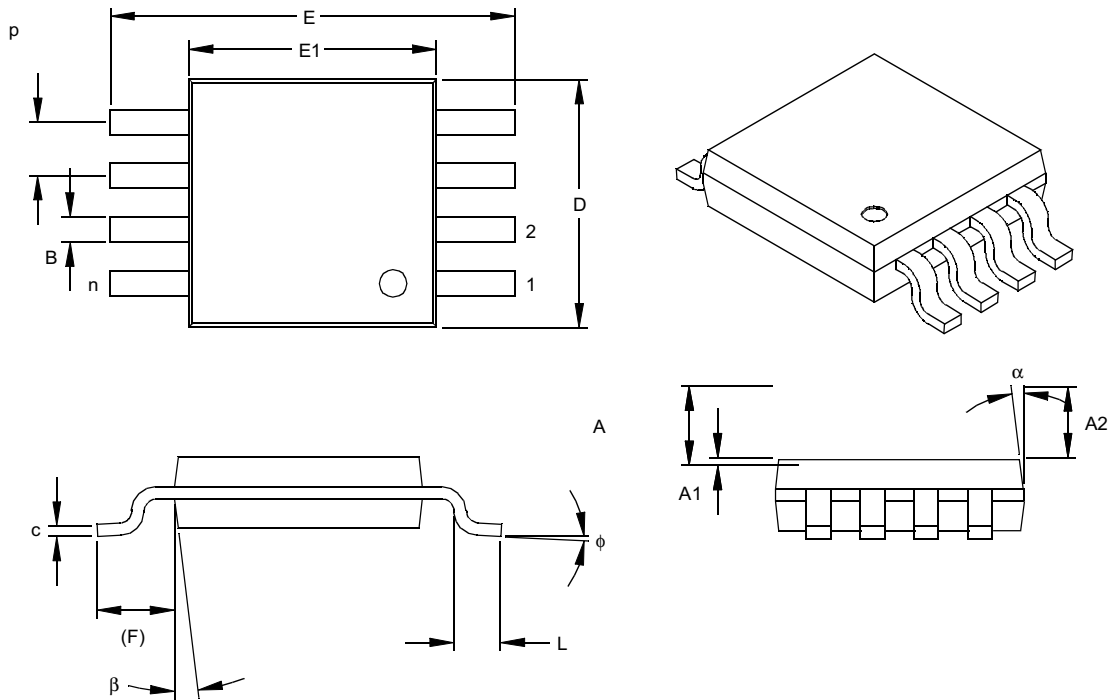
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

# MCP3202

## 8-Lead Plastic Micro Small Outline Package (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	P	.026			0.65		
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

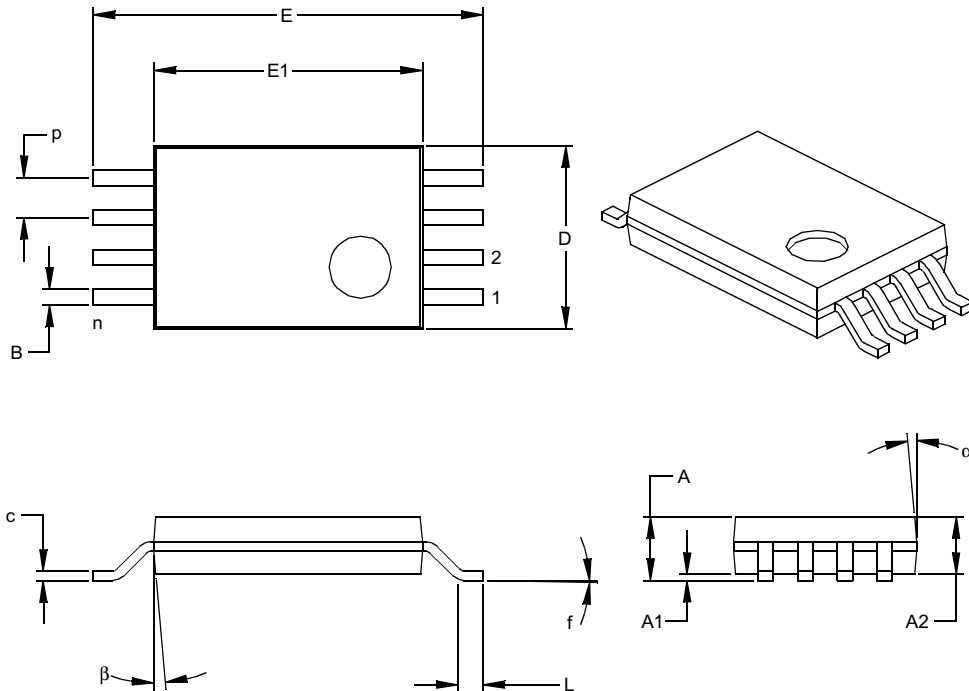
\*Controlling Parameter  
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

## 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter  
 § Significant Characteristic

Notes:  
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.  
 JEDEC Equivalent: MO-153  
 Drawing No. C04-086

# MCP3202

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NOTES:

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Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

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**<ftp://ftp.microchip.com>**

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013001

# MCP3202

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Device: **MCP3202** Literature Number: **DS21034C**

Questions:

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\_\_\_\_\_
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\_\_\_\_\_  
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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>		<u>X</u>	<u>X</u>	<u>/XX</u>
Device	Performance Grade	Temperature Range	Package	
Device:	MCP3202:	12-Bit Serial A/d Converter		
	MCP3202T:	12-Bit Serial A/D Converter (Tape and Reel) (SOIC and TSSOP package only)		
Performance Grade:	B	= ±1 LSB INL (TSSOP not available)		
	C	= ±2 LSB INL		
Temperature Range:	I	= -40°C to +85°C		
Package:	MS	= Plastic Micro Small Outline (MSOP), 8-Lead		
	P	= Plastic DIP (300 mil Body), 8-Lead		
	SN	= Plastic SOIC (150 mil Body), 8-Lead		
	ST	= TSSOP (4.4 mm Body), 8-Lead (C Grade only)		

**Examples:**

- a) MCP3202-I/MS: = Industrial temperature, MSOP package.
- b) MCP3202-BI/P: = B Performance grade, industrial temp., PDIP package
- c) MCP3202-CI/SN: = C Performance grade, industrial temp., SOIC package
- d) MCP3202T-BI/SN: = Tape and Reel, B Performance grade, industrial temp., SOIC package
- a) MCP3202T-CI/ST: = Tape and Reel, C Performance grade, industrial temp., TSSOP package.

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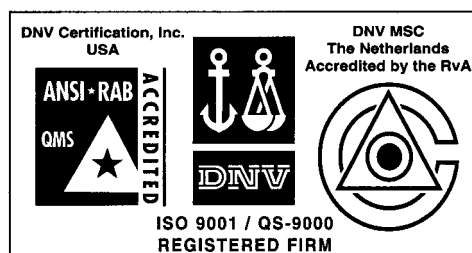
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#### New York

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Tel: 631-273-5305 Fax: 631-273-5335

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Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408-436-7950 Fax: 408-436-7955

#### Toronto

6285 Northam Drive, Suite 108  
Mississauga, Ontario L4V 1X5, Canada  
Tel: 905-673-0699 Fax: 905-673-6509

### ASIA/PACIFIC

#### Australia

Microchip Technology Australia Pty Ltd  
Suite 22, 41 Rawson Street  
Epping 2121, NSW  
Australia  
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

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Microchip Technology Consulting (Shanghai)  
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No. 6 Chaoyangmen Beidajie  
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#### China - Shenzhen

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Shenzhen Liaison Office  
Rm. 1315, 13/F, Shenzhen Kerry Centre,  
Renminnan Lu  
Shenzhen 518001, China  
Tel: 86-755-2350361 Fax: 86-755-2366086

#### Hong Kong

Microchip Technology Hongkong Ltd.  
Unit 901-6, Tower 2, Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2401-1200 Fax: 852-2401-3431

#### India

Microchip Technology Inc.  
India Liaison Office  
Divyasree Chambers  
1 Floor, Wing A (A3/A4)  
No. 11, O'Shaughnessy Road  
Bangalore, 560 025, India  
Tel: 91-80-2290061 Fax: 91-80-2290062

### Japan

Microchip Technology Japan K.K.  
Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
Kanagawa, 222-0033, Japan  
Tel: 81-45-471-6166 Fax: 81-45-471-6122

### Korea

Microchip Technology Korea  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea 135-882  
Tel: 82-2-554-7200 Fax: 82-2-558-5934

### Singapore

Microchip Technology Singapore Pte Ltd.  
200 Middle Road  
#07-02 Prime Centre  
Singapore, 188980  
Tel: 65-334-8870 Fax: 65-334-8850

### Taiwan

Microchip Technology Taiwan  
11F-3, No. 207  
Tung Hua North Road  
Taipei, 105, Taiwan  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### Denmark

Microchip Technology Nordic ApS  
Regus Business Centre  
Lautrup høj 1-3  
Ballerup DK-2750 Denmark  
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#### France

Microchip Technology SARL  
Parc d'Activite du Moulin de Massy  
43 Rue du Saule Trapu  
Batiment A - 1er Etage  
91300 Massy, France  
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

#### Germany

Microchip Technology GmbH  
Gustav-Heinemann Ring 125  
D-81739 Munich, Germany  
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

#### Italy

Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Taurus 1 V. Le Colleoni 1  
20041 Agrate Brianza  
Milan, Italy  
Tel: 39-039-65791-1 Fax: 39-039-6899883

#### United Kingdom

Arizona Microchip Technology Ltd.  
505 Eskdale Road  
Winnersh Triangle  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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