MCP2502X/5X

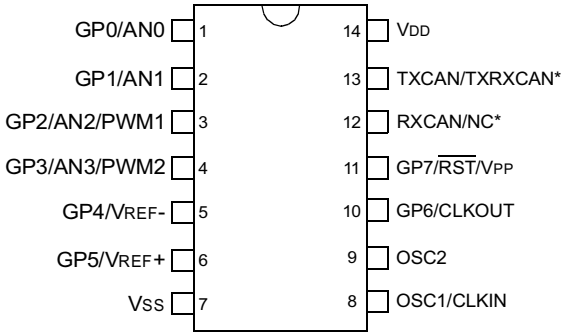
CAN I/O Expander Family

Features

- Implements CAN V2.0B
  - Programmable bit rate up to 1 Mb/s
  - One programmable mask
  - Two programmable filters
  - Three auto-transmit buffers
  - Two message reception buffers
  - Does not require synchronization or configuration messages
- Hardware Features
  - Non-volatile memory for user configuration
  - User configuration automatically loaded on power-up
  - Eight general purpose I/O lines individually selectable as inputs or outputs
  - Individually selectable transmit-on-pin-change for each input
  - Four, 10-bit, analog input channels with programmable conversion clock and VREF sources (MCP2505X devices only)
  - Message scheduling capability
  - Two, 10-bit PWM outputs with independently programmable frequencies
  - Device configuration can be modified via CAN bus messages
  - In-Circuit Serial Programming™ (ICSP™) of default configuration memory
  - Optional 1-wire CAN bus operation
- Low power CMOS technology
  - Operates from 2.7V to 5.5V
  - 10 mA active current typical
  - 30 µA standby current (CAN Sleep mode)
- 14-pin PDIP (300 mil) and SOIC (150 mil) packages
- Available temperature ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C

Package Types

PDIP/SOIC



* One-wire option available on MCP250X5 devices.

Description

The MCP2502X/5X devices operate as I/O expanders for a Controller Area Network (CAN) system, supporting CAN V2.0B active with bus rates up to 1 Mb/s, The MCP2502X/5X allows a simple CAN node to be implemented without the need for a microcontroller.

The devices are identical, with the following exceptions:

Device	A/D	One-wire CAN
MCP25020	No	No
MCP25025	No	Yes
MCP25050	Yes	No
MCP25055	Yes	Yes

The MCP2502X/5X devices feature a number of peripherals, including digital I/O, four channel 10-bit A/D (MCP2505X), and PWM outputs, with automatic message transmission on change of input state, including when an analog input exceeds a preset threshold.

One mask and two acceptance filters are provided to give maximum flexibility during system design with respect to identifiers that the device will respond to. The device can also be configured to automatically transmit a unique message whenever any of several error conditions occur.

The device is pre-programmed in non-volatile memory so that the part defaults to a specific configuration upon power-up.

Definition of Terms

The following terms are used throughout this document:

I/O Expander - refers to the integrated circuit (IC) device being described (MCP2502X/5X).

Input Message - term given to messages that are received by the MCP2502X/5X and cause the internal registers to be modified. Once the register modification has been performed, the MCP2502X/5X transmits a 'Command Acknowledge' message to indicate that the command was received and processed.

Command Acknowledge Message - term given to the message that is automatically transmitted by the MCP2502X/5X after receiving and processing an input message.

Information Request Message - term given to Remote Request messages that are received by the MCP2502X/5X which subsequently generate an output message (data frame) in response.

Output Message - term given to the message that the MCP2502X/5X sends in response to a Information Request message.

On Bus Message - term given to the message that the MCP2502X/5X transmits after completing the power-on/self configuration sequence and at timed intervals if enabled.

Self Configuration - term used to describe the process of transferring the contents of the EPROM memory array to the SRAM memory array.

On Bus - term used to describe the condition when the MCP2502X/5X is fully configured and ready to transmit or receive on the bus. On bus is the only state in which the MCP2502X/5X can transmit on the bus.

Edge Detection - refers to the MCP2502X/5X's abilility to automatically transmit a message due to the occurance of a predefined edge on any digital input.

Threshold Detection - refers to the MCP2502X/5X's ability to automatically transmit a message when a predefined analog threshold is reached.

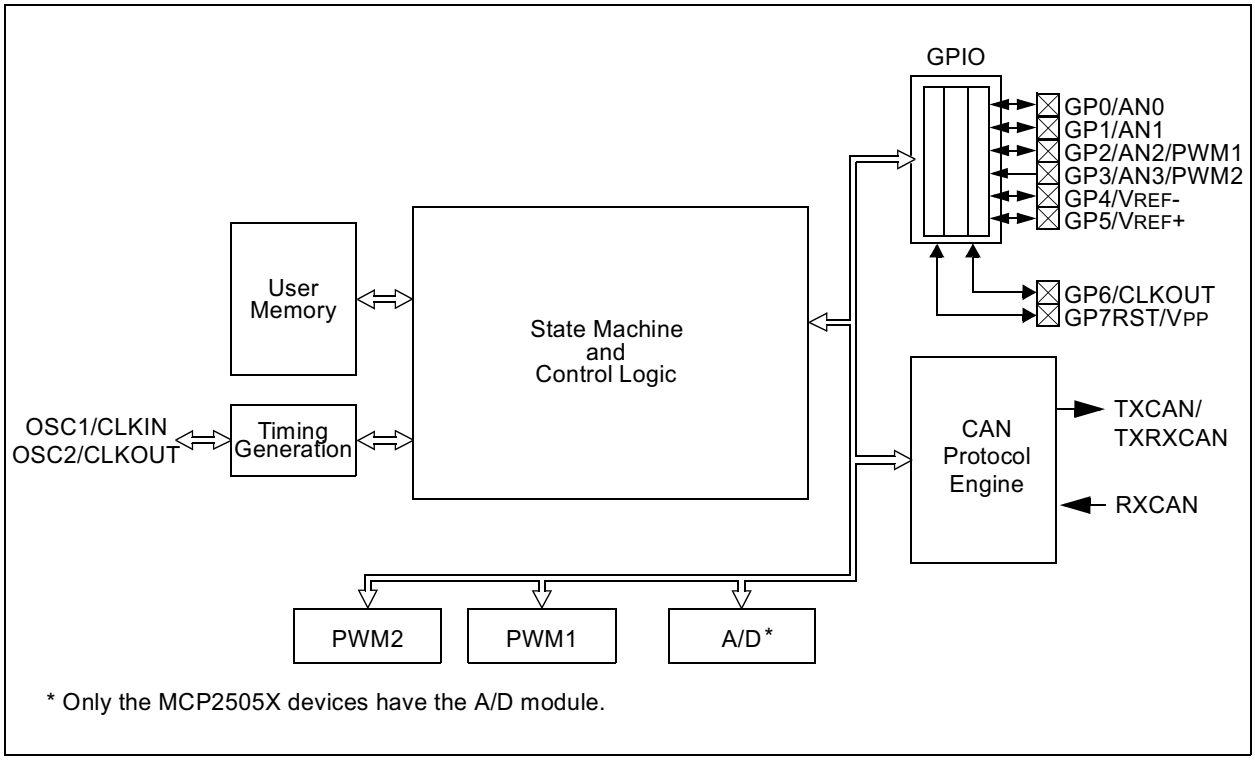
1.0 DEVICE OVERVIEW

This document contains device-specific information on the MCP2502X/5X family of CAN I/O expanders. The CAN protocol is not discussed in depth in this document. Additional information on the CAN protocol can be found in the “CAN Specification” as defined by Robert Bosch GmbH.

Figure 1-1 is the block diagram of the MCP2502X/5X and Table 1-1 is the pinout description.

The following sections detail the modules as listed in Figure 1-1.

FIGURE 1-1: MCP2502X/5X BLOCK DIAGRAM



* Only the MCP2505X devices have the A/D module.

TABLE 1-1: PINOUT DESCRIPTION

Pin Name	Pin Number	Standard Function	Alternate Function	Programming Mode Function
GP0/AN0 *	1	Bi-directional I/O pin, TTL input buffer	Analog input channel	None
GP1/AN1 *	2	Bi-directional I/O pin, TTL input buffer	Analog input channel	None
GP2/AN2/PWM2 *	3	Bi-directional I/O pin, TTL input buffer	Analog input/PWM output	None
GP3/AN3/PWM3 *	4	Bi-directional I/O pin, TTL input buffer	Analog input/PWM output	None
GP4/VREF-	5	External oscillator input	External clock input	None
GP5/VREF+	6	External oscillator output	None	None
VSS	7	Ground	None	Ground
OSC1/CLKIN	8	Bi-directional I/O pin, TTL input buffer	External VREF-	Data
OSC2	9	Bi-directional I/O pin, TTL input buffer	External VREF input	Clock
GP6/CLKOUT	10	Bi-directional I/O pin, TTL input buffer	CLKOUT output	None
GP7/$\overline{\text{RST}}$/VPP	11	Bi-directional I/O pin, TTL input buffer	External Reset input	Vpp
RXCAN	12	CAN data receive input	Not connected for 1-wire	None
TXCAN/TXRXCAN	13	CAN data transmit output	CAN TX and RX for 1-wire operation (MCP250X5)	None
VDD	14	Power	None	Power

* Only the MCP2505X devices have the A/D module

2.0 CAN MODULE

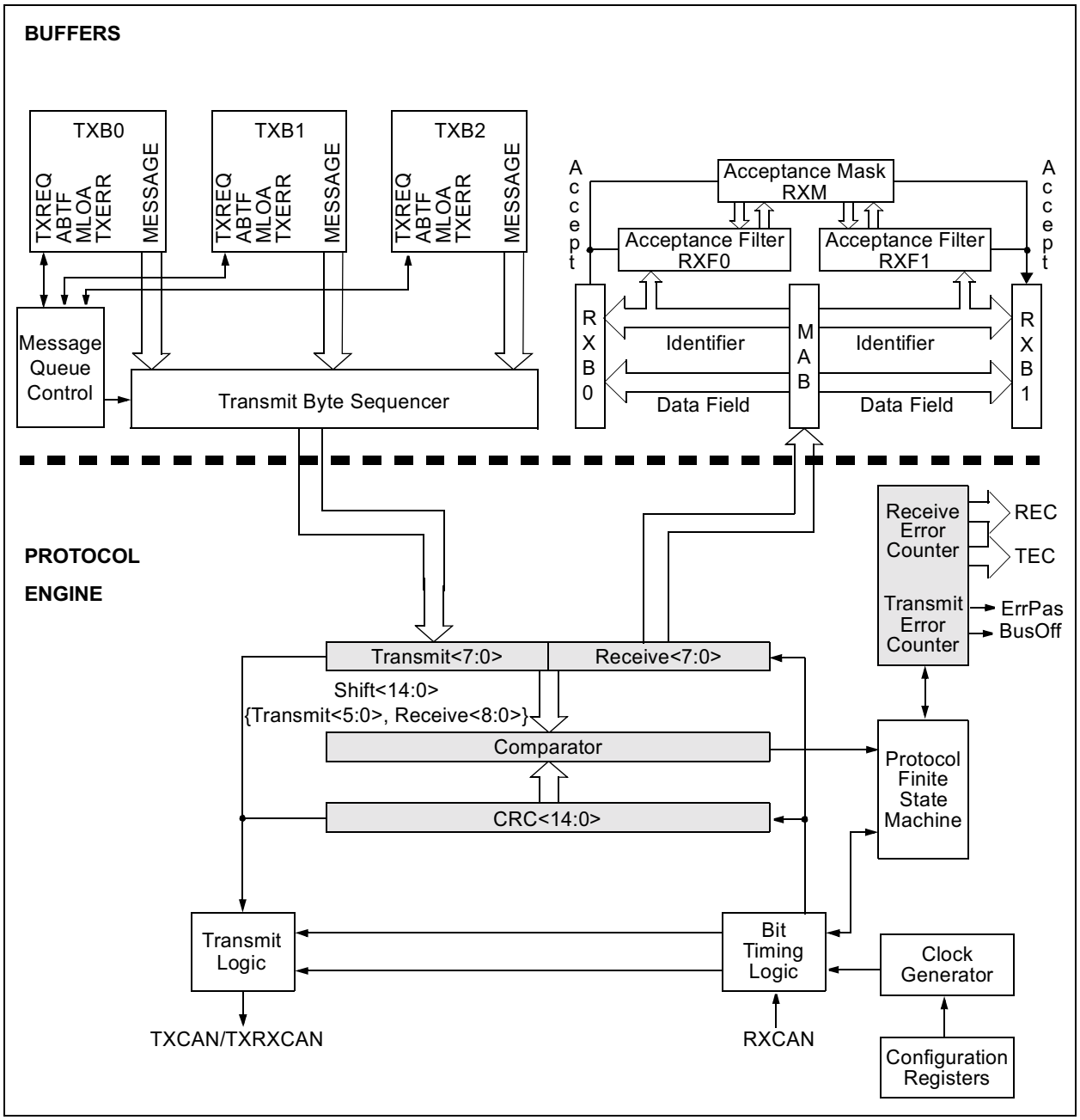
The CAN module is a protocol controller that converts between raw digital data and CAN message packets. The main functional block of the CAN module are shown in Figure 2-1 and consists of:

- CAN protocol engine
- Buffers, Masks, and Filters

The module features are as follows:

- Implementation of the CAN protocol
- Double buffered receiver with two separate receive buffers
- One full acceptance mask (standard and extended)
- Two full acceptance filters (standard and extended)
- One filter for each receive buffer
- Three prioritized transmit buffers
- For transmitting predefined message types
- Automatic wake-up on bus traffic function
- Error management logic for transmit and receive error states
- Low power SLEEP mode

FIGURE 2-1: CAN MODULE



2.1 CAN Protocol Finite State Machine

The heart of the engine is the Finite State Machine (FSM). This state machine sequences through messages on a bit by bit basis, changing states as the fields of the various frame types are transmitted or received. The FSM is a sequencer controlling the sequential data stream between the TX/RX Shift Register, the CRC Register, and the bus line. The FSM also controls the Error Management Logic (EML) and the parallel data stream between the TX/RX Shift Registers and the buffers. The FSM insures that the processes of reception, arbitration, transmission, and error signaling are performed according to the CAN protocol. The automatic retransmission of messages on the bus line is also handled.

2.2 Cyclic Redundancy Check (CRC)

The Cyclic Redundancy Check Register generates the Cyclic Redundancy Check (CRC) code which is transmitted after either the Control Field (for messages with 0 data bytes) or the Data Field, and is used to check the CRC field of incoming messages.

2.3 Error Management Logic

The Error Management Logic is responsible for the fault confinement of the CAN device. Its two counters, the Receive Error Counter (REC) and the Transmit Error Counter (TEC), are incremented and decremented by commands from the Bit Stream Processor. According to the values of the error counters, the MCP2502X/5X is set into the states error-active, error-passive, or bus-off.

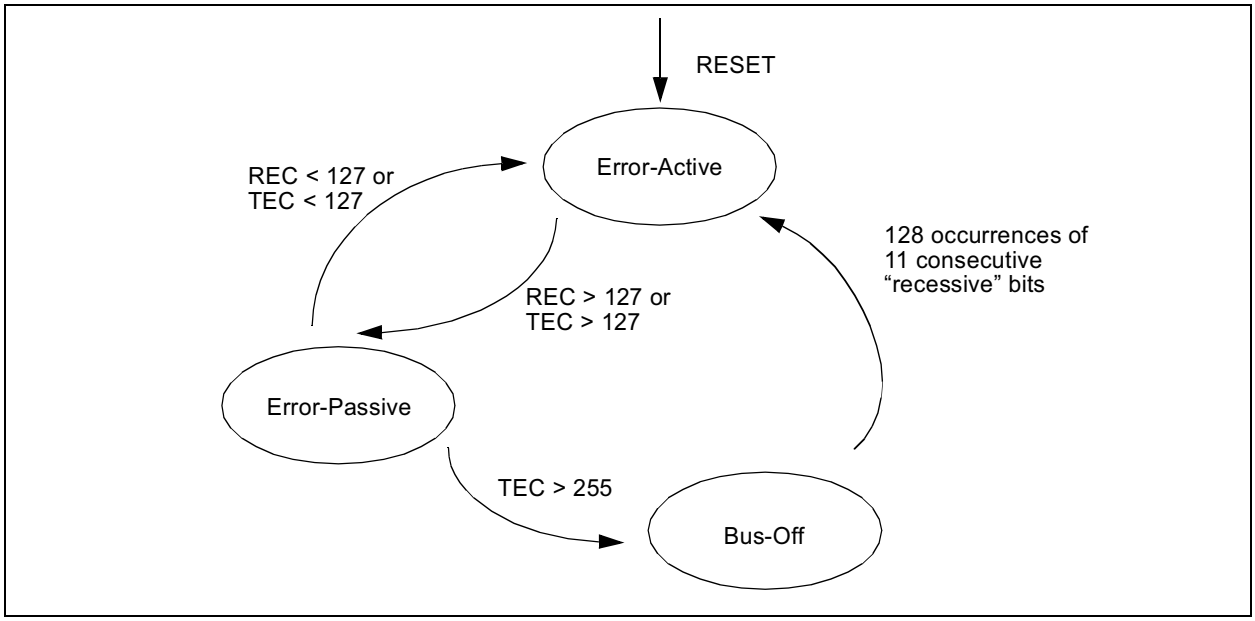
Error-active: Both error counters are below the error-passive limit of 128.

Error-passive: At least one of the error counters (TEC or REC) equals or exceeds 128.

Bus-off: The transmit error counter (TEC) equals or exceeds the bus-off limit of 256. The device remains in this state, until the bus-off recovery sequence is received. The bus-off recovery sequence consists of 128 occurrences of 11 consecutive recessive bits.

Note:	The MCP2502X/5X, after going bus-off, will recover back to error-active automatically if the bus remains idle for 128 X 11 bits. OPTREG2.ERRE must be set to force the MCP2502X/5X to enter Listen Only mode instead of Normal mode during bus recovery. The current error mode (except for bus-off) of the MCP2502X/5X can be determined by reading the EFLG register via the “Read CAN Error” message.

FIGURE 2-2: ERROR MODES STATE DIAGRAM



REGISTER 2-1: TEC - TRANSMITTER ERROR COUNTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0: **TEC<7:0>**: Transmit Error Counter

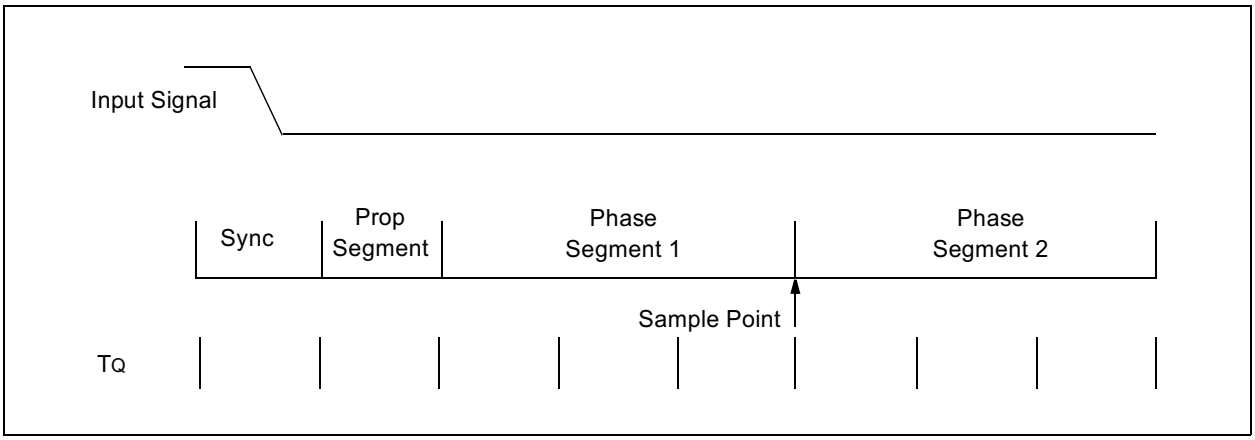
REGISTER 2-2: REC - RECEIVER ERROR COUNTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
REC7	REC6	REC5	REC4	REC3	REC2	REC1	REC0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0: **REC<7:0>**: Receive Error Counter

FIGURE 2-3: BIT TIME PARTITIONING



2.4 Bit Timing Logic

The Bit Timing Logic (BTL) monitors the bus line input and handles the bus-related bit timing according to the CAN protocol. The BTL synchronizes on a recessive-to-dominant bus transition at Start-of-Frame (hard synchronization) and on any further recessive-to-dominant bus line transition if the CAN controller itself does not transmit a dominant bit (resynchronization). The BTL also provides programmable time segments to compensate for the propagation delay time, phase shifts, and to define the position of the Sample Point within the bit time. These programmable segments are made up of integer units called Time Quanta (TQ). The nominal bit time is calculated by programming the TQ length and the number of TQ in each time segment as discussed below.

2.4.1 TIME QUANTUM (TQ)

A Time Quantum is a fixed unit of time derived from the oscillator period. There is a programmable baud rate prescaler (BRP), with integral values ranging from 1 to 64, in addition to a fixed divide by two for clock generation.

The base TQ is defined as twice the oscillator period. Adding the BRP into the equation yields:

$$T_Q = 2 * T_{OSC} * (BRP + 1)$$

where BRP = binary value represented by CNF1.BRP<5:0>

By definition, the nominal bit time is programmable from a minimum of 8TQ to 25TQ. Also, the minimum nominal bit time is 1 µs which corresponds to 1 Mb/s.

2.4.2 TIME SEGMENTS

Time segments make up the nominal bit time. The nominal bit time can be thought of as being divided into separate non-overlapping time segments. These segments are shown in Figure 2-3.

- Synchronization Segment (SyncSeg)
- Propagation Segment (PropSeg)
- Phase Buffer Segment 1 (PS1)
- Phase Buffer Segment 2 (PS2)

$$Nominal\ Bit\ Time = T_Q * (Sync\_Seg + PropSeg + Phase\_Seg1 + Phase\_Seg2)$$

Rules for Programming the Segments

There are a few rules to follow when programming the time segments:

- PropSeg + PS1 >= PS2
- PS2 > Sync Jump Width
- PS2 >= Information Processing Time

2.4.2.1 Synchronization Segment

This part of the bit time is used to synchronize the various CAN nodes on the bus. The edge of the input signal is expected to occur during the SyncSeg. The duration is fixed at 1TQ.

2.4.2.2 Propagation Segment

This part of the bit time is used to compensate for physical delay times within the network. These delay times consist of the signal propagation time on the bus line and the internal delay time of the nodes. The delay is calculated as being the round trip time from transmitter to receiver (twice the signal's propagation time on the bus line), the input comparator delay, and the output driver delay. The length of the Propagation Segment can be programmed from 1TQ to 8TQ by setting the PRSEG2:PRSEG0 bits of the CNF2 register.

2.4.2.3 Phase Buffer Segments

The Phase Buffer Segments are used to optimally locate the sampling point of the received bit within the nominal bit time. The sampling point occurs between PS1 and PS2. These segments can be automatically lengthened or shortened by the resynchronization process. Thus, the variation of the values of the phase buffer segments represent the DPLL functionality.

Phase Segment 1: The end of PS1 determines the sampling point within a bit time. PS1 is programmable from 1TQ - 8TQ in duration.

Phase Segment 2: PS2 provides delay before the next transmitted data transition and is also programmable from 1TQ - 8TQ in duration. However, due to IPT requirements, the actual minimum length of phase segment 2 is 2TQ, or it may be defined to be equal to the greater of PS1 or the Information Processing Time (IPT).

2.4.3 SAMPLE POINT

The Sample Point is the point of time at which the bus level is read and value of the received bit is determined. The sampling point occurs at the end of PS1. If desired, it is possible to specify multiple sampling of the bus line at the sample point. The value of the received bit is determined to be the value of the majority decision of three values. The three samples are taken at the sample point, and twice before with a time of TQ / 2 between each sample.

2.4.4 INFORMATION PROCESSING TIME

The Information Processing Time (IPT) is the time segment, starting at the sample point, that is reserved for calculation of the subsequent bit level. The CAN specification defines this time to be less than or equal to 2TQ. The MCP2502X/5X defines this time to be 2TQ. Thus, PS2 must be at least 2TQ long.

2.4.5 SYNCHRONIZATION JUMP WIDTH

To compensate for phase shifts and oscillator tolerances between the nodes in the system, each CAN controller must be able to synchronize to the relevant signal edge of the incoming signal. When a recessive-to-dominant edge in the transmitted data is detected, the logic will compare the location of the edge to the expected time (SyncSeg). The circuit will then adjust the values of PS1 and PS2 as necessary using the programmed Synchronization Jump Width (SJW). This adjustment is made for *resynchronization* during a message and not *hard synchronization* which occurs only at the message Start-of-Frame (SOF).

As a result of resynchronization, PS1 may be lengthened or PS2 may be shortened. The amount of lengthening or shortening of the phase buffer segments has an upper bound given by the SJW. The SJW is programmable between 1TQ and 4TQ. The value of the SJW will be added to PS1 or subtracted from PS2 depending on the phase error (e) of the edge in relation to the receiver's SyncSeg. The phase error is defined as follows:

- e = 0 if the edge lies within SYNCESEG
  - No resynchronization is required.
- e > 0 if the edge lies ***before*** the sample point
  - PS1 will be ***lengthened*** by the amount of the SJW.
- e < 0 if the edge lies ***after*** the sample point of the previous bit and before the SyncSeg of the current bit
  - PS2 will be ***shortened*** by the amount of the SJW.

2.4.6 CONFIGURATION REGISTERS

There are three registers (in the configuration register module) associated with the CAN bit timing logic that control the bit timing for the CAN bus interface.

2.4.6.1 CNF1

The BRP<5:0> bits control the baud rate prescaler. These bits set the length of TQ relative to the OSC1 input frequency, with the minimum length of TQ being 2TOSC in length (when BRP<5:0> are set to 000000). The SJW<1:0> bits select the synchronization jump width in terms of number of TQ's.

2.4.6.2 CNF2

The PRSEG<2:0> bits set the length (in TQ's) of the propagation segment. The PS1<2:0> bits set the length (in TQ's) of phase segment 1. The SAM bit controls how many times the RXCAN pin is sampled. Setting this bit to a '1' causes the bus to be sampled three times; twice at TQ/2 before the sample point, and once at the normal sample point (which is at the end of phase segment 1). The value of the bus is determined to be the value read during at least two of the samples. If the SAM bit is set to a '0' then the RXCAN pin is sampled only once at the sample point. The BTLMODE bit controls how the length of phase segment 2 is determined. If this bit is set to a '1' then the length of phase segment 2 is determined by the PS2<2:0> bits of CNF3. If the BTLMODE bit is set to a '0' then the length of phase segment 2 is the greater of phase segment 1 and the information processing time (which is fixed at 2TQ for the MCP2502X/5X).

2.4.6.3 CNF3

The PS2<2:0> bits set the length, in TQ's, of Phase Segment 2, if the CNF2.BTLMODE bit is set to a '1'. If the BTLMODE bit is set to a '0' then the PS2<2:0> bits have no effect.

In addition, the wake-up filter (CNF3.WAKFIL) is implemented in the CNF3 register. This filter is a low pass filter that can be used to prevent the MCP2502X/5X from waking up due to short glitches on the CAN bus.

REGISTER 2-3: CNF1 - CAN CONFIGURATION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-6: **SJW1:SJW0**: Synchronized Jump Width
11 = Length = 4 x TQ
10 = Length = 3 x TQ
01 = Length = 2 x TQ
00 = Length = 1 x TQ

bit 5-0: **BRP5:BRP0**:Baud Rate Prescaler
111111 = TQ = 2 x 64 x 1/FOSC
²
²
000000 = TQ = 2 x 1 x 1/FOSC

REGISTER 2-4: CNF2 - CAN CONFIGURATION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BTLMODE	SAM	PHSEG12	PHSEG11	PHSEG10	PRSEG2	PRSEG1	PRSEG0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7: **BTLMODE**: Length determination of PHSEG2
1 = Length of Phase_Seg2 determined by bits 2:0 of CNF3
0 = Length of Phase_Seg2 is the greater of Phase_Seg1 or IPT(2TQ)

bit 6: **SAM**: Sample of the CAN bus line
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 5-3: **PHSEG12:PHSEG10**: Phase Buffer Segment1
111 = length = 8 x TQ
-
-
-
000 = length = 1 x TQ

bit 2-0 **PRSEG2:PRSEG0**: Propagation Time Segment
111 = length = 8 x TQ
-
-
-
000 = length = 1 x TQ

REGISTER 2-5: CNF3 - CAN CONFIGURATION REGISTER 3

U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	WAKFIL	—	—	—	PHSEG22	PHSEG21	PHSEG20
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7 **Unimplemented**: (Reads as 0)

bit 6 **WAKFIL**: Wake-up filter

1 = Wake-up filter enabled
0 = Wake-up filter disabled

bit 5:3 **Unimplemented**: (Reads as 0)

bit 2-0 **PHSEG22:PHSEG20**: Phase Buffer Segment2
111 = length = 8 x TQ
-
-
-
001 = length = 2 x TQ
000 = Invalid

2.5 Buffers, Masks, and Filters

This part of the CAN module supports the transmitting, receiving and acceptance of CAN messages.

Three transmit buffers are used for the three ***transmit message IDs*** as discussed later in this section. Two ***receive buffers*** store the CAN message's arbitration field, control field, and the data field.

One mask defines which bits are to be applied to either filter. The mask can be regarded as defining "don't care" bits for the filter.

Each of the two filters define a bit pattern that will be compared to all incoming messages. All filter bits that have not been defined as "don't care" by the mask are applied to the message.

2.5.1 TRANSMIT MESSAGE ID'S

The MCP2502X/5X device contains three separate transmit message ID's: TXID0, TXID1, and TXID2. The data length code is predefined for each of the various

output messages and the data that is transmitted comes directly from the contents of the device's peripheral registers.

2.5.1.1 Transmit Message ID0 (TXID0)

Transmit ID0 contains the identifier that is used when transmitting the 'On Bus' message. If enabled (STCON.STEN = 1), the 'On Bus' message will be transmitted at predefined intervals. Depending on the message select bit (STCON.STMS = 1), the CAN message will send GPIO and A/D data.

Transmit Message ID0 will not automatically be sent when the device is brought out of sleep.

2.5.1.2 Transmit Message ID1 (TXID1)

Transmit ID1 contains the identifier that is used when the MCP2502X/5X sends the "Command Acknowledge" message, the "Receive Overflow" message and/or the "Error Condition" message. All message types use the same identifier.

The CAEN bit in the OPTREG2 register selects between the Command Acknowledge and Receive Overflow operation. These message types have a DLC of 0 and do not contain any data. The Error Condition message can occur anytime, has a DLC of 3, and contains the EFLG, TEC, and REC data values.

Note:	A zero data length 'On Bus' message will be transmitted once after power-up regardless of scheduled transmission enable status.

Command Acknowledge: TXID1 sends a Command Acknowledge message when the MCP2502X/5X receives an Input Message and processes the instruction (and OPTREG2.CAEN = 1). This message is used as a handshake for the node requesting the modification of the MCP2502X/5X. There is no data associated with this message.

Receive Overflow: TXID1 sends a Receive Overflow message if there is a Receive Overflow condition (and OPTREG2.CAEN = 0). This only occurs if the device has received a valid message before processing the previous valid message from the same receive buffer. There is no data associated with this message.

Error Condition: An Error Condition message is transmitted if the TEC or REC counters reach error warning (> 95) or error passive (> 127). This message contains the TXID1 identifier and the TEC, REC and EFLG.

A hysteresis is implemented in hardware that prevents messages from repeatedly being transmitted due to error counts changing by one or two bits. After a message is sent for an error warning (TEC or REC > 95), the message will not trigger again until the error counter ≤ 79 and back to > 95 (hysteresis = 17 counts).

Similarly, an error passive message is sent at TEC or REC > 127 and is not sent again until the error counter ≤ 111 and back to > 127 (hysteresis = 17 counts).

2.5.1.3 Transmit Message ID2 (TXID2)

Transmit ID2 contains the identifier that is used when transmitting auto-conversion initiated messages, including digital input edge detection and/or analog input exceeding a threshold. This message will also be sent when the device wakes up from sleep due to a digital input change of state condition (i.e., change of state occurs on input configured to transmit-on-change of state).

2.6 Receive Buffers

The MCP2505X contains two receive buffers, each with their own filter. There is also a Message Assembly Buffer (MAB) which acts as a third receive buffer (see Figure 2-1).

The two receive buffers combined with the MAB helps insure that received messages will be processed while minimizing the chances of receive buffer overrun due to maximum bus loading of messages destined for the MCP2502X/5X.

Note:	The receive buffers are used by the MCP2502X/5X to implement the "Command Messages" and are not externally accessible.

2.7 Acceptance Mask

The acceptance mask is used to define which bits in the CAN ID are to be compared against the programmable filters. Individual bits within the mask correspond to bits in the CAN ID, which correspond to bits in the acceptance filters. Any bit in the mask that is set to a '1' will cause the corresponding CAN ID bit to be compared against the associated filter bit. Any bit in the mask that is set to a '0' is not compared and effectively sets the associated CAN ID bit to 'don't care'.

2.7.1 MASKS AND STANDARD/ EXTENDED IDS

To insure proper operation of the "Information Request" and "Input" messages, some mask bits as configured in the mask registers may be ignored as explained:

Message with a standard ID - The three least significant bits of a standard identifier (RXMSIDL.SID2:SID0) are 'don't care' for the mask registers and effectively become ZERO.

Message with an extended ID - The three least significant bits of the standard identifier (RXMSIDL.SID2:SID0) are configurable and the three least

significant bits of the extended identifier (RXMEID0.EID2:EID0) are always 'don't care' and effectively become ZERO.

Note:	The EXIDE bit in the Mask register (RXM-SIDL) can be used to mask the IDE bit in the corresponding Receive buffer register (RXBnSIDL).

2.8 Acceptance Filters

There are two separate acceptance filters defined for the MCP2502X/5X: RXF0 and RXF1. RXF0 is used for "Information Request" messages and RXF1 is used for "Input" messages (seeTable 4-2 and Table 4-3). Each bit in the filters corresponds to a bit in the CAN ID. Every bit in the CAN ID, for which the corresponding Mask bit is set, must match the associated filter bit in order for the message to be accepted. Messages that fail to meet the Mask/FIlter criteria are ignored.

REGISTER 2-6: TXIDNSIDH - TRANSMIT IDENTIFIER N STANDARD IDENTIFIER HIGH

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0: **SID10:SID3**: Standard Identifier

REGISTER 2-7: TXIDNSIDL - TRANSMIT IDENTIFIER N STANDARD IDENTIFIER LOW

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDE	—	EID17	EID16
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-5: **SID2:SID0**: Standard Identifier

bit 4: **Unimplemented**: Read as '0'

bit 3: **EXIDE**: Extended Identifier Enable
1 = Message will transmit extended identifier
0 = Message will transmit standard identifier

bit 2: **Unimplemented**: Read as '0'

bit 1-0: **EID17:EID16**: Extended Identifier

REGISTER 2-8: TXIDNEID8 - TRANSMIT IDENTIFIER N EXTENDED IDENTIFIER HIGH

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0: **EID15:EID8**: Extended Identifier

REGISTER 2-9: TXIDNEID0 - TRANSMIT IDENTIFIER N EXTENDED IDENTIFIER LOW

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0: **EID7:EID0**: Extended Identifier

REGISTER 2-10: TXIDNDLC - TRANSMIT IDENTIFIER N DATA LENGTH CODE

U-0	Reserved	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	R	—	—	DLC3	DLC2	DLC1	DLC0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7: **Unimplemented:** Reads as '0'

bit 6: **Reserved:** Clear to '0'

bit 5-4: **Unimplemented:** Reads as '0'

bit 3-0: **DLC3:DLC0**: Data Length Code

REGISTER 2-11: RXMSIDH - ACCEPTANCE FILTER MASK STANDARD IDENTIFIER HIGH

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3*
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0: **SID10:SID3**: Standard Identifier

* If OPTREG2.MTYPE = 1, then SID3 is forced to zero.

REGISTER 2-12: RXMSIDL - ACCEPTANCE FILTER MASK STANDARD IDENTIFIER LOW

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDE	—	EID17	EID16
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-5: **SID2:SID0**: Standard Identifier
Standard messages, bits = b'000'
Extended messages, bits = SID2:SID0

bit 4: **Unimplemented:** Read as '0'

bit 3: **EXIDE**: Extended Identifier Enable
1 = Apply filter to RXFnSIDL.EXIDE (filter applies to standard **or** extended message frames depending on filter bit)
0 = Do not apply filter to RXFnSIDL.EXIDE (filter will be applied to both standard **and** extended message frames)

bit 2: **Unimplemented:** Read as '0'

bit 1-0: **EID17:EID16:** Extended Identifier

REGISTER 2-13: RXMEID8 - ACCEPTANCE FILTER MASK EXTENDED IDENTIFIER MID

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0: **EID15:EID8**: Extended Identifier

REGISTER 2-14: RXMEID0 - ACCEPTANCE FILTER MASK EXTENDED IDENTIFIER LOW

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-3: **EID7:EID3**: Extended Identifier

bit 2-0: **EID2:EID0**: Extended Identifier (always reads as 0)

REGISTER 2-15: RXFNSIDH - ACCEPTANCE FILTER N STANDARD IDENTIFIER HIGH

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3*
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0: **SID10:SID3**: Standard Identifier

* If OPTREG2.MTYPE = 1 then SID3 = X

REGISTER 2-16: RXFNSIDL - ACCEPTANCE FILTER N STANDARD IDENTIFIER LOW

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDE	—	EID17	EID16
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-5: **SID2:SID0**: Standard Identifier
When EXIDE = 0:
SID2:SID0 = b'xxx'
When EXIDE = 1:
SID2:SID0 = as configured

bit 4: **Unimplemented:** Read as '0'

bit 3: **EXIDE**: Extended Identifier Enable
1 = Filter will apply to extended identifier
0 = Filter will apply to standard identifier

bit 2: **Unimplemented:** Read as '0'

bit 1-0: **EID17:EID16**: Extended Identifier

REGISTER 2-17: RXFNEID8 - ACCEPTANCE FILTER N EXTENDED IDENTIFIER MID

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0: **EID15:EID8**: Extended Identifier

REGISTER 2-18: RXFNEID0 - ACCEPTANCE FILTER N EXTENDED IDENTIFIER LOW

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0: **EID7:EID0**: Extended Identifier (always = b'xxx')

REGISTER 2-19: EFLG - ERROR FLAG REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ESCF	RBO	TXBO	TXEP	RXEP	TXWAR	RXWAR	EWARN
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7 **ESCF**: Error state change (for sending Error state message)
1 = An error state change occurred
0 = No error state change

bit 6 **RBO**: Receive buffer overflow
1 = Overflow occurred
0 = No overflow occurred

bit 5: **TXBO**: Transmitter in Bus Off Error State
1 = TEC reaches 256
0 = Indicates a successful bus recovery sequence

bit 4: **TXEP**: Transmitter in Error Passive State
1 = TEC is equal to or greater than 128
0 = TEC is less than 128

bit 3: **RXEP**: Receiver in Error Passive State
1 = REC is equal to or greater than 128
0 = REC is less than 128

bit 2: **TXWAR**: Transmitter in Error Warning State
1 = TEC is equal to or greater than 96
0 = TEC is less than 96

bit 1: **RXWAR**: Receiver in Error Warning State
1 = REC is equal to or greater than 96
0 = REC is less than 96

bit 0: **EWARN**; Either the Receive Error counter or Transmit error counter has reached or exceeded 96 errors'
1 = TEC or REC is equal to or greater than 96 (TXWAR or RXWAR = 1)
0 = Both REC and TEC are less than 96

3.0 USER REGISTERS

3.1 Description

The MCP2502X/5X allows the user to pre-program registers pertaining to CAN module and device configuration into non-volatile EPROM memory. In this way the device is initialized to a default state after power-up. The user registers are transferred to SRAM during the power-up sequence, and many of the registers are able to be accessed via the CAN bus after the device establishes a connection with the bus. In addition, there are 16 user-defined registers that can be used to store information about the part (e.g., serial number, node identifier, etc.). The registers are summarized in Table 3-1.

Note 1: When transferred to RAM, the register addresses are offset by 1Ch. Accessing individual registers using the "Write Register" or "Read Register command requires use of the offset address. Also, see Table 3-2 for information on accessible registers not contained in user EPROM.

2: Do not address locations outside of the user memory map or unexpected results may occur.

TABLE 3-1: USER MEMORY MAP

Address	Name	Description	Address	Name	Description
00h	IOINTEN	Enable inputs for Transmit-On-Change feature	1Bh	RXF0EID0	Acceptance Filter 0, Extended ID LSB
01h	IOINTPO	Defines polarity for I/O or greater than/less than operator for A/D Transmit-On-Change inputs	1Ch	RXF1SIDH	Acceptance Filter 1, Standard ID MSB
02h	GPLAT	General Purpose I/O (GPIO) Register	1Dh	RXF1SIDL	Acceptance Filter 1, Standard ID LSB, Extended ID USB, and Extended ID enable
03h	0xFF	Reserved	1Eh	RXF1EID8	Acceptance Filter 1, Extended ID MSB
04h	OPTREG1	Configuration options, including GPIO pull-up enable, clockout enable and prescaler	1Fh	RXF1EID0	Acceptance Filter 1, Extended ID LSB
05h	T1CON	PWM1 Timer Control Register; contains enable bit, clock prescale and DC LSBs	20h	TXID0SIDH	Transmit Buffer 0, Standard ID MSB
06h	T2CON	PWM2 Timer Control Register; contains enable bits, clock prescale and DC LSBs	21h	TXID0SIDL	Transmit Buffer 0, Standard ID LSB, Extended ID USB, and Extended ID enable
07h	PR1	PWM1 Period Register	22h	TXID0EID8	Transmit Buffer 0, Extended ID MSB
08h	PR2	PWM2 Period Register	23h	TXID0EID0	Transmit Buffer 0, Extended ID LSB
09h	PWM1DCH	PWM1 Duty Cycle (DC) MSBs	24h	TXID1SIDH	Transmit Buffer 1, Standard ID MSB
0Ah	PWM2DCH	PWM2 Duty Cycle (DC) MSBs	25h	TXID1SIDL	Transmit Buffer 1, Standard ID LSB, Extended ID USB, and Extended ID enable
0Bh	CNF1 [3]	CAN module register configures synchronization jump width and baud rate prescaler	26h	TXID1EID8	Transmit Buffer 1, Extended ID MSB
0Ch	CNF2 [3]	CAN module register configures propagation segment, phase segment 1, and determines number of sample points	27h	TXID1EID0	Transmit Buffer 1, Extended ID LSB
0Dh	CNF3 [3]	CAN module register configures phase buffer segment 2, sleep mode	28h	TXID2SIDH	Transmit Buffer 2, Standard ID MSB
0Eh	ADCON0[4]	A/D Control Register; contains enable, conversion rate, channel select bits	29h	TXID2SIDL	Transmit Buffer 2, Standard ID LSB, Extended ID USB, and Extended ID enable
0Fh	ADCON1[4]	A/D Control Register; contains Voltage Reference source, conversion rate and A/D input enable bits	2Ah	TXID2EID8	Transmit Buffer 2, Extended ID MSB
10h	STCON	Scheduled Transmission Control Register	2Bh	TXID2EID0	Transmit Buffer 2, Extended ID LSB
11h	OPTREG2	Configuration options, including Sleep mode, RTR message and error recovery enables	2Ch	ADCMP3H[4]	Analog Channel 3 Compare Value MSB
12h	—	Reserved	2Dh	ADCMP3L[4]	Analog Channel 3 Compare Value LSb's
13h	—	Reserved	2Eh	ADCMP2H[4]	Analog Channel 2 Compare Value MSB
14h	RXMSIDH	Acceptance Filter Mask, Standard ID MSB	2Fh	ADCMP2L[4]	Analog Channel 2 Compare Value LSb's
15h	RXMSIDL	Acceptance Filter Mask, Standard ID LSB and Extended ID USB	30h	ADCMP1H[4]	Analog Channel 1 Compare Value MSB
16h	RXMEID8	Acceptance Filter Mask, Extended ID MSB	31h	ADCMP1L[4]	Analog Channel 1 Compare Value LSb's

1: GPDDR is mapped to 1Fh is SRAM and not offset by 1Ch.
2: User memory (35h-44h) is not transferred to RAM on power-up and can only be accessed via "Read User Mem" commands.
3: Cannot be modified from initial programmed values.
4: Unimplemented on MCP2502X devices and read 0x00 (exception, ADCON1 = 0x0F)

Address	Name	Description	Address	Name	Description
17h	RXMEID0	Acceptance Filter Mask, Extended ID LSB	32h	ADCMP0H[4]	Analog Channel 0 Compare Value MSB
18h	RXF0SIDH	Acceptance Filter 0, Standard ID MSB	33h	ADCMP0L[4]	Analog Channel 0 Compare Value LSb's
19h	RXF0SIDL	Acceptance Filter 0, Standard ID LSB, Extended ID USB, and Extended ID enable	34h	GPDDR[1]	General Purpose I/O Data Direction Register
1Ah	RXF0EID8	Acceptance Filter 0, Extended ID MSB	35-44h	USER[0:F][2]	User Defined Bytes (0-15)

1: GPDDR is mapped to 1Fh is SRAM and not offset by 1Ch.
2: User memory (35h-44h) is not transferred to RAM on power-up and can only be accessed via "Read User Mem" commands.
3: Cannot be modified from initial programmed values.
4: Unimplemented on MCP2502X devices and read 0x00 (exception, ADCON1 = 0x0F)

TABLE 3-2: ACCESSIBLE RAM REGISTERS NOT IN THE EPROM MAP

Addr*	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value on POR	Value on RST
1Fh**	GPDDR	—	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0	-111 1111	-111 1111
18h	EFLG	ESCF	RBO	TXBO	TXEP	RXEP	TXWAR	RXWAR	EWARN	0000 0000	0000 0000
19h	TEC	Transmit Error Counters								0000 0000	0000 0000
1Ah	REC	Receive Error Counters								0000 0000	0000 0000
50h	ADRES3H	AN3.9	AN3.8	AN3.7	AN3.6	AN3.5	AN3.4	AN3.3	AN3.2	xxxx xxxx	uuuu uuuu
51h	ADRES3L	AN3.1	AN3.0	—	—	—	—	—	—	xx-- ----	uu-- ----
52h	ADRES2H	AN2.9	AN2.8	AN2.7	AN2.6	AN2.5	AN2.4	AN2.3	AN2.2	xxxx xxxx	uuuu uuuu
53h	ADRES2L	AN2.1	AN2.0	—	—	—	—	—	—	xx-- ----	uu-- ----
54h	ADRES1H	AN1.9	AN1.8	AN1.7	AN1.6	AN1.5	AN1.4	AN1.3	AN1.2	xxxx xxxx	uuuu uuuu
55h	ADRES1L	AN1.1	AN1.0	—	—	—	—	—	—	xx-- ----	uu-- ----
56h	ADRES0H	AN0.9	AN0.8	AN0.7	AN0.6	AN0.5	AN0.4	AN0.3	AN0.2	xxxx xxxx	uuuu uuuu
57h	ADRES0L	AN0.1	AN0.0	—	—	—	—	—	—	xx-- ----	uu-- ----

* These addresses are used when using the "Write Register" or "Read Register" command (i.e., no offset).

** The GPDDR register is not offset to RAM the same as the other registers in the EPROM map. This register is transfered to 1Fh on power-up

4.0 DEVICE OPERATION

4.1 Power-Up Sequence

The following sections describe the events/actions of the MCP2502X/5X during normal power-up and operation.

4.1.1 POWER ON RESET

The MCP2502X/5X goes through a sequence of events at power-on reset (POR) in order to load the programmed configuration and insure that errors are not introduced on the bus. During this time, the device is prevented from generating a low condition on the TXCAN pin. The TXCAN pin must remain high from power-on until the device goes 'on bus'.

Operational Mode at Power On

The MCP2502X/5X initially powers up in 'configuration' mode. While in this mode, the MCP2502X/5X will be prevented from sending or receiving messages via the CAN interface. The ADC and PWM peripherals are disabled while in this mode.

Self Configuration

Once the MCP2502X/5X is out of reset it will perform a self configuration. This is accomplished by transferring the contents of the EPROM array to the corresponding locations within the SRAM array. In addition, the checksum of the data written to SRAM will be compared to a pre-programmed value as a test of valid data.

Going On Bus

Once the self configuration cycle has successfully completed, the MCP2502X/5X switches to 'Listen-only' mode where it will remain until an error free CAN message is detected. This is done to ensure that the device is at the correct bus rate for the system.

After the device detects an error free message, it waits for CAN bus idle before switching to 'Normal' mode. This prevents it from going 'on bus' in the middle of another node's transmission and generating an error frame.

Alternately, the MCP2505X may directly enter 'Normal' mode (without first entering Listen-only Mode) after completing its self configuration. This is configured by the user via a control bit (OPTREG2.PUNRM).

Once the MCP2502X/5X enters 'Normal' mode, it is ready to send/receive messages via the CAN interface. At this point the ADC and PWM peripherals are operational (if enabled).

Scheduled Transmissions

After the MCP2502X/5X has gone 'on bus' it will transmit the 'On Bus' message once regardless of whether enabled or not. This message notifies the network of the MCP2502X/5X's presence. The 'On Bus' message will (if enabled STCON.STEN) repeat at a frequency determined by the STCON register (Register 4-1).

This message can also be configured to send the "Read A/D Register" data bytes along with the predefined identifier in TXID2 by setting STCON.STMS = 1.

Note:	The first "On Bus" message sent after powerup will NOT send the "Read A/D Register" data bytes regardless of the STCON.STMS value.
Note:	If the MCP2502X/5X enters SLEEP mode, the scheduled transmissions will cease until the device wakes up again. This implies that SLEEP mode has priority over scheduled transmissions.

4.2 Message Functions

The MCP2502X/5X uses the global mask (RXMASK) along with the two filters (RXF0 and RXF1) and two receive buffers (RB0 and RB1) to determine if a received message should be acted upon. There are 16 functions that can be performed by the MCP2502X/5X based upon received messages (see Table 4-1).These functions allow the device to not only be accessed for Information Request/Input/Output operations, but also to be reconfigured via the CAN bus if necessary.

4.3 Message Types

There are three types of messages that are used to implement the functions of Table 4-1.

1. Information Request Messages (IRM) - Received by the MCP2502X/5X.
2. Output Messages - Transmitted from the MCP2502X/5X as a response to IRMs.
3. Input Messages - Received by the MCP2502X/5X. Used to modify registers.

Note:	'Information Request Messages' (IRMs) and 'Input' messages are both input messages to the MCP2502X/5X. IRMs are received into receive buffer 0 and 'Input' messages are received into receive buffer 1. This must be taken into account while configuring the acceptance filters.

4.3.1 INFORMATION REQUEST MESSAGES

Information Request Messages (IRM) are messages that the MCP2502X/5X receives into Receive Buffer 0 (matches Filter 0) and then responds to by transmitting a message (Output message) containing the requested data.

IRMs can be implemented as either a Remote Transfer Request (RTR) or a Data Frame message by configuring the MTYPE bit in the OPTREG2 register.

TABLE 4-1: MESSAGE FUNCTION

Name	Description
Read A/D Registers	Transmits a single message containing the current state of the analog and I/O registers including the configuration
Read Control Registers	Transmits several control registers not included in other messages
Read Configuration Registers	Transmits the contents of many of the configuration registers
Read CAN error states	Transmits the error flag register and the error counts
Read PWM Configuration	Transmits the registers associated with the PWM modules
Read User Registers 1	Transmits a the values in bytes 0 - 7 of the user memory
Read User Registers 2	Transmits a the values in bytes 8 -15 of the user memory
Read Register*	Transmits a single byte containing the value in an addressed user memory register
Write Register	Uses a mask to write a value to an addressed register
Write TX Message ID0 (TXID0)	Writes the identifiers to a specified value
Write TX Message ID1 (TXID1)	Writes the identifiers to a specified value
Write TX Message ID2 (TXID2)	Writes the identifiers to a specified value
Write I/O Configuration Registers	Writes specified values to the three IOCON registers
Write RX Mask	Changes the receive mask to the specified value
Write RX Filter0	Changes the specified filter to the specified value
Write RX Filter1	Changes the specified filter to the specified value

*The Read Register command is available when using extended message format only. Not available with standard message format.

4.3.1.1 RTR Message Type

When RTR message types are selected (OPTREG2.MTYPE) and a node in the system wants information from the MCP2502X/5X, it has to send a Remote Frame on the bus. The Identifier for the remote frame must be such that it will be accepted through the MCP2502X/5X's mask/filter process (using RXF0). The RTR message type (remote frames) is the default configuration (MTYPE bit = 0).

Information Request "RTR" messages must not only meet the RXMASK/RXF0 criteria but must also have the RTR bit of the CAN ID *set* (since the filter registers do not contain an explicit RTR bit). If a message passes the mask/filter process and the RTR bit is a '0' that message will be ignored.

Once the MCP2502X/5X has received a remote frame it will determine the function to be performed based upon the three LSb's (RXB0SIDL.SID2:SID0 for standard messages and RXB0EID0.EID2:EID0 for extended messages) of the received Remote Frame.

In addition, a predefined Data Length Code (DLC) must be sent to signify the number of data bytes that the MCP2502X/5X must return in it's output message (see Table 4-2 and Table 4-3).

4.3.1.2 Data Frame Message Type

When a non-RTR (or Data Frame) message type is selected and a node in the system wants information from the MCP2502X/5X, it sends an Information Request in the form of a Data Frame. The Identifier for this request must be such that it will be accepted through the MCP2502X/5X's mask/filter process (using RXF0).

Information Request messages in the data frame format must not only meet the RXMASK/RXF0 criteria but must also have the RTR bit of the CAN ID *cleared* (since the filter registers do not contain an explicit RTR bit). If a message passes the mask/filter process and the RTR bit is a '1', that message will be ignored.

Once the MCP2502X/5X has received a data frame Information Request, it will determine the function to be performed based upon the three LSb's (RXB0SIDL.SID2:SID0 for standard messages and RXB0EID0.EID2:EID0 for extended messages) of the received Data Frame. Also, Bit 3 of the received message ID must be set to a '1'.

In addition, the Data Length Code (DLC) must be set to a zero. Refer to Table 4-2 and Table 4-3 for more information.

Regardless of the message format, all messages except the 'Read Register' message can use either standard or extended identifiers. The 'Read Register' message has one additional requirement that it must be an extended identifier. This is discussed in more detail in a later section.

4.3.2 OUTPUT MESSAGES

The Data Frame that is sent in response to the Information Request message is defined as an 'Output' message.

If the data fame is in response to a **remote frame** it will have the same identifier (standard or extended) and contain the same number of data bytes specified by the DLC of the remote frame (per the CAN 2.0B specification).

Note: If the DLC of the incoming remote frame differs from the message definitions summarized in Table 4-2 and Table 4-3, the resulting Output message will limit itself to the erroneous DLC that was received (to maintain compliance with the Bosch CAN specification). The output message will concatenate the number of data bytes for an erroneous DLC that is less than the defined number. For an erroneous DLC that is greater than the defined number, the MCP2502X/5X will extend the number of data bytes, with the data value of the last defined data byte being repeated in the extra bytes in the data field.

If the Output message is in response to a **Data Frame** the lower three LSb's of the identifier (standard or extended) must be the same as the received message, as well as the upper seven MSb's in the case of a standard identifier, or the upper 25 MSb's in the case of an extended identifier. Bit 3 of a standard or extended identifier of the output message will differ from the received Information Request message in that the value equals one for an "IRM" and equals zero for the resulting "Output Message".

Output messages contain the requested data (in the data field). For example: The Information Request message 'Read CAN Error' is a Remote Transmit Request received by the MCP2502X/5X with a DLC of 3. The responding Output Message will return a data frame that contains the same identifier (standard or extended) as the receive message. The accompanying data bytes will contain the values of the predefined GPIO registers and related control/status registers, as shown in Table 4-2 and 4-3.

4.3.3 INPUT MESSAGES

Input messages are received into receive buffer 1 and are used to change the values of the pre-defined groups of registers. There is also an Input message that can change a single register's contents. The primary purpose of Input messages are to reconfigure MCP2502X/5X parameters (if needed) while in an operating CAN system and are therefore optional in system implementation. These messages are in the form of standard or extended data frames (per the CAN 2.0B specification) that have identifiers which pass the MCP2502X/5X's mask/filter process (using RXF1). After passing the mask and filter, the lower three bits of the standard identifier (RXF1SIDL.SID2:SID0) will indicate which register(s) are to be written. The values for the register(s) are contained in the data byte registers as defined in Table 4-2.

Note: If using more than one controlling node, the MCP2502X/5X must be set up to accept "Input Messages" with different identifiers to avoid possible message collisions in the DLC or data bytes if transmitted at the same time.

Note 1: IRMs can theoretically be sent by more than one controlling node because the message is a predefined constant and destructive collisions will not occur.

2: The number of data bytes in an input message must match the DLC number as defined in Table 4-2 and Table 4-3. If the user specifies and transmits an input message with a DLC that is less than the required number of data bytes, the MCP25020 will operate on corrupted data for the bytes that it did not receive and unknown results will occur.

4.4 Dynamic Message Handling

The design insures that transmit and receive messages are handled properly for variable bus loading conditions and different transmit and receive combinations.

4.4.1 MESSAGE ACCEPTANCE/ REJECTION

Messages that are received and meet the Mask/RXFn criteria are then compared to the requirements for Input messages or IRMs as determined by the filter used to accept the message. If the message meets the requirements of one of the associated Input or Information Request messages, then the appropriate actions for that message function are taken.

4.4.2 RECEIVING MULTIPLE MESSAGES

The MCP2502X/5X can only receive and process one message at a time. While the MCP2502X/5X should have ample time to process any received message before another is completely received, in the unlikely event that a second message is received before the first message is finished processing, the second message will be lost.

However, the MCP2502X/5X has the ability to notify the network if a message is lost. Transmit Message ID1 (TXID1) can be configured to transmit a message if a receive overflow occurs (OPTREG2.CAEN = 0).

4.4.3 TRANSMIT MESSAGE PRIORITY

There is a priority for all transmit messages including TXIDn and all "Output" messages.

The transmit message priority is as follows:

1. "Output" messages have the highest priority. Prioritization of the individual "output" message types is determined by the three bits that determine message type, with the lowest value having the highest priority (e.g., "Read A/D Regs" is a higher priority than "Read Control Regs").
2. TXID2 (Transmit auto-converted messages) has the second highest priority.

3. TXID1 (Command Acknowledge) has the third highest priority.
4. TXID0 (On Bus message) has the lowest priority.

In the event two or more messages are pending transmission, but not actually transmitting, transmit message prioritization will occur and the highest message type will be sent first. Messages that are currently transmitting will not be prioritized.

TABLE 4-2: COMMAND MESSAGES (STANDARD IDENTIFIER)

Information Request Messages (to MCP2502X/5X)																															
	Standard ID																Data Bytes														
	10	9	8	7	6	5	4	3	2	1	0	RTR	IDE	DLC																	
Read A/D Regs	x	x	x	x	x	x	x	*	0	0	0	1*	0	1	0	0	0	8*	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a						
Read Control Regs	x	x	x	x	x	x	x	*	0	0	1	1*	0	0	1	1	1	7*	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a						
Read Config Regs	x	x	x	x	x	x	x	*	0	1	0	1*	0	0	1	0	1	5*	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a						
Read CAN Error	x	x	x	x	x	x	x	*	0	1	1	1*	0	0	0	1	1	3*	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a						
Read PWM Config	x	x	x	x	x	x	x	*	1	0	0	1*	0	0	1	1	0	6*	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a						
Read User Mem (bank1)	x	x	x	x	x	x	x	*	1	0	1	1*	0	1	0	0	0	8*	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a						
Read User Mem (bank 2)	x	x	x	x	x	x	x	*	1	1	0	1*	0	1	0	0	0	8*	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a						

Output Messages (from MCP2502X/5X)																															
	Standard ID																Data Bytes														
	10	9	8	7	6	5	4	3	2	1	0	RTR	IDE	DLC																	
Read A/D Regs	x	x	x	x	x	x	x	*	0	0	0	0	0	1	0	0	0	8	IOINTFL	GPIO	AN0H	AN1H	AN10L	AN2H	AN3H	AN23L						
Read Control Regs	x	x	x	x	x	x	x	*	0	0	1	0	0	0	1	1	1	7	ADCON0	ADCON1	OPTREG1	OPTREG2	STCON	IOINTEN	IOINTPO	n/a						
Read Config Regs	x	x	x	x	x	x	x	*	0	1	0	0	0	0	1	0	1	5	DDR	GPIO	CNF1	CNF2	CNF3	n/a	n/a	n/a						
Read CAN Error	x	x	x	x	x	x	x	*	0	1	1	0	0	0	0	1	1	3	EFLG	TEC	REC	n/a	n/a	n/a	n/a	n/a						
Read PWM Config	x	x	x	x	x	x	x	*	1	0	0	0	0	0	1	1	0	6	PR1	PR2	T1CON	T2CON	PWM1DCH	PWM2DCH	n/a	n/a						
Read User Mem (bank1)	x	x	x	x	x	x	x	*	1	0	1	0	0	1	0	0	0	8	USERID0	USERID1	USERID2	USERID3	USERID4	USERID5	USERID6	USERID7						
Read User Mem (bank 2)	x	x	x	x	x	x	x	*	1	1	0	0	0	1	0	0	0	8	USERID8	USERID9	USERID10	USERID11	USERID12	USERID13	USERID14	USERID15						

Input Messages** (to MCP2502X/5X)																															
	Standard ID																Data Bytes														
	10	9	8	7	6	5	4	3	2	1	0	RTR	IDE	DLC																	
Write Register	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	1	1	3	addr	mask	value	n/a	n/a	n/a	n/a	n/a						
Write TX Message ID 0	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	0	4	TX0SIDH	TX0SIDL	TX0EID8	TX0EID0	n/a	n/a	n/a	n/a						
Write TX Message ID 1	x	x	x	x	x	x	x	x	0	1	0	0	0	0	1	0	0	4	TX1SIDH	TX1SIDL	TX1EID8	TX1EID0	n/a	n/a	n/a	n/a						
Write TX Message ID 2	x	x	x	x	x	x	x	x	0	1	1	0	0	0	1	0	0	4	TX2SIDH	TX2SIDL	TX2EID8	TX2EID0	n/a	n/a	n/a	n/a						
Write I/O Configuration	x	x	x	x	x	x	x	x	1	0	0	0	0	0	0	1	1	5	IOINTEN	IOINTPO	DDR	OPTREG1	ADCON1	n/a	n/a	n/a						
Write RX Mask	x	x	x	x	x	x	x	x	1	0	1	0	0	0	1	0	0	4	RXMSIDH	RXMSIDL	RXMEID8	RXMEID0	n/a	n/a	n/a	n/a						
Write RX Filter0	x	x	x	x	x	x	x	x	1	1	0	0	0	0	1	0	0	4	RXF0SIDH	RXF0SIDL	RXF0EID8	RXF0EID0	n/a	n/a	n/a	n/a						
Write RX Filter1	x	x	x	x	x	x	x	x	1	1	1	0	0	0	1	0	0	4	RXF1SIDH	RXF1SIDL	RXF1EID8	RXF1EID0	n/a	n/a	n/a	n/a						

* If using non-RTR messages for Information Request Messages (IRM), the RTR bit = 0, DLC bit field = 0, and bit three of the IRM ID = 1. Also, bit three of the Output Message ID = 0. If using RTR messages for IRMs, the RTR bit = 1, DLC bit field = number of bytes in corresponding output message, and bit three of the IRM ID = x (don't care), also, bit three of the Output Message = x (don't care).

** User defined IRM IDs must be different from Input message IDs to avoid message contention between the corresponding Output message and the Input message.

TABLE 4-3: COMMAND MESSAGES (EXTENDED IDENTIFIER)

Information Request Messages (to MCP2502X/5X)

	Standard ID														Extended ID				Data Bytes							
	10	9	8	7	6	5	4	3	2	1	0	RTR	IDE	DLC	17	16	RXBEID8 (8 bits)	RXBEID0 (8 bits)								
Read A/D Regs	x	x	x	x	x	x	x	x	x	x	x	1*	1	1000 8*	x	x	xxxx xxxx	xxxx *000	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Read Control Regs	x	x	x	x	x	x	x	x	x	x	x	1*	1	0111 7*	x	x	xxxx xxxx	xxxx *001	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Read Config Regs	x	x	x	x	x	x	x	x	x	x	x	1*	1	0101 5*	x	x	xxxx xxxx	xxxx *010	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Read CAN Error	x	x	x	x	x	x	x	x	x	x	x	1*	1	0011 3*	x	x	xxxx xxxx	xxxx *011	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Read PWM Config	x	x	x	x	x	x	x	x	x	x	x	1*	1	0110 6*	x	x	xxxx xxxx	xxxx *100	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Read User Mem	x	x	x	x	x	x	x	x	x	x	x	1*	1	1000 8*	x	x	xxxx xxxx	xxxx *101	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Read User Mem (bank	x	x	x	x	x	x	x	x	x	x	x	1*	1	1000 8*	x	x	xxxx xxxx	xxxx *110	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Read Register	x	x	x	x	x	x	x	x	x	x	x	1*	1	0000 1*	x	x	addr	xxxx *111	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

Output Messages (from MCP2502X/5X)

	Standard ID														Extended ID				Data Bytes							
	10	9	8	7	6	5	4	3	2	1	0	RTR	IDE	DLC	17	16	RXBEID8 (8 bits)	RXBEID0 (8 bits)								
Read A/D Regs	x	x	x	x	x	x	x	x	x	x	x	0	1	1000 8	x	x	xxxx xxxx	xxxx *000	IOINTFL	GPIO	AN0H	AN1H	AN10L	AN2H	AN3H	AN23L
Read Control Regs	x	x	x	x	x	x	x	x	x	x	x	0	1	0111 7	x	x	xxxx xxxx	xxxx *001	ADCON0	ADCON1	OPTREG1	OPTREG2	STCON	IOINTEN	IOINTPO	n/a
Read Config Regs	x	x	x	x	x	x	x	x	x	x	x	0	1	0101 5	x	x	xxxx xxxx	xxxx *010	DDR	GPIO	CNF1	CNF2	CNF3	n/a	n/a	n/a
Read CAN Error	x	x	x	x	x	x	x	x	x	x	x	0	1	0011 3	x	x	xxxx xxxx	xxxx *011	EFLG	TEC	REC	n/a	n/a	n/a	n/a	n/a
Read PWM Config	x	x	x	x	x	x	x	x	x	x	x	0	1	0110 6	x	x	xxxx xxxx	xxxx *100	PR1	PR2	T1CON	T2CON	PWM1DCH	PWM2DCH	n/a	n/a
Read User Mem (bank1)	x	x	x	x	x	x	x	x	x	x	x	0	1	1000 8	x	x	xxxx xxxx	xxxx *101	USERID0	USERID1	USERID2	USERID3	USERID4	USERID5	USERID6	USERID7
Read User Mem (bank	x	x	x	x	x	x	x	x	x	x	x	0	1	1000 8	x	x	xxxx xxxx	xxxx *110	USERID8	USERID9	USERID10	USERID11	USERID12	USERID13	USERID14	USERID15
Read Register	x	x	x	x	x	x	x	x	x	x	x	0	1	0000 1	x	x	addr	xxxx *111	value	n/a	n/a	n/a	n/a	n/a	n/a	n/a

Input Messages (to MCP2502X/5X)

	Standard ID														Extended ID				Data Bytes							
	10	9	8	7	6	5	4	3	2	1	0	RTR	IDE	DLC	17	16	RXBEID8 (8 bits)	RXBEID0 (8 bits)								
Write Register	x	x	x	x	x	x	x	x	x	x	x	0	1	0011 3	x	x	xxxx xxxx	xxxx x000	addr	mask	value	n/a	n/a	n/a	n/a	n/a
Write TX Message ID 0	x	x	x	x	x	x	x	x	x	x	x	0	1	0100 4	x	x	xxxx xxxx	xxxx x001	TX0SIDH	TX0SIDL	TX0EID8	TX0EID0	n/a	n/a	n/a	n/a
Write TX Message ID 1	x	x	x	x	x	x	x	x	x	x	x	0	1	0100 4	x	x	xxxx xxxx	xxxx x010	TX1SIDH	TX1SIDL	TX1EID8	TX1EID0	n/a	n/a	n/a	n/a
Write TX Message ID 2	x	x	x	x	x	x	x	x	x	x	x	0	1	0100 4	x	x	xxxx xxxx	xxxx x011	TX2SIDH	TX2SIDL	TX2EID8	TX2EID0	n/a	n/a	n/a	n/a
Write I/O Configuration	x	x	x	x	x	x	x	x	x	x	x	0	1	0101 5	x	x	xxxx xxxx	xxxx x100	IOINTEN	IOINTPO	DDR	OPTREG1	ADCON1	n/a	n/a	n/a
Write RX Mask	x	x	x	x	x	x	x	x	x	x	x	0	1	0100 4	x	x	xxxx xxxx	xxxx x101	RXMSIDH	RXMSIDL	RXMEID8	RXMEID0	n/a	n/a	n/a	n/a
Write RX Filter0	x	x	x	x	x	x	x	x	x	x	x	0	1	0100 4	x	x	xxxx xxxx	xxxx x110	RXF0SIDH	RXF0SIDL	RXF0EID8	RXF0EID0	n/a	n/a	n/a	n/a
Write RX Filter1	x	x	x	x	x	x	x	x	x	x	x	0	1	0100 4	x	x	xxxx xxxx	xxxx x111	RXF1SIDH	RXF1SIDL	RXF1EID8	RXF1EID0	n/a	n/a	n/a	n/a

* If using non-RTR messages for Information Request Messages (IRM), the RTR bit = 0, DLC bit field = 0, and bit three of the IRM ID = 1. Also, bit three of the Output Message ID = 0.
If using RTR messages for IRMs, the RTR bit = 1, DLC bit field = number of bytes in corresponding output message, and bit three of the IRM ID = x (don't care), also, bit three of the Output Message = x (don't care).

** User defined IRM IDs must be different from Input message IDs to avoid message contention between the corresponding Output message and the Input message.

4.5 Automatic Transmission

The MCP2502X/5X can automatically initiate four different message types to indicate the following situations:

- Edge Detected on a digital input (TXID2)
- Threshold exceeded on an analog input (TXID2)
- Error condition (Read Error “Output” Message)
- Scheduled Transmissions (TXID0)

The buffers have an implied transmit priority where buffer two is highest and buffer 0 is the lowest. Therefore, multiple message buffers can be requested for transmission and each one will be sent in order of priority.

4.5.1 DIGITAL INPUT EDGE DETECTION

Each GPIO pin that has been configured as a digital input can be individually configured to automatically transmit a message when a defined edge occurs as explained in the GPIO module section. When transmitting this message, the MCP2502X/5X uses **TXID2**. The DLC is set to two and the first two bytes of the ‘Read A/D Registers’ (IOINTFL and GPIO) are sent.

4.5.2 ANALOG INPUT THRESHOLD DETECTION

Each GPIO pin that has been configured as an analog input can be individually configured to automatically transmit a message when a threshold is exceeded as described in the Analog-to-Digital Converter Module section. The MCP2502X/5X sends **TXID2** when transmitting this message. The DLC is set to eight and the eight bytes of the ‘Read A/D Registers’ are sent.

Note:	The GPIO register that is sent with the message (data byte 2) can be ignored if there are no digital inputs enabled for ‘Change-of-State’ as it contains no useful information for the ‘Analog Input Threshold Detect’ function.

4.5.2.1 Hysteresis Function

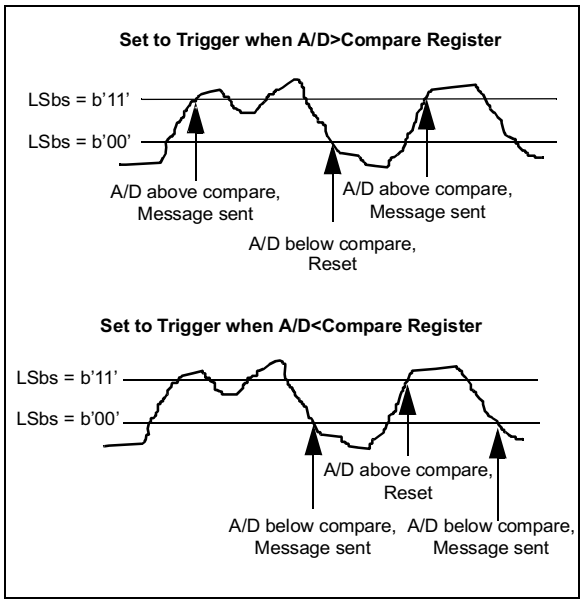
This function is automatic and will insure that an analog value that is on the compare edge (i.e., toggling LSb) does not fill the CAN bus with continuous A/D message transmissions.

The hysteresis uses the two LSb’s of the compare register. These two bits are forced bits and are not configurable by the user. They will be forced to either b’00’ or b’11’ depending on the compare polarity. If configured for A/D result > compare register, the automatic transmission will occur when the A/D value is greater than or equal to b’nnnn nnnn 11’ and reset when less than or equal to b’nnnn nnnn 00’. The opposite conditions must occur if the compare polarity is set for A/D result < compare register.

A hysteresis example:

- The user sets the upper eight bits of the 10-bit compare register (ADCMP0H). The lower two bits of the compare register are not configurable by the user and are forced to either b’11’ or b’00’ depending on the polarity of the compare threshold (i.e., transmit is triggered above or below the compare value via the IOINTPO register).
- The user sets the polarity of the compare threshold (IOINTPO). In this example, the threshold is set for triggering a message on an A/D > compare register. The two LSb’s are forced to b’11’.
- When the A/D conversion exceeds the compare register (b’nnnn nnnn 11’), an automatic transmission will occur once.
- In order for the automatic transmission to occur again, the A/D value must first drop below the compare register b’nnnn nnnn 00’ and then back above the compare register b’nnnn nnnn 11’.

FIGURE 4-1: HYSTERESIS FUNCTION



4.5.3 ERROR CONDITION

The MCP2502X/5X can be configured to automatically transmit a message whenever one or more of the following error conditions occur:

- Receiver has entered error warning state
- Receiver has entered error passive state
- Transmitter has entered error warning state
- Transmitter has entered error passive state
- A Receive Buffer has overflowed

If the Error Condition message is enabled (OPTREG2.TXONE = 1) and one of the above conditions occur, the MCP2502X/5X sends TXID1 identifier with ‘Output’ message ‘Read CAN Error States’ data field (three data bytes).

4.5.4 SCHEDULED TRANSMISSIONS

The MCP2502X/5X has the capability of sending scheduled transmissions (on bus message) if enabled.

The scheduled transmission control register (STCON) enables and configures the occurrence of the scheduled message. Setting the STEN bit in the STCON register enables the scheduled message. The STBF1:STBF0 and STM3:STM0 bits allow a scheduled transmission to be initiated from a minimum of 256 µs to a maximum of 16.8 seconds (using a 16 MHz FOSC) and the following equation:

Scheduled Transmission
= STBF1:STBF0(STM3:STM0)

Message Type - The message sent for scheduled transmissions consists of either **TXID0** with zero data bytes or **TXID0** with eight data bytes containing the "Read A/D Regs" message, depending on STMS bit in the STCON register.

Note: The actual scheduled transmission intervals may vary slightly due to the internal event que of the control module.

REGISTER 4-1: STCON - SCHEDULED TRANSMISSION CONTROL REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
STEN	STMS	STBF1	STBF0	STM3	STM2	STM1	STM0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7 **STEN:** Scheduled Transmission Enable
1 = Enabled
0 = Disabled

bit 6 **STMS:** Scheduled transmission message select
1 = Sends Transmit ID 0 (TXID0) with the "Read A/D Regs" data (DLC = 8)
0 = Sends Transmit ID 0 (TXID0) with no data (DLC = 0)

bit 5:4 **STBF1:STBF0:** Base Transmission Frequency
00 = 4096TOSC
01 = 16•(4096TOSC)
10 = 256•(4096TOSC)
11 = 4096•(4096TOSC)
(e.g., STBF1:STBF0 => 00 => 256 µs for a 16 MHz FOSC)

bit 3:0 **STM3:STM0:** Scheduled Transmission Multiplier
0000 = 1
0001 = 2
:
:
1110 = 15
1111 = 16

TABLE 4-4: REGISTERS ASSOCIATED WITH THE CAN MODULE

Addr	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value on POR	Value on RST
0Bh	CNF1	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	xxxx xxxx	uuuu uuuu
0Ch	CNF2	BTLM-ODE	SAM	PHSEG12	PHSEG11	PHSEG10	PRSEG2	PRSEG1	PRSEG0	xxxx xxxx	uuuu uuuu
0Dh	CNF3	—	WAKF	—	—	—	PHSEG22	PHSEG21	PHSEG20	-x-- xxxx	-u-- uuuu
10h	STCON	STEM	STMS	STBF1	STBF0	STM3	STM2	STM1	STM0	0xxx xxxx	0uuu uuuu
11h	OPTREG2	CAEN	ERRE	TXONE	SLPEN	MTYPE	PDEFEN	PUSLP	PUNRM	0000 0000	uuuu uuuu
14h	RXMSIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	uuuu uuuu
15h	RXMSIDL	SID2	SID1	SID0	—	—	—	EID17	EID16	xxx- --xx	uuu- --uu
16h	RXMEID8	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	uuuu uuuu
17h	RXMEID0	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	uuuu uuuu
18h	RXF0SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	uuuu uuuu
19h	RXF0SIDL	SID2	SID1	SID0	—	—	—	EID17	EID16	xxx- --xx	uuu- --uu
1Ah	RXF0EID8	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	uuuu uuuu
1Bh	RXF0EID0	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	uuuu uuuu
1Ch	RXF1SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	uuuu uuuu
1Dh	RXF1SIDL	SID2	SID1	SID0	—	—	—	EID17	EID16	xxx- --xx	uuu- --uu
1Eh	RXF1EID8	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	uuuu uuuu
1Fh	RXF1EID0	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	uuuu uuuu
20h	TXB0SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	uuuu uuuu
21h	TXB0SIDL	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxx- x-xx	uuu- u-uu
22h	TXB0EID8	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	uuuu uuuu
23h	TXB0EID0	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	uuuu uuuu
24h	TXB1SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	uuuu uuuu
25h	TXB1SIDL	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxx- x-xx	uuu- u-uu
26h	TXB1EID8	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	uuuu uuuu
27h	TXB1EID0	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	uuuu uuuu
28h	TXB2SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	uuuu uuuu
29h	TXB2SIDL	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxx- x-xx	uuu- u-uu
2Ah	TXB2EID8	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	uuuu uuuu
2Bh	TXB2EID0	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	uuuu uuuu

5.0 GPIO MODULE

5.1 Description

The MCP2502X/5X has eight general purpose input/output (GPIO) pins (GP0 to GP7) collectively labeled GPIO. All GPIO port pins have TTL input levels and full CMOS output drivers, with the exception of GP7, which is input only. Pins GP6:GP0 can be individually configured as input or output via the GPDDR register.

Note:	The GPDDR register controls the direction of the GPIO pins, even when they are being used as analog inputs. The user must ensure that the bits in the GPDDR register are maintained ***set*** (input) when using them as analog inputs.

Each of the GPIO pins has a weak internal pull-up resistor. A single control bit (OPTREG.$\overline{GPPU}$) can turn on/off all the pull-ups. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled during a Power-on Reset.

All of the pins are multiplexed with an alternate function, including analog-to-digital conversion on up to four of the GPIO pins, analog V_{REF} inputs on up to two pins, PWM outputs on up to two pins, clock out function, and external reset. The operation of each pin is selected by clearing or setting control bits in various control registers. GPIO pin functions are summarized in Table 5-1.

TABLE 5-1: GPIO FUNCTIONS

Name	Bit#	Function
GP0/AN0	bit0	I/O or analog input
GP1/AN1	bit1	I/O or analog input
GP2/AN2/PWM2	bit2	I/O, analog input, or PWM out
GP3/AN3/PWM3	bit3	I/O, analog input, or PWM out
GP4/VREF-	bit4	I/O or analog voltage reference
GP5/VREF+	bit5	I/O or analog voltage reference
GP6/CLKOUT	bit6	I/O or Clock output
GP7/nRST/VPP	bit7	Input, external reset input, or programming voltage input

5.2 Digital Edge Detection

All GPIO pins have a "Digital Edge Detection" feature that will automatically transmit a message when an edge with the proper polarity occurs on any of the digital inputs. Only pins configured as inputs and enabled for this function via control register IOINTPO will perform this operation.

Note:	Refer to Section 7.4, "A/D Transmit-on-change Function" for information with respect to A/D channels.

Three control registers are associated with this function. An enable pin for each GPIO pin resides in the IOINTEN register. When a bit is set to a '1', the corresponding GPIO pin is enabled to generate a transmit-on-change message (TXID2) when an edge of specified polarity occurs.

The "Digital Edge Detection" function on a GPIO pin configured as a digital input is ***edge triggered***. A rising edge will generate a transmission if the corresponding bit in the IOINTPO register is ***set***, or a falling edge will generate a transmission if the bit is ***cleared***. When a valid edge appears on the enabled GPIO pin, CAN message TXID2 is initiated.

Theedge detectionfunction on any given GPIO pin (configured as a digital input) can wake up the processor from SLEEP if the corresponding interrupt enable bit in the IOINTEN register was set prior to going into SLEEP mode. If a wake up from SLEEP is caused in this manner, the device will immediately initiate a transmit message (TXID2).

REGISTER 5-1: GPDDR - DATA DIRECTION REGISTER

U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7 **Unimplemented**

bit 6-0 **DDR<6:0>**: data direction register*
1 = corresponding GPIO pin is configured as an input
0 = corresponding GPIO pin is configured as an output
* must bet set if corresponding analog channel is enabled (see ADCON1)

REGISTER 5-2: GPLAT - GPIO OUTPUT REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	GP6	GP5	GP4	GP3	GP2	GP1	GP0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7 **Unimplemented**

bit 6-0 **GP<6:0>**: GPIO
1 = corresponding GPIO pin output latch is a '1'
0 = corresponding GPIO pin output latch is a 0

REGISTER 5-3: IOINTEN REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP7TXC	GP6TXC	GP5TXC	GP4TXC	GP3TXC	GP2TXC	GP1TXC	GP0TXC
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0 **GP7TXC:GP0TXC** - Transmit-on-change Enable
1 = Enable Transmit-On-Change/Compare For Corresponding GPIO/AN Channel
0 = Disable Transmit-On-Change/Compare For Corresponding GPIO/AN Channel

REGISTER 5-4: IOINTPO REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP7POL	GP6POL	GP5POL	GP4POL	GP3POL	GP2POL	GP1POL	GP0POL
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0 **GP7POL:GP0POL** - Transmit-on-change Polarity
1 = Digital Inputs: Low to High Transition On Corresponding GPIO Input Pin Generates a transmit message
Analog Inputs: A/D result above compare value generates a transmit message
0 = Digital Inputs: High to Low Transition On Corresponding GPIO Input Generates transmit message
Analog Inputs: A/D result below compare value generates a transmit message

REGISTER 5-5: IOINTFL REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
GP7TXF	GP6TXF	GP5TXF	GP4TXF	GP3TXF	GP2TXF	GP1TXF	GP0TXF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0 **GP7TXF:GP0TXF** - Transmit-on-change Polarity
1 = Digital Inputs: A valid edge has occurred on the digital input
Analog Inputs: A/D result does exceed the compare threshold
0 = Digital Inputs:A valid edge has not occurred on the digital input
Analog Inputs: A/D result does not exceed the compare threshold

Register 5-6: OPTREG1 Register

R/W-1	R/W-1	R/W-1	R/W-1	U-0	R/W-0	R/W-0	R/W-0
$\overline{\text{GPPU}}$	$\overline{\text{CLKEN}}$	CLKPS1	CLKPS0	—	CMREQ	AQT1	AQT0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7 **$\overline{\text{GPPU}}$:** Weak pullup enable
1 = Weak pullups disabled
0 = Weak pullups enabled (GP7:GP0)

bit 6 **$\overline{\text{CLKEN}}$:**
1 = Clock Out Function disabled
0 = Clock Out Function enabled

bit 5:4 **CLKPS1:CLKPS0:** CLKOUT prescaler
00 = Fosc/1
01 = Fosc/2
10 = Fosc/4
11 = Fosc/8

bit 3 **Reserved**:

bit 2 **CMREQ**: Requests mode of operation (allows mode changes via the CAN bus)
1 = Requests "Listen Only" mode
0 = Requests "Normal" mode *

bit 1:0 **AQT1:AQT0**: Analog acquisition time
00 = 64Tosc
01 = 2•(64Tosc)
10 = 4•(64Tosc)
11 = 8•(64Tosc)
(e.g., AQT1:AQT0 => 00 => 2.56 µs for a 25 MHz Fosc)

* CMREQ must be cleared as default to avoid device entering Listen Only mode on first "Input" message.

Register 5-7: OPTREG2 Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAEN	ERREN	TXONEN	SLPEN	MTYPE	PDEFEN	PUSLP	PUNRM
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7 **CAEN -** Command acknowledge enable
1 = Enables the "Command Acknowledge" message (TXID1)
0 = Enables the "Receive Overflow" message (TXID1)

bit 6 **ERREN**: Error recovery enable
1 = MCP2502X/5X will recover into Listen Only mode from bus off
0 = MCP2502X/5X will recover into Normal mode from bus-off

bit 5 **TXONEN: T**ransmit on error condition (REC or TEC)
1 = Enable, will send message if error counter(s) go high enough
0 = Disable, will NOT send message regardless of error counter values

bit 4 **SLPEN:** Low power SLEEP mode enable/disable
1 = Device will enter Sleep if bus is idle for at least 1408 bit times
0 = SLEEP mode is disabled

bit 3 **MTYPE**: Determines if "Information Request Messages" use RTR or not
1 = RTR is NOT used for IRM (Data Frame)
0 = RTR is used for IRM (Remote Frame)

bit 2 **PDEFEN**: Enables PWM outputs to return to POR default values when CAN bus communication is lost
1 = Enables PWM output default values
0 = Disables PWM output default values

bit 1 **PUSLP**: Allows device to enter SLEEP while in Listen Only mode during power-up sequence
1 = Enables SLEEP when in Listen Only mode during power-up sequence
0 = Disables SLEEP when in Listen Only mode during power-up sequence

bit 0 **PUNRM**: Enters "Normal" mode after completing self-configuration during power-up sequence
1 = Enters "Normal" mode after completing self-configuration during power-up sequence
0 = Enables "Listen Only" mode after completing self-configuration during power-up sequence and waits for an error-free message before switching to Normal mode

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO MODULE

Addr	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value on POR	Value on $\overline{RST}$
Bank 0											
34h	GPDDR	—	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0	-111 1111	-111 1111
00h	IOINTEN	GP7TXC	GP6TXC	GP5TXC	GP4TXC	GP3TXC	GP2TXC	GP1TXC	GP0TXC	0000 0000	0000 0000
01h	IOINTPO	GP7POL	GP6POL	GP5POL	GP4POL	GP3POL	GP2POL	GP1POL	GP0POL	0000 0000	0000 0000
04h	OPTREG1	$\overline{GPPU}$	CLKEN	CLKPS1	CLKPS0	—	CMREQ	AQT1	AQT0	0000 ----	0000 ----

Legend: x = unknown, U = unchanged, - = unimplemented read as '0'. Shaded cells are not used by module

6.0 PWM MODULE

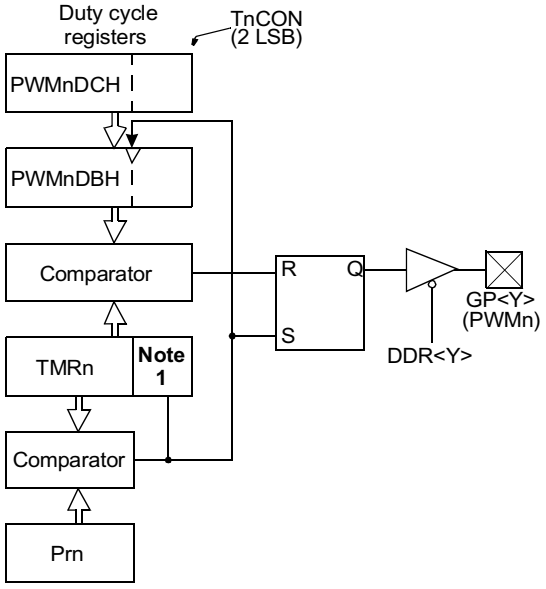
6.1 Description

There are two Pulse Width Modulation (PWM) modules, PWM1 and PWM2, that generate up to a 10-bit resolution output signal on GP2 and GP3, respectively. Each of these outputs can be separately enabled, and each has its own associated timer, duty cycle, and period registers for controlling the PWM output shape.

Each PWM module contains a set of master/slave Duty Cycle registers, providing up to a 10-bit resolution PWM output. Figure 6-1 shows a simplified block diagram of the PWM module. A PWM output has a time base (period) and a time that the output stays high (duty cycle), as shown in Figure 6-2. The frequency of the PWM is the inverse of the period (1/period).

At power on, the PWM outputs are not enabled until after the self configuration sequence has been completed (i.e., all SRAM registers have been loaded with their default values) to prevent invalid signals from occurring on the PWM outputs.

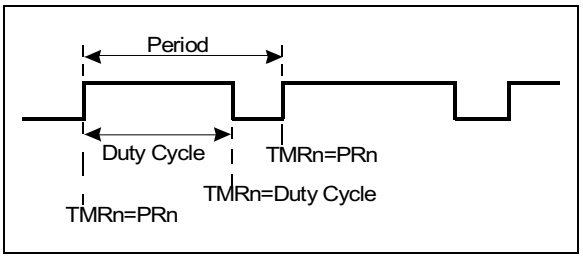
FIGURE 6-1: SIMPLIFIED BLOCK DIAGRAM



Note 1: 8-bit timer is concatenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time-base

The PWM outputs can be forced to their default POR conditions if CAN bus communication is lost, and is enabled via OPTREG2.PDEFEN. The system designer must implement a “hand shaking” protocol, such that the MCP2505X will receive a valid message into one of the receive buffers before four successive scheduled transmissions occur. If a valid message is not received, the PWM outputs, GP2 and GP3 will automatically reconfigure to their default conditions. This includes the PWM module itself being disabled and the GPIO being forced low, high, or tri-state.

FIGURE 6-2: PWM OUTPUT



6.2 PWM Timer Modules

There are two 8-bit timers supporting the two PWM outputs. Both timers have a prescaler only. The timers are readable and writable, and are cleared on any device reset or when the timer is turned off.

The input clock (Fosc/4) has a prescale option of 1:1, 1:4, or 1:16, selected by control bits TnCKPS[1:0] in register TnCON<5:4> (where n corresponds to the appropriate timer).

Each timer module has an 8-bit period register, PRn. The timer module increments from 00h until it matches PRn and then resets to 00h on the next increment cycle. PRn is a readable and writable register. The PRn register is set when the device is reset.

Each timer can be shut off by clearing control bit TMRnON (TnCON<7>).

6.2.1 TIMER MODULE PRESCALER

The prescaler counters are cleared when a write to the TnCON or TMRn register or any device reset ($\overline{RST}$ reset or Power-on reset) occurs.

6.3 PWM Modules

Each PWM module contains a set of master/slave Duty Cycle registers, providing up to a 10-bit resolution PWM output. Figure 6-2 shows a simplified block diagram of the PWM module.

6.3.1 PWM PERIOD

The PWM period is specified by writing to the PRn register. The PWM period can be calculated using the following formula:

$$PWM\ period = [(PR_n) + 1] * 4T_{OSC} * (TMRn\ prescale\ value)$$

$$PWM\ frequency = 1/(PWM\ period)$$

When TMRn is equal to PRn, the following two events occur on the next cycle:

- TMRn is cleared
- The PWM duty cycle is latched from PWMnDCH into PWMnDBH

6.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the PWMnDCH and TnCON registers. Up to 10-bit resolution is available, the PWMnDCH contains the eight MSb's and the TnCON register contains the two LSb's. This 10-bit value is represented by PWM1DCH:T1CON<1:0> for PWM Module 1 and PWM2DCH:T2CON<1:0> for PWM Module 2.

The following equation is used to calculate the PMW duty cycle:

$$PWMDC = (PWMnDC) * T_{OSC} * TMRn\ (prescale)$$

PWMnDCH can be written to at any time, but the duty cycle value is not latched into PWMnDBH until after a match between PRn and TMRn occurs (i.e., the period is complete).

The PWMnDBH register and 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitch-less PWM operation.

When the PWMnDBH and 2-bit latch match TMRn concatenated with an internal 2-bit Q clock or 2 bits of the TMRn prescaler, the PWM output pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency =

$$log((F_{OSC})/(Fpwm))/(log(2)bits)$$

Note:	If the PWM duty cycle value is longer than the PWM period (PWM duty cycle = 100%), the PWM output pin will not be cleared.

In order to achieve higher resolution, the PWM frequency must be decreased. In order to achieve higher PWM frequency, the resolution must be decreased. Table 6-1 lists example PWM frequencies and resolutions for Fosc = 20 MHz. TMRn prescaler and PRn values are also shown.

TABLE 6-1: PWM FREQUENCIES AND RESOLUTIONS AT 20 MHZ

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.30 kHz	208.30 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PRn Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	5.5

REGISTER 6-1: PWM1 DUTY CYCLE REGISTER MSB (PWM1DCH)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
DC1B9	DC1B8	DC1B7	DC1B6	DC1B5	DC1B4	DC1B3	DC1B2
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0 **DC1B7:DC1B2**: Most Significant PWM0 Duty Cycle Bits

REGISTER 6-2: PWM2 DUTY CYCLE REGISTER MSB (PWM2DCH)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
DC2B9	DC2B8	DC2B7	DC2B6	DC2B5	DC2B4	DC2B3	DC2B2
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7-0 **DC2B7:DC2B2**: Most Significant PWM2 Duty Cycle Bits

REGISTER 6-3: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-x	R/W-x
TMR1ON	—	T1CKPS1	T1CKPS0	—	—	DC1B1	DC1B0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7 **TMR1ON**: Timer1 On bit
1 = Enables Timer1
0 = Disables Timer1

bit 6 **Unimplemented**: Read as '0'

bit 5:4 **T1CKPS1:T1CKPS0**: Timer1 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

bit 3:2 **Unimplemented**: Read as '0'

bit 1:0 **DC1B1:DC1B0**: Least Significant PWM1 Duty Cycle bits

REGISTER 6-4: T2CON: TIMER2 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-x	R/W-x
TMR2ON	—	T2CKPS1	T2CKPS0	—	—	DC2B1	DC2B0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7 **TMR2ON**: Timer2 On bit
1 = Enables Timer2
0 = Disables Timer2

bit 6 **Unimplemented**: Read as '0'

bit 5:4 **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

bit 3:2 **Unimplemented**: Read as '0'

bit 1:0 **DC2B1:DC2B0**: Least Significant PWM2 Duty Cycle bits

REGISTER 6-5: PR1: PERIOD REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PR1B7	PR1B6	PR1B5	PR1B4	PR1B3	PR1B2	PR1B1	PR1B0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7:0 **PR1B7:PR1B0**: PWM1 Period Register

REGISTER 6-6: PR2: PERIOD REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PR2B7	PR2B6	PR2B5	PR2B4	PR2B3	PR2B2	PR2B1	PR2B0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7:0 **PR2B7:PR2B0**: PWM2 Period Register

REGISTER 6-7: PWM1DCH: PWM1 DUTY CYCLE UPPER EIGHT BITS

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
DC1B9	DC1B8	DC1B7	DC1B6	DC1B5	DC1B4	DC1B3	DC1B2
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7:0 **DC1B9:DC1B2**: PWM1 Upper Eight Bits of the Duty Cycle

REGISTER 6-8: PWM2DCH: PWM2 DUTY CYCLE UPPER EIGHT BITS

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
DC2B9	DC2B8	DC2B7	DC2B6	DC2B5	DC2B4	DC2B3	DC2B2
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7:0 **DC2B9:DC2B2**: PWM2 Upper Eight Bits of the Duty Cycle

TABLE 6-2: REGISTERS ASSOCIATED WITH THE PWM MODULE

Addr	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value on POR	Value on RST
34h	GPDDR	—	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0	-111 1111	-111 1111
05h	T1CON	TMR1ON	—	T1CKPS1	T1CKPS0	—	—	DC1B1	DC1B0	0-00 --xx	0-00 --uu
06h	T2CON	TMR2ON	—	T2CKPS1	T2CKPS0	—	—	DC2B1	DC2B0	0-00 --xx	0-00 --uu
07h	PR1	Timer 1 Module's Period Register								1111 1111	1111 1111
08h	PR2	Timer 2 Module's Period Register								1111 1111	1111 1111
09h	PWM1DCH	DC1B9	DC1B8	DC1B7	DC1B6	DC1B5	DC1B4	DC1B3	DC1B2	xxxx xxxx	uuuu uuuu
0Ah	PWM2DCH	DC2B9	DC2B8	DC2B7	DC2B6	DC2B5	DC2B4	DC2B3	DC2B2	xxxx xxxx	uuuu uuuu

Legend: x = unknown, U = unchanged, - = unimplemented read as '0'. Shaded cells are not used by module

7.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

7.1 Description

The Analog-to-Digital (A/D) module is a four channel, 10-bit successive approximation type of A/D. The A/D allows conversion of an analog input signal to a corresponding 10-bit number. The four channels are multiplexed on the GP[3:0] pins. The converter is turned off/on via the ADCON0 register and each channel is individually enabled via the ADCON1 control register. The V_{REF}+ and V_{REF}- sources are user selectable, as internal or external. Each channel can be set to one of two conversion modes:

1. Auto-conversion or
2. Convert-on-request.

7.2 A/D Module Registers

The A/D module itself has several registers. The registers are:

- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- Transmit-on-Change Register (IOINTEN)
- Compare and Polarity Register (ADCMPnL)
- A/D Result Registers (ADRESnL, ADRESnH)

The ADCON0 register controls the operation of the A/D module, including autoconversion rate and enable bit. The ADCON1 register enables the A/D function on port pins GP3:GP0, A/D conversion rate, and selects the voltage reference source. The IOINTEN register's four least significant bits enable/disable the transmit-on-change function. The ADCMPnL.ADPOL bit sets the polarity (above or below threshold) for the transmit-on-change function.

The result of an A/D conversion is made available to the user within the data field of the "Read A/D Registers" Output Message via the CAN bus. This message can be directly requested by another CAN node or automatically transmitted (TXIDO) as described in another section.

Additionally, the individual channel results may be read using the "Read Register" command as described in Table 4.3.1 and as shown in Table 3-2 by addressing the appropriate A/D result register (ADRESnL and ADRESnH).

Note:	The GPDDR register controls the direction of the GPIO pins, even when they are being used as analog inputs. The user must ensure that the bits in the GPDDR register are maintained ***set*** (input) when using them as analog inputs.

7.3 A/D Conversion Modes

There are two modes of conversion that can be individually selected for each analog channel that has been enabled. These are auto-conversion and conversion-on-request.

7.3.1 AUTO-CONVERSION MODE

If the auto-conversion mode is selected (STCON), an A/D conversion is performed sequentially for each channel that has been set to analog input mode and has been configured for auto-conversion mode. Conversion starts with AN0 and is immediately followed by AN1, etc. After the conversion has been completed, the value is stored in the Analog Channel registers for the respective channel.

The rate of the auto-conversion is determined by an 8-bit timer and prescaler. Typical conversion rates with a 20 MHz oscillator input are shown in Table 7-1.

TABLE 7-1: AUTO-CONVERSION RATES FOR GIVEN PRESCALE RATES AT 20 MHZ

TMR0PS[2:0]	Prescale Rate	Auto-Conversion Rate
000	1:32	51 µs
001	1:64	410 µs
010	1:128	2 ms
011	1:256	7 ms
100	1:512	26 ms
101	1:1024	52 ms
110	1:2048	105 ms
111	1:4096	210 ms

The timer is turned on if one of the GPnTXC bits are set in the IOINTEN register and configured as analog input.

The prescaler counter is cleared when the device is reset ($\overline{RST}$ reset or Power-on reset).

7.3.2 CONVERSION-ON-REQUEST MODE

If the conversion-on-request mode is selected, the device performs an A/D conversion only after receiving a "Read A/D Registers" or "Read Register" receive message. In the case of the "Read A/D Registers" command, all of the GPIO pins that have been configured as analog input channels will have an A/D conversion done before the data frame is sent. When a "Read Register" receive message is initiated, the A/D conversion is performed when the MSB of the analog channel is requested, with the MSB result being transferred. A subsequent read of the LSB will transmit the value latched when the MSB was requested (it is recommended that the "Read A/D Registers" receive message is used to obtain complete analog channel values

in one message).

7.4 A/D Threshold Detection

Once an A/D auto-conversion has been completed, the A/D channel result(s) can be compared to a value stored in the associated A/D channel comparator registers.

If the value in the analog channel result registers (i.e., AN0L and AN10H registers for analog channel 0) is lower or higher than the value in the A/D comparator registers (as specified by a corresponding polarity bit), then a "transmit-on-change" message will be sent (TXID2). The threshold detection function for all analog channels are bit selectable.

If the A/D channel has been configured for transmit-on-change mode, then the MCP2505 will send a Transmit Message with the appropriate data. It is possible that more than one A/D channel has a change-of-state condition. This does not pose a problem since all analog channel data is provided in the transmit message.

REGISTER 7-1: A/D MODULE RESULT REGISTER MSB (ADRESNH)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7:0 **AD9:AD2** - Most Significant A/D Result

REGISTER 7-2: A/D MODULE RESULT REGISTER LSB (ADRESNL)

R/W-x	R/W-x	U-0	U-0	U-0	U-0	U-0	U-0
AD1	AD0	—	—	—	—	—	—
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7:4 **AD1:AD0** - Least significant A/D result

bit 5:0 Unimplemented (Reads as 0)

REGISTER 7-3: A/D MODULE COMPARE REGISTER MSB (ADCMPNH)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
ANnCMP9	ANnCMP8	ANnCMP7	ANnCMP6	ANnCMP5	ANnCMP4	ANnCMP3	ANnCMP2
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7:0 **ANnCMP9:ANnCMP2** - Most Significant A/D Compare

REGISTER 7-4: A/D MODULE COMPARE REGISTER LSB (ADCMPNL)

R/W-x	R/W-x	U-0	U-0	U-0	U-0	U-0	U-0
ANnCMP1	ANnCMP0	—	—	—	—	—	—
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7:6 **ANnCMP1:ANnCMP0** - Least Significant A/D Compare

bit 5:0 Unimplemented (Reads as 0)

REGISTER 7-5: ADCON0 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-x	U-0	U-x	U-x
ADON	T0PS2	T0PS1	T0PS0	—	—	—	—
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7 **ADON**: A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shut off and consumes no operating current

bit 6:4 **T0PS2:T0PS0**: Timer0 Prescaler Rate Select Bits (used for auto conversions)

T0PS2: T0PS0	Prescaler Rate
000	1:32
001	1:64
010	1:128
011	1:256
100	1:512
101	1:1024
110	1:2048
111	1:4096

bit 2 **Unimplemented**: (Reads as 0)

Shaded bits (—) **Reserved**

REGISTER 7-6: ADCON1 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, read as '0'

bit 7:6 **ADCS2:ADCS0**: A/D Conversion Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = Reserved

bit 5:4 **VCFG1:VCFG0**: Voltage Reference Configuration Bits

VCFG1:VCG0	A/D VREF+	A/D VREF-
00	VDD	VSS
01	External VREF+	VSS
10	VDD	External VREF-
11	External VREF+	External VREF-

bit 3:0 **PCFG3:PCFG0**: A/D Port Configuration Control Bits*
1 = Corresponding GPIO pin configured as Digital I/O
0 = Corresponding GPIO pin configured as A/D Input

* corresponding data direction bit (GPDDR register) must be set for each enabled analog channel.

TABLE 7-2: REGISTERS ASSOCIATED WITH THE A/D MODULE

Addr	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value on POR	Value on $\overline{RST}$
1Eh	**GPPIN**	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000	0000 0000
34h	**GPDDR** *	—	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0	-111 1111	-111 1111
00h	**IOINTEN**	GP7TXC	GP6TXC	GP5TXC	GP4TXC	GP3TXC	GP2TXC	GP1TXC	GP0TXC	0000 0000	0000 0000
01h	**IOINTPO**	GP7POL	GP6POL	GP5POL	GP4POL	GP3POL	GP2POL	GP1POL	GP0POL	0000 0000	0000 0000
0Eh	**ADCON0**	ADON	T0PS2	T0PS1	T0PS0	GO/DONE	—	CHS1	CHS0	0000 0-00	0000 0-00
0Fh	**ADCON1**	ADCS1	ADCS0	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	0000 0000	0000 0000
2Ch	**ADCMP3H**	AN3CMP.	AN3CMP.8	AN3CMP.7	AN3CMP.6	AN3CMP.5	AN3CMP.4	AN3CMP.3	AN3CMP2	xxxx xxxx	uuuu uuuu
2Dh	**ADCMP3L**	AN3CMP.	AN3CMP.0	—	—	Reserved			ADPOL	xx-- ----x	uu-- ----u
2Eh	**ADCMP2H**	AN2CMP.	AN2CMP.8	AN2CMP.7	AN2CMP.6	AN2CMP.5	AN2CMP.4	AN2CMP.3	AN2CMP2	xxxx xxxx	uuuu uuuu
2Fh	**ADCMP2L**	AN2CMP.	AN2CMP.0	—	—	Reserved			ADPOL	xx-- ----x	uu-- ----u
30h	**ADCMP1H**	AN1CMP.	AN1CMP.8	AN1CMP.7	AN1CMP.6	AN1CMP.5	AN1CMP.4	AN1CMP.3	AN1CMP2	xxxx xxxx	uuuu uuuu
31h	**ADCMP1L**	AN1CMP.	AN1CMP.0	—	—	Reserved			ADPOL	xx-- ----x	uu-- ----u
32h	**ADCMP0H**	AN0CMP.	AN0CMP.8	AN0CMP.7	AN0CMP.6	AN0CMP.5	AN0CMP.4	AN0CMP.3	AN0CMP2	xxxx xxxx	uuuu uuuu
33h	**ADCMP0L**	AN0CMP.	AN0CMP.0	—	—	Reserved			ADPOL	xx-- ----x	uu-- ----u
10h	STCON	STEM	STMS	STBF1	STBF0	STM3	STM2	STM1	STM0	0xxx xxxx	0uuu uuuu

* The GPDDR register controls the direction of the GPIO pins, even when they are being used as analog inputs. The user must ensure that the bits in the GPDDR register are maintained ***set*** (input) when using them as analog inputs.

8.0 SPECIAL FEATURES OF THE MCP2502X/5X

8.1 Description

There are a number of special circuits in the MCP2502X/5X that deal with the needs of real-time applications. These features are intended to maximize system reliability, minimize cost through elimination of external components, and provide power saving operating modes. These are:

- Oscillator selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- SLEEP
- In-Circuit Serial Programming

Several oscillator options are offered to allow the device to fit the application. XT and HS modes allow the device to support a wide range of crystal frequencies while the LP crystal option saves power.

Two timers are implemented to offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the device in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, transmit-on-change, or CAN bus activity.

A set of configuration bits are used to select various options.

FIGURE 8-1: CRYSTAL/CERAMIC RESONATOR OPERATION

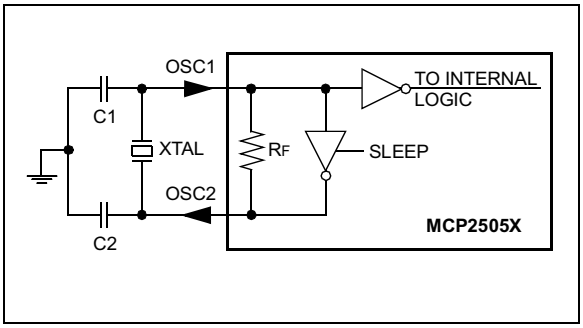
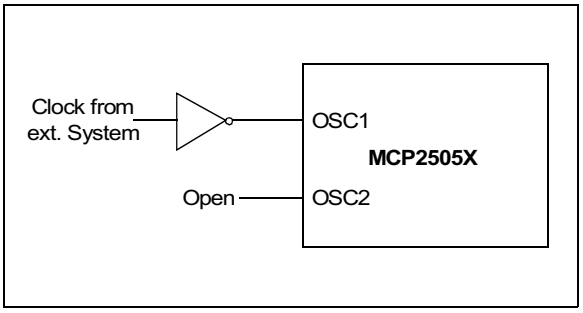


FIGURE 8-2: EXTERNAL CLOCK INPUT OPERATION



8.2 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h. The configuration register is actually beyond program memory space and belongs to the special test/configuration memory space (2000h-3FFFh) which can be accessed only during programming.

8.3 Oscillator Configurations

Four different oscillator modes may be selected. The user can program two configuration bits, $F_{OSC}1$:$F_{OSC}0$ in the CONFIG register to select one of these modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal Resonator

In all modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 8-1). The oscillator design requires the use of a parallel cut crystal. The device can also have an external clock source to drive the OSC1/CLKIN pin (Figure 8-2).

The device will default to HS mode if the CONFIG register is not programmed.

REGISTER 8-1: CONFIGURATION REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W	R/W	R/W
—	—	R	R	R	R	R	R	R	R	R	RSTEN	FOSC1	FOSC0
bit13													bit0

bit 13:11 **Unimplemented**: Read as '0'

bit 10:3 Reserved, do not attempt to modify

bit 2 **RSTEN**: Enable RST input on GP7
1 = $\overline{\text{RST}}$ input Enabled
0 = $\overline{\text{RST}}$ input Disabled

bit 1:0 **$F_{OSC}1:F_{OSC}0$**: Oscillator Selection bits
11 = HS oscillator
10 = Reserved for Test (EC oscillator)
01 = XT oscillator
00 = LP oscillator

8.4 Reset

The MCP2502X/5X differentiates between two kinds of reset:

- Power-on Reset (POR)
- External $\overline{\text{RST}}$ reset

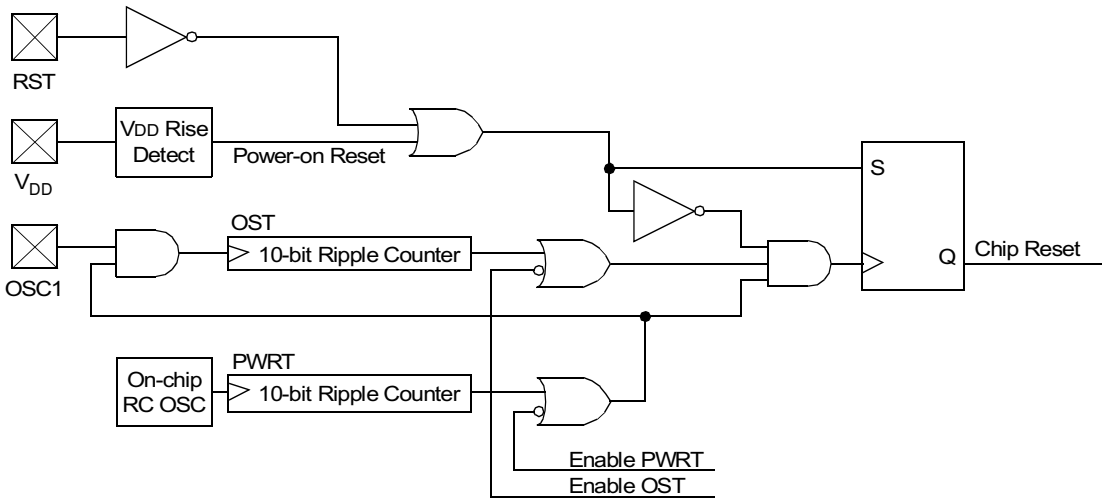
Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), on $\overline{\text{RST}}$, and on $\overline{\text{RST}}$ during SLEEP. They are not affected by a wake-up from SLEEP, which is viewed as the resumption of normal operation. A simplified block diagram of the on-chip reset circuit is shown in Figure 8-3. The MCP2502X/5X has an $\overline{\text{RST}}$ noise filter in the $\overline{\text{RST}}$ reset path. The filter will detect and ignore small pulses.

8.4.1 POWER-ON RESET

A Power-on Reset pulse is generated on-chip when V_{DD} rise is detected (in the range of 1.5V to 2.1V). If the $\overline{\text{RST}}$ input on the GP7 pin is selected, the $\overline{\text{RST}}$ pin may be tied through a series resistor to V_{DD}, eliminating the need for external RC components usually required for a Power-on Reset. A maximum rise time for V_{DD} is specified in the Electrical Specifications section of this document.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure proper operation (for additional information, refer to Application Note AN607, "*Power-up Troubleshooting*").

FIGURE 8-3: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



8.4.2 POWER-UP TIMER

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only, from the POR. The Power-up Timer operates on an internal RC oscillator. The device is kept in reset as long as the PWRT is active. The PWRT's time delay allows V_{DD} to rise to an acceptable level. The power-up time delay will vary from device to device due to V_{DD}, temperature, and process variation. See DC parameters for details.

8.5 Oscillator Start-up Timer

The Oscillator Start-up Timer (OST) provides a 512 oscillator cycle (TOSC) delay after the PWRT delay is complete. This ensures that the crystal oscillator has started and stabilized, and must be less than the total time it takes (704 oscillator cycles or 44TQ) for the minimum standard data frame or remote transmit message to be completed on the CAN bus after a wake-up from SLEEP occurs. The OST time-out is invoked only on Power-on Reset or wake-up from SLEEP.

8.6 Power-down Mode (SLEEP)

Power-down mode, or SLEEP, is enabled via the SLPEN bit in the OPTREG2 register. When enabled, the MCP2502X/5X will enter SLEEP after the CAN bus has been idle for a minimum 1408 bit times while in Normal mode.

In addition, the device may be configured to enter SLEEP while in Listen Only mode immediately after power-up if there is no activity on the CAN bus. Subsequent CAN bus activity will wake the device up from SLEEP, and the NEXT message will be confirmed as a valid message before entering Normal mode. This feature is enabled via the PUSLP bit in the OPTREG2 register.

While in SLEEP, the I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or hi-impedance).

The following operations will not function while the device is in SLEEP:

- A/D Module data conversion
- Auto-conversion mode
- Auto-messaging
- PWM module and outputs
- Clock Output

8.6.1 WAKE-UP FROM SLEEP

The MCP2502X/5X can wake-up from SLEEP through one of the following events:

- External reset input on $\overline{RST}$ pin
- Transmit-on-change due to edge detected on GPIO pin
- Activity detected on CAN bus

For the device to wake-up due to a GPIO transmit-on-change, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit.

If a wake-up from SLEEP is caused by activity on the CAN bus, the message that caused the wake-up will not be received or acknowledged by the MCP2502X/5X.

8.7 In-Circuit Serial Programming

The MCP2502X/5X can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards, with unprogrammed devices, and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the GP4 and GP5 pins low while raising GP7 (VPP) pin from VIL to VIH (see the MCP2502X/5X programming specification, DS20072). GP4 becomes the programming data and GP5 becomes programming clock. Both GP4 and GP5 are Schmitt Trigger inputs in this mode. The signal definitions are summarized in Table 8-1

TABLE 8-1: IN-CIRCUIT SERIAL PROGRAMMING PIN FUNCTIONS

Pin Name	Pin Number	Programming Mode Function
VSS	7	Ground
GP4	8	Data
GP5	9	Clock
GP7	11	VPP
VDD	14	Power

9.0 ELECTRICAL CHARACTERISTICS

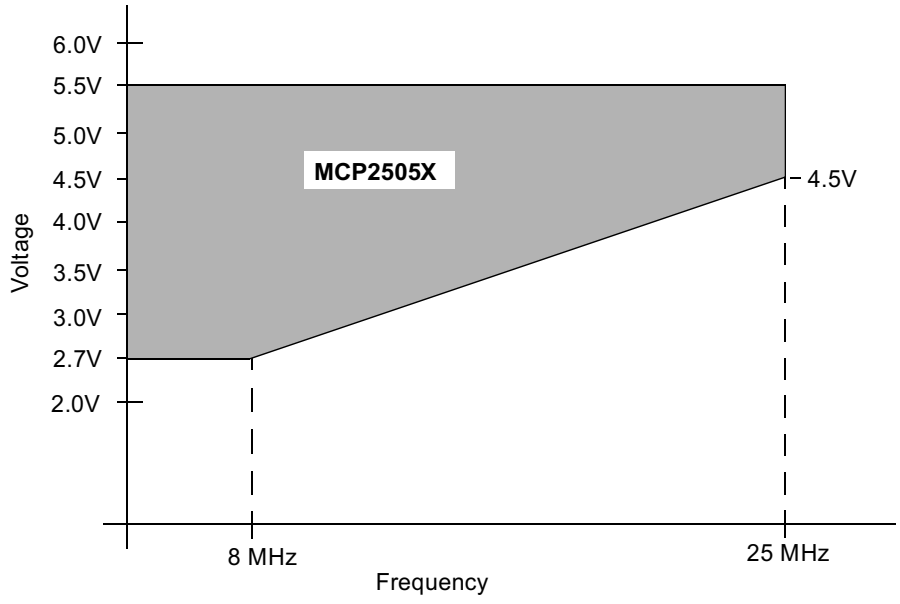
9.1 Absolute Maximum Ratings†

Ambient temperature under bias ..... -55°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with respect to Vss (except V_{DD} and $\overline{RST}$) ..... -0.3V to (V_{DD} + 0.6V)
V_{DD} ..... 0 V to 7.0V
Voltage on $\overline{RST}$ with respect to Vss ..... 0 V to 14V
Total power dissipation (**Note 1**) ..... 1.0 W
Maximum source current out of V_{SS} pin ..... 300 mA
Maximum sink current into V_{DD} pin ..... 250 mA
Input clamp current, Iik (Vi < 0 or Vi > V_{DD}) ..... ±20 mA
Output clamp current, Iok (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum current sunk by any I/O pin ..... 25 mA
Maximum current sourced by any input pin ..... 25 mA
Maximum current sunk by GPIO port ..... 200 mA
Maximum current sourced by GPIO port ..... 200 mA
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins ..... ≥ 3.5 kV

Note 1: Power dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 9-1: MCP2505X VOLTAGE-FREQUENCY GRAPH



Fmax = (9.44 MHz/V) (Vddappmin - 2.7V) + 8 MHz

Note: Vddappmin is the minimum voltage of the **MCP2505X** device in the application. Characterized and not 100% tested.

9.2 DC Characteristics

DC Characteristics			Industrial (I): TAMB = -40°C to +85°C VCC = 2.7V to 5.5V Automotive (E): TAMB = -40°C to +125°C VCC = 4.5V to 5.5V			
Param. No.	**Sym**	**Characteristics**	**Min**	**Max**	**Units**	**Test Conditions**
	VDD	Supply Voltage	2.7 4.5	5.5 5.5	V V	XT and LP OSC configuration HS OSC configuration (**Note 2**)
	SVDD	VDD Rise Rate to ensure internal power-on reset signal	0.05	—	V/ms	**(Note 3)**
		High level input voltage				
	VIH	GPIO pins	2	VDD+0.3	V	
	VIH	RXCAN (Schmitt Trigger)	.7VDD	VDD	V	
		OSC1	.85VDD	VDD	V	
		Low level input voltage		—		
	VIL	RXCAN (Schmitt Trigger)	VSS	0.2VDD	V	
	VIL	GPIO pins	-0.3	0.5V	V	
		OSC1	Vss	0.2VDD	V	
		Low level output voltage				
	VOL	TXCAN GPIO pins	—	0.6	V	IOL = 8.5 mA,VDD = 4.5V
		High level output voltage			V	
	VOH	TXCAN, GPIO pins	VDD -0.7	—	V	IOH =-3.0 mA, VDD = 4.5V, I temp
		Input leakage current				
	ILI	All I/O except OSC1, GP7	-1	+1	µA	
		OSC1, GP7 pin	-5	+5	µA	
	CINT	Internal Capacitance (all inputs and outputs except GP7)	—	7	pF	TAMB = 25°C, fC = 1.0 MHz, VDD = 5.0V (**Note 3**)
		GP7	—	15	pF	
	IDD	Operating Current	—	20	mA	XT OSC VDD = 5.5V; FOSC=25 MHz
	IDDS	Standby Current (CAN Sleep Mode)	—	30	µA	Inputs tied to VDD or VSS

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: Refer to Table 9-1.

3: This parameter is periodically sampled and not 100% tested.

9.3 AC Characteristics

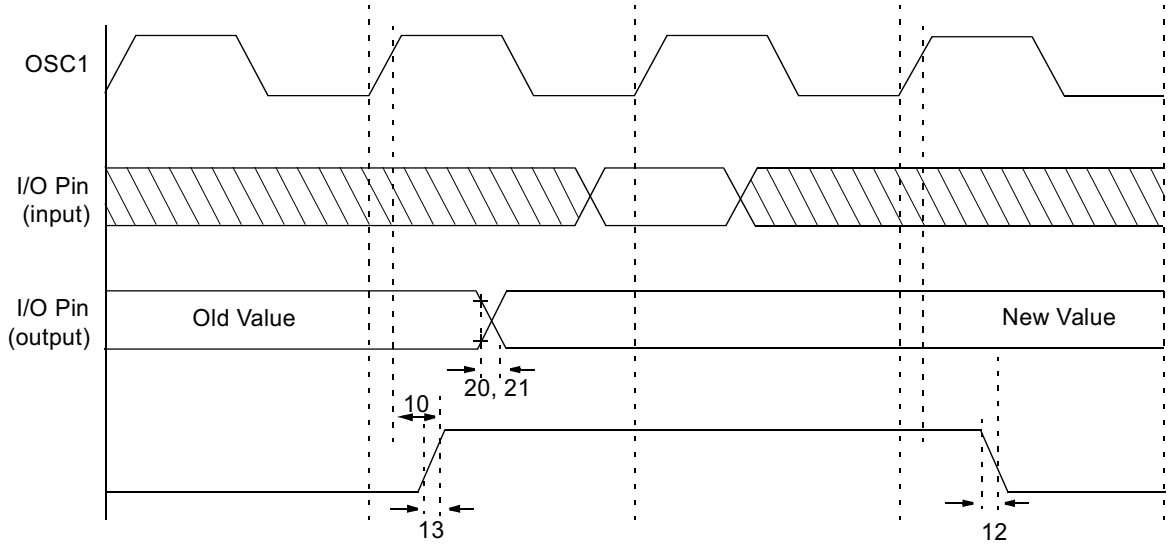
AC Characteristics			Industrial (I): TAMB = -40°C to +85°C VCC = 2.7V to 5.5V Automotive (E):TAMB = -40°C to +125°C VCC = 4.5V to 5.5V			
Param. No.	**Sym**	**Characteristics**	**Min**	**Max**	**Units**	**Test Conditions**
	FOS	CLKIN Frequency	DC	4	MHz	XT osc mode
			DC	25	MHz	HS osc mode (**Note 3**)
			DC	200	kHz	LP osc mode
	FOS	Oscillator Frequency	0.1	4	MHz	XT osc mode
			4	25	MHz	HS osc mode (**Note 3**)
			5	200	kHz	LP osc mode
1	TOSC	CLKIN Period	250	—	ns	XT osc mode
			40	—	ns	HS osc mode
			5	—	µs	LP osc mode
		Oscillator Period	0.25	10	µs	XT osc mode
			40	250	ns	HS osc mode
			5	—	µs	LP osc mode
3	TOSL	CLKIN High or Low Time	100	—	ns	XT osc mode
	TOSH		15	—	ns	HS osc mode
			2.5	—	µs	LP osc mode
4	TOSR	CLKIN Rise or Fall Time	—	25	ns	XT osc mode (**Note 1**)
			—	50	ns	HS osc mode
			—	15	ns	LP osc mode
10	TDCLKOUT	CLKOUT Propagation Delay	—	60	ns	VDD = 4.5 V (**Note 2**)
12	TCKR	CLKOUT Rise Time	—	100	ns	**Note 2**
13	TCKR	CLKOUT Fall Time	—	200	ns	**Note 2**
20	TIOR	Port output rise time	—	40	ns	**Note 1**
21	TIOF	Port output fall time	—	40	ns	**Note 1**
30	TMCL	RST Pulse Low	2	—	µs	VDD= 5V
32	TOST	Oscillation Start-up Timer	512	—	TOSC	TOSC = OSC1 period
33	TPWRT	Power-up Timer	28	132	ms	VDD = 5V
34	TIOZ	I/O Hi-impedance from RST low	—	2.1	µs	
	TPWMR	PWM output rise time	—	25	ns	**Note 1**
	TPWMF	PWM output fall time	—	25	ns	**Note 1**
	TAD	A/D clock period	1.6	—	µs	VREFΔ ≥ 2.5V
			3.0	—	µs	VREF full range
	TCNV	Conversion Time (not including acquisition time)	—	13	TAD	

Note 1: This parameter is periodically sampled and not 100% tested.

2: Measurements are taken with CLKOUT output configured as 4 x TOSC.

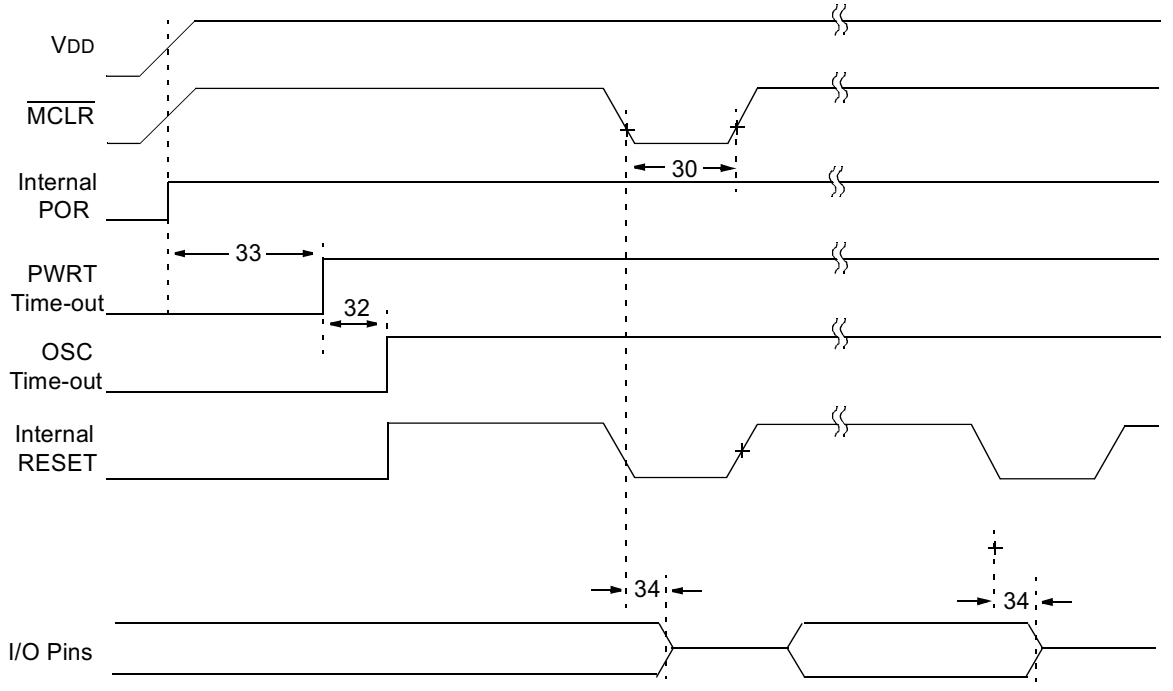
3: Refer to Table 9-1.

FIGURE 9-2: I/O TIMING



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins.

FIGURE 9-3: RESET, OST, AND POWER-UP-TIMER



9.4 A/D Converter Characteristics

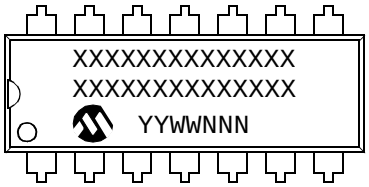
AC Converter Characteristics			Industrial (I): TAMB = -40°C to +85°C VCC = 2.7V to 5.5V Automotive (E): TAMB = -40°C to +125°C VCC = 4.5V to 5.5V			
Param. No.	**Sym**	**Characteristics**	**Min**	**Max**	**Units**	**Test Conditions**
	NR	A/D resolution	—	10-bits		VREF = VDD = 5.12V, VSS ≤ in ≤VREF
	NINT	A/D Integral error	—	less than ±1 LSb		VREF+ = VDD = 5.12V, VSS- = VSS = 0 V (I TEMP)
	NDIF	A/D Differential error	—	less than ±1 LSb		VREF+ = VDD = 5.12V, VSS- = VSS = 0 V (I TEMP)
	NG	A/D Gain error	—	less than ±1 LSb		VREF+ = VDD = 5.12V, VSS- = VSS = 0 V
	NOFF	A/D Offset error	—	less than ±2 LSb		VREF+ = VDD = 5.12V, VSS- = VSS = 0 V
		Monotonicity	—	—		VSS ≤ in ≤VREF
	VREF	Reference Voltage	4.096	VDD+0.3	V	Absolute minimum to ensure 10-bit accuracy.
	VREF+	Reference V high	VREF-	VDD+0.3	V	Minimum resolution for A/D is 1mV.
	VREF-	Reference V low	VSS-0.3	VREF+	V	Minimum resolution for A/D is 1mV.
	VAIN	Analog input V	VREF-	VREF+	V	
	ZAIN	Recommended impedance of analog voltage source	—	2.5	kohm	**Note**
	IREF	VREF input current	—	10	µA	
	NHYS	Analog Transmit-on-change Hysteresis	—	2 LSb		Specified by design (see Section 4.5.2.1)

Note: Design guidance only

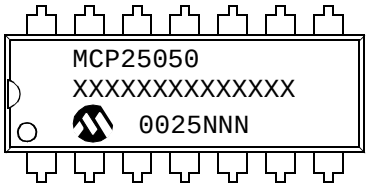
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

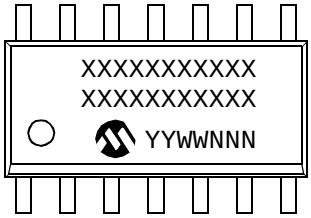
14-Lead PDIP (300 mil)



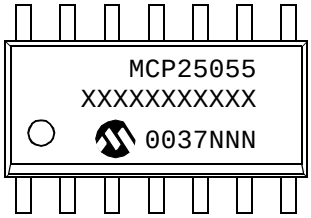
Example:



14-Lead SOIC (208 mil)



Example:

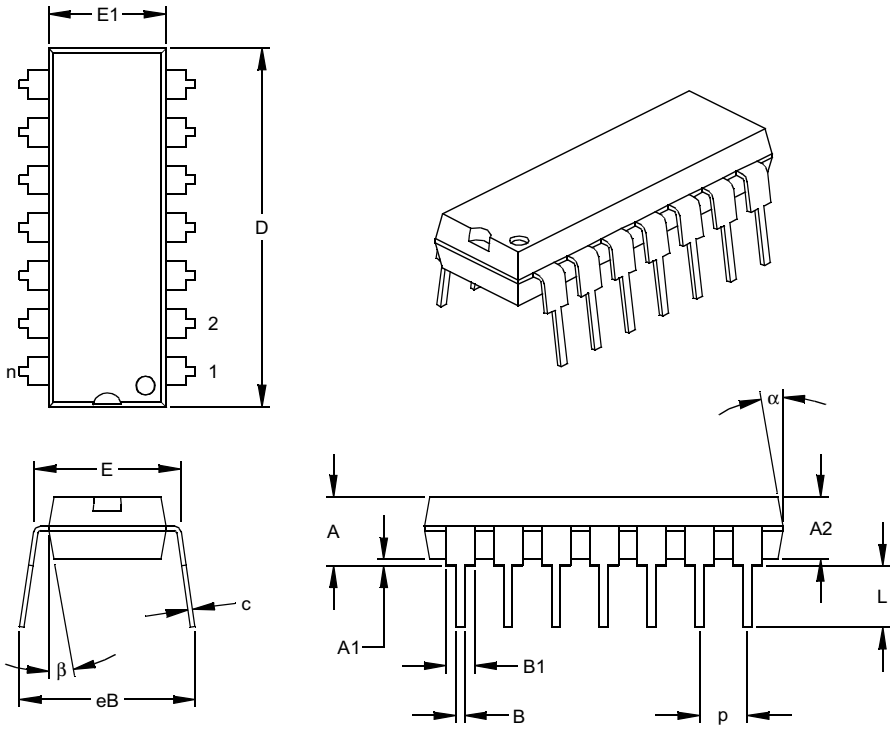


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

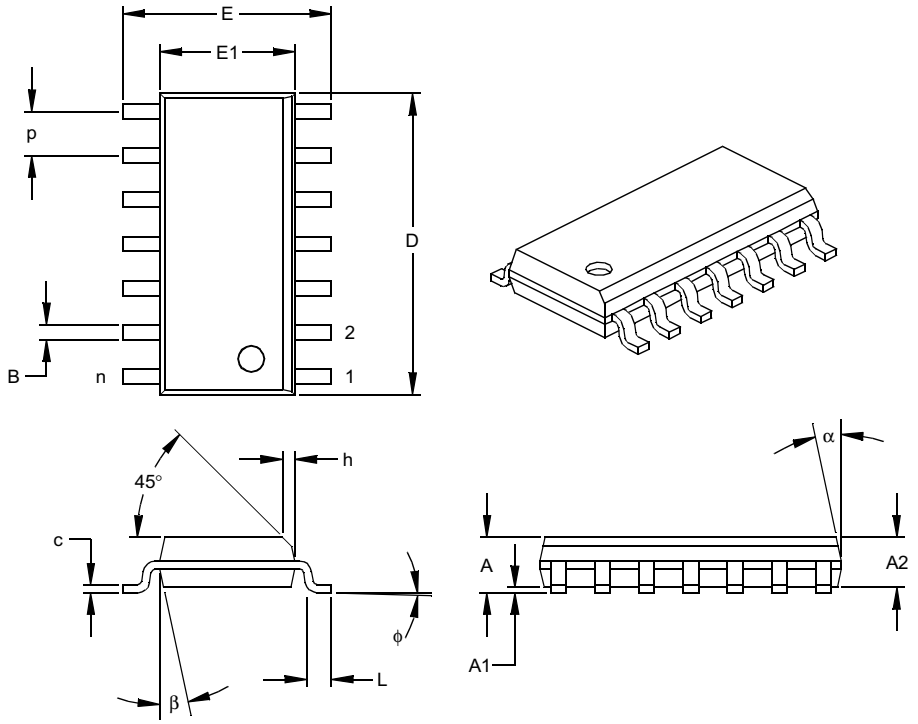
14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

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013001

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Device: **MCP2502X/5X** Literature Number: **DS21664B**

Questions:

1. What are the best features of this document?

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PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	MCP25020:	CAN I/O Expander
	MCP25020T:	CAN I/O Expander (Tape and Reel)
	MCP25025:	CAN I/O Expander
	MCP25025T:	CAN I/O Expander (Tape and Reel)
	MCP25050:	Mixed Signal CAN I/O Expander
	MCP25050T:	Mixed Signal CAN I/O Expander (Tape and Reel)
	MCP25055:	Mixed Signal CAN I/O Expander
	MCP25055T:	Mixed Signal CAN I/O Expander (Tape and Reel)
Temperature Range:	I =	-40°C to +85°C
	E =	-40°C to +125°C (not available on MCP25025 or MCP25055 devices)
Package:	P =	Plastic DIP (300 mil Body), 14-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead

Examples:

a) MCP25020–I/P: Industrial temperature, PDIP package.
b) MCP25025–I/SL: Industrial temperature, SOIC package.
c) MCP25050T-E/SL: Tape and Reel, Extended temperature, SOIC package.
d) MCP25055-I/SL: Industrial temperature SOIC package.

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Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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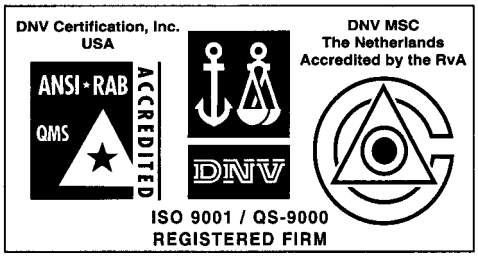

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