TDA 2151

LINEAR INTEGRATED CIRCUIT

LUMINANCE AND CHROMINANCE AMPLIFIER FOR COLOUR TV

The TDA 2151 is a monolithic integrated circuit for CTV receivers that amplifies and controls the luminance and chrominance signals. It is encapsulated in a 16-lead dual in-line plastic package and its main features are:

- No pre-adjustments are needed for DC controls of contrast, brightness and saturation
- Tracked DC contrast control in chrominance and luminance channels
- Beam current limiter acting on contrast and brightness controls
- Programmable contrast reduction at beam current limiter action
- Independent video signal output for driving the sync. separator; this is for VCR playback operation
- Black level of the video output signal thermally compensated
- Generation of a luminance service signal to adjust the CRT cathode bias.

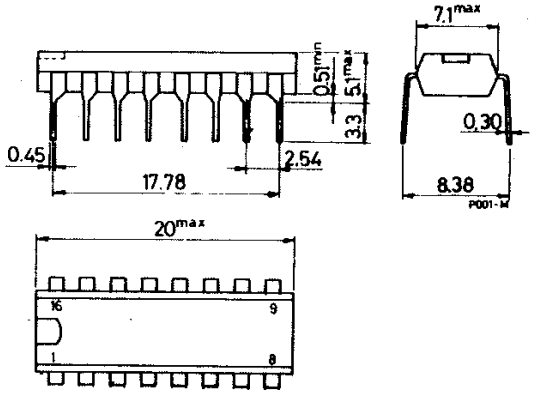
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 11)	15	V
V_1, V_8	Voltages at pin 1 and pin 8	V_s	
P_{tot}	Power dissipation at $T_{amb} \leqslant 70°C$	800	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

ORDERING NUMBER: TDA 2151

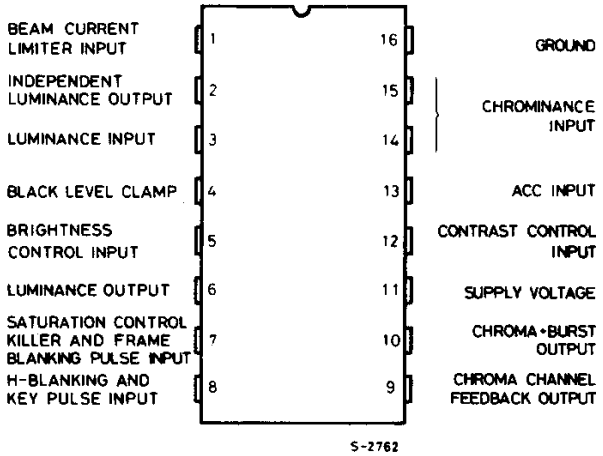
MECHANICAL DATA

Dimensions in mm

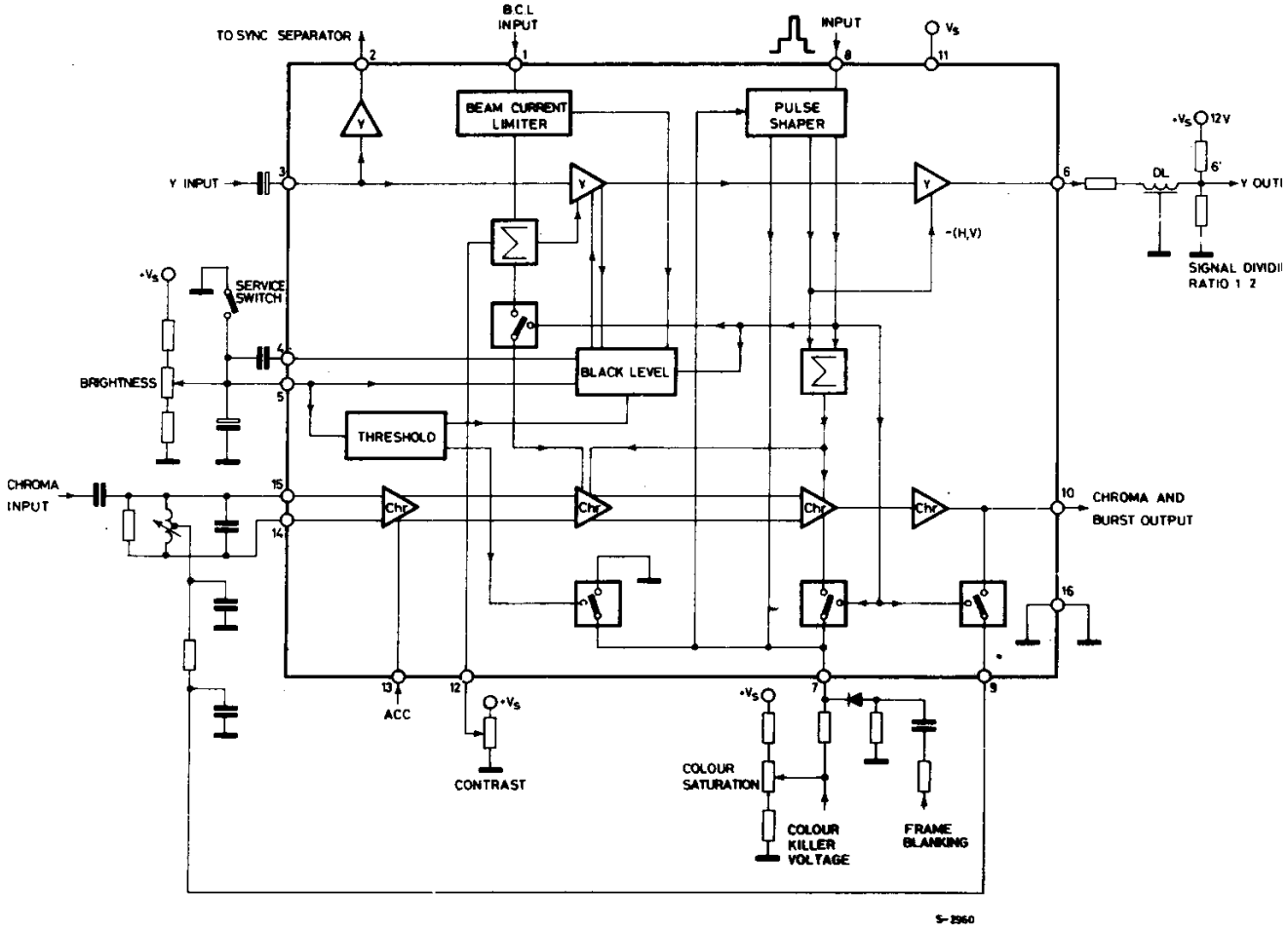


TDA 2151

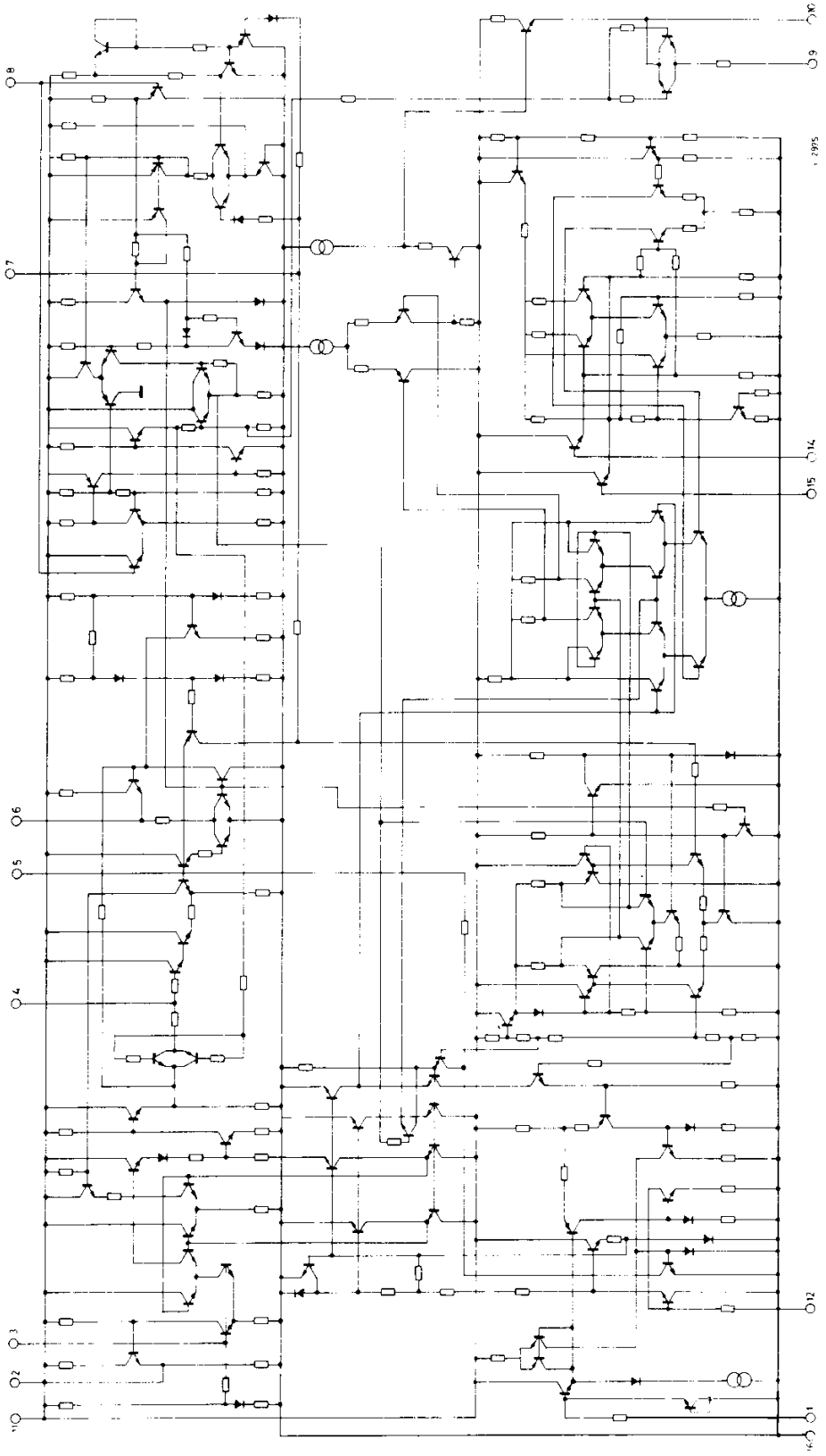
CONNECTION DIAGRAM
(top view)



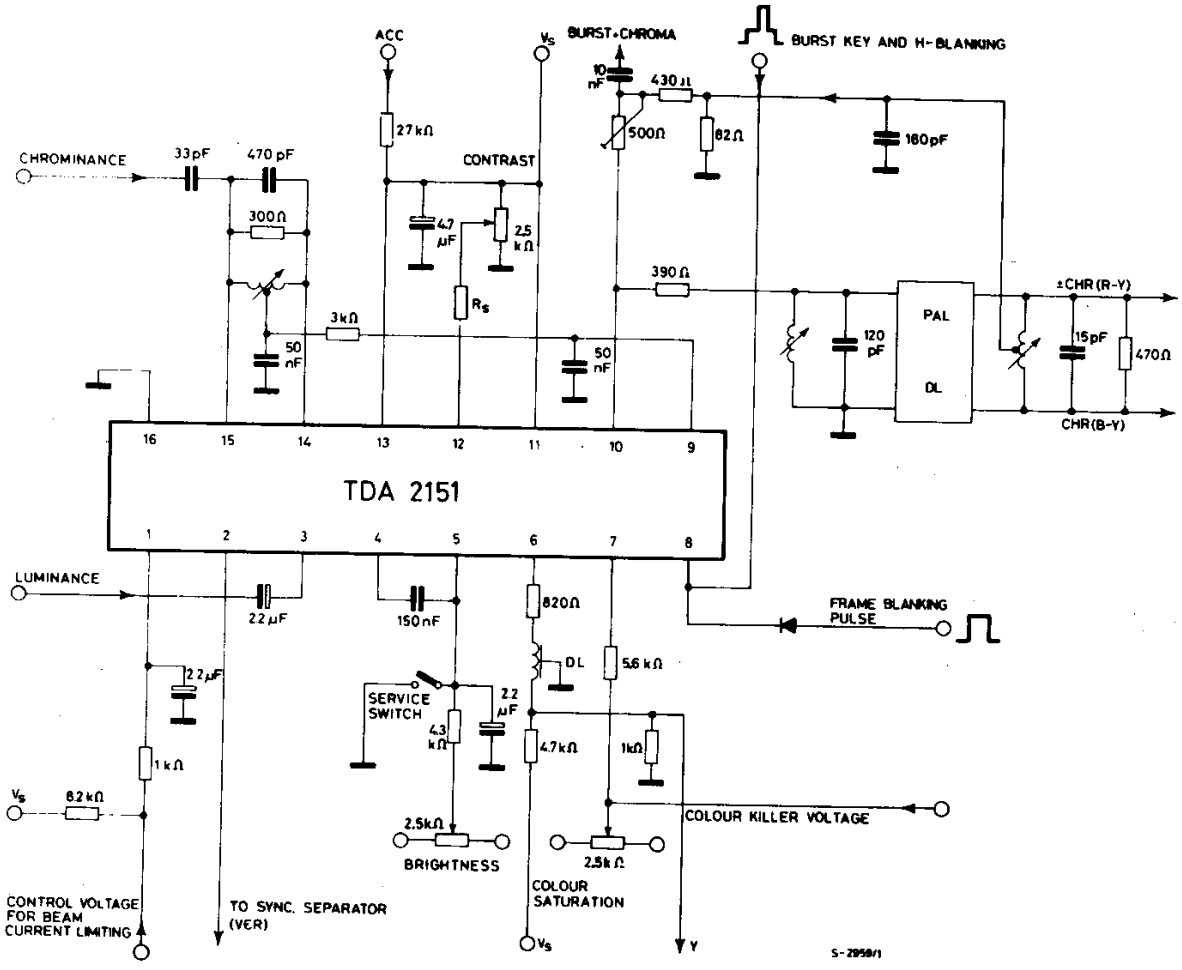
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, V_s = 12V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 11)		10.8		13.2	V
I_s	Supply current (pin 11)			45	56	mA
CHROMINANCE SECTION						
V_i	Peak to peak input signal (between pin 14 and pin 15)	f = 4.4 MHz			80	mV
V_o	Peak to peak chroma output signal (pin 10)	f = 4.4 MHz K ⩽ 5%		3		V
V_o	Max. peak to peak chroma output signal (pin 10)	f = 4.4 MHz		3.8		V
ΔG_{chr}	ACC range	$\Delta V_{10} \leqslant 1$ dB	26			dB
ΔG_{chr}	Saturation control range	V_{12} = 12V ΔV_7 = 2.1 to 6.5V		40		dB
$\frac{V_i}{V_o}$	Chroma signal attenuation during killer action	V_{12} = 12V	8			dB
$\frac{G_{chr}}{G_{burst}}$	Ratio of chroma voltage gain to burst voltage gain	V_{12} = 12V V_7 = 6.5V	0.94	1	1.06	–
		V_{12} = 12V V_7 = 4.3V	0.47	0.5	0.53	–
$\frac{\Delta G_y}{\Delta G_{chr}}$	Tracking ratio of luminance and chroma channels contrast control	ΔV_{12} = 0 to 12V		1	1.5	dB
LUMINANCE SECTION						
V_i	Peak to peak input signal (pin 3)	100% white bar		1		V
R_i	Input resistance (between pin 3 and pin 16)			12		kΩ
C_i	Input capacitance (between pin 3 and pin 16)				8	pF
V_2	Independent luminance output signal (peak to peak)	V_i = 1 Vpp		3.7		V
R_2	Independent luminance output resistance			100		Ω
V_5	Brightness DC control voltage			2 to 5.5		V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Luminance output signal at pin 6 (black to white)	V_{12} = 12V V_i = 1 Vpp	2	2,2	2.4	V
		V_{12} = 0V V_i = 1 Vpp	0.4		0.48	V
V_o	Black level of the luminance output signal (pin 6)	V_5 = 4.7V		3.6		V
V_o	Luminance service peak to peak output signal (pin 6)	V_5 = 0V		240		mV
V_8	Frame blanking pulse		1.4			V
I_7	Frame blanking pulse input current	Positive pulse	1			mA
		Negative pulse			-1	mA
$\frac{\Delta V_o}{\Delta V_5}$	Ratio of output blank level change to brightness control DC voltage change			0.5		–
ΔG_y	Contrast control range	V_{12} = 0 to 12V		13		dB

BEAM CURRENT LIMITER CHARACTERISTICS

Fig. 1 - Y output signal (black to white) and its reduction due to beam current limiter action vs. contrast control voltage

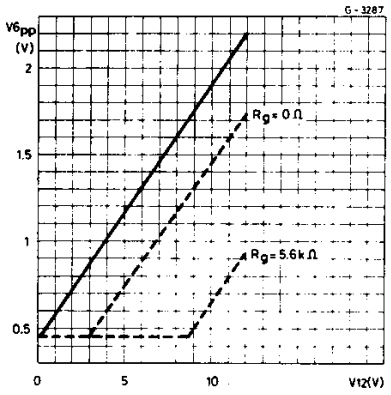


Fig. 2 - Normalized Y amplif. gain vs. b.c.l. control voltage

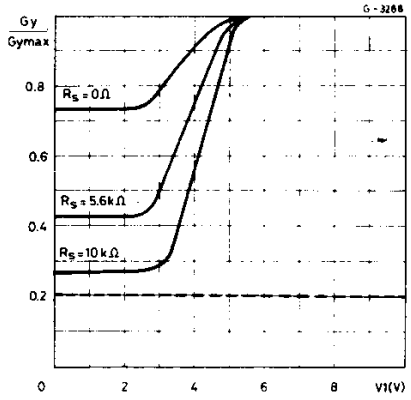
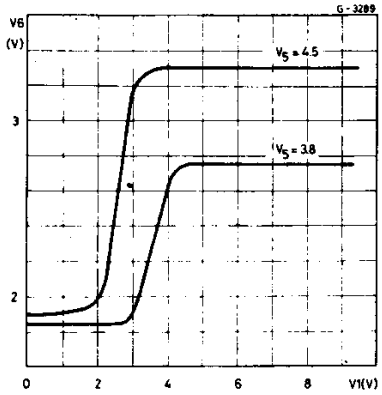
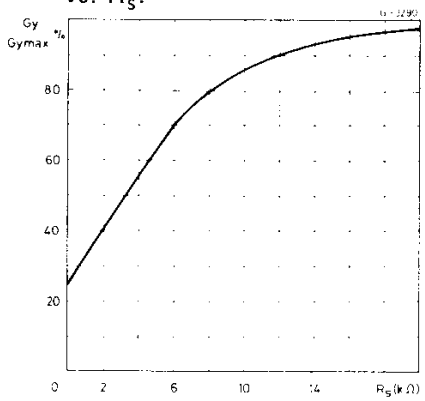


Fig. 3 - Y output black level vs. b.c.l. control voltage



APPLICATION INFORMATION

Fig. 4 - Reduction of the contrast due to b.c.l. action vs. R_S.



Pin 1 - Beam current limiter input

The beam current limiter is controlled through pin 1 by a DC voltage which is proportional to the average CRT beam current. When the beam current increases, the voltage applied at pin 1 decreases and causes first a reduction in contrast and then a reduction in brightness. The amount of the contrast reduction is programmable by means of the resistance R_S connected in series to pin 12. The characteristics of b.c.l. are shown in figures 1, 2, 3 and 4. By varying the values of the integrator circuit components on the EHT transformer, both the intervention point and the limitation slope can be adjusted to suit the various types of CRTs.

Pin 2 - VCR Output

The luminance signal, with typical amplitude of 3.5 Vpp, is available at pin 2 of the IC. This signal has positive sync.suitable for driving the sync.separator if external video sources such as VCRs or video disc players are to be used.

Pin 3 - Y input

The luminance signal, of amplitude 1 Vpp, is capacitively coupled to pin 3 of the IC which shows high input impedance. The luminance signal is separated from the chrominance signal by means of a 4.43 MHz trap. The design of this trap is very important. In fact the 4.43 MHz leakage at the decoder RGB outputs is largely due to the leakage which passes through the luminance channel.

Pins 4 and 5 - Black level clamp and brightness control

The clamp locking pulse is supplied by the pulse shaper circuit which receives the composite blanking and key pulse (sandcastle) from pin 8. The clamp circuit compares the brightness control setting. When pin 5 is connected to ground, a service signal suitable for alignment of CRT cutoffs is available at the luminance output.
The service signal on the voltage divider after the delay line is:

S - 2835

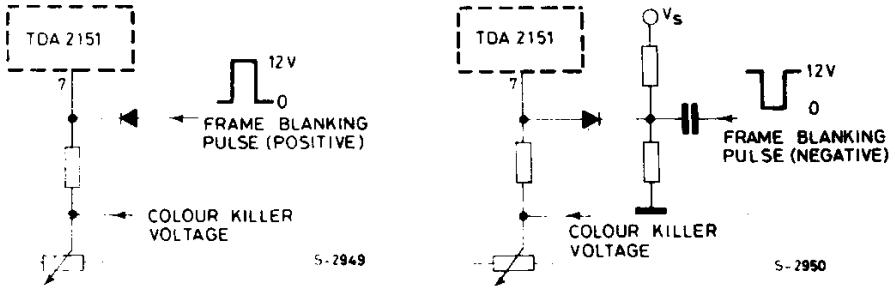
Pin 6 - Y output

With contrast control at maximum, a luminance signal, with typical amplitude from white to black of 2.2V, is present at pin 6. The black level of this signal is determined by the brightness control voltage. To allow the luminance delay line to be adapted easily, output Y of the TDA 2151 has low impedance. Before the output, the luminance signal is cutoff during line and frame flyback by the horizontal and vertical blanking pulses.

Pin 7 - Saturation control

The gain of the chroma amplifier is set by means of the colour saturation control connected to pin 7 of the IC. The control range is between 2.1V and 6.5V, causing a chrominance channel gain variation of 60 dB. The colour killer, which is activated in the TDA 2140, also acts on pin 7 and guarantees 8 dB as minimum attenuation of the chroma signal.
Pin 7 also receives frame blanking pulses. Using the application circuits shown on the next page, positive or negative blanking pulses can be applied to the IC.

APPLICATION INFORMATION (continued)



Pin 8 - H and V blanking and key pulses input
The H and V blanking and key pulses are separated by means of internally fixed thresholds whose levels are 1.2V, 1.4V and 4V respectively. A suitable composite blanking and key pulse is generated by the TDA 2140 but any other source can be used if correct amplitude and phase of blanking and key pulses are provided. The input impedance at pin 8 is 50 kΩ.

Pin 9 - (see pins 14 and 15)

Pin 10 - Chroma output
Pin 10 is the low impedance chrominance output. In order to prevent the colour burst signal from being influenced by contrast and saturation controls, the second and third stages of the amplification chain are at maximum gain during the burst period. It is important to note that the signal, to which the TDA 2140 refers for generating the ACC control voltage, is picked up after the PAL delay line so that the attenuation spread of the delay line is compensated. This in addition to the low gain spread in the chrominance amplification chain, eliminates presetting of the saturation control. With saturation and contrast controls at maximum, the relationship between chrominance and burst signals at pin 10 corresponds to that at the input; this relationship, referred to the brightness output signal, gives an oversaturation of 6 dB.

Pin 11 - Positive supply
The operating supply voltage of the device ranges from 10.8V to 13.2V.

Pin 12 - Contrast control
The contrast control is connected to pin 12. A special circuit gives a linear gain characteristic to the contrast control voltage; gain variation is 14 dB over the 0 to 12V DC control voltage range. The contrast control acts in the same way on the luminance channel and on the chrominance channel. Excellent tracking is thus obtained between luminance channel amplification and chrominance channel amplification throughout the range of contrast adjustment.

Pin 13 - ACC input
Pin 13 is the high impedance input for controlling the gain of the chroma amplifier. It has to be connected to pin 10 of the TDA 2140 through a low pass filter whose purpose is to reduce the ripple on the ACC control voltage.

Pins 14 and 15 - Chroma input
The chroma signal is carried symmetrically by pins 14 and 15 to the high impedance input of a 4 stage amplification chain. The gain of the first stage is regulated by the ACC voltage generated in the TDA 2140. The balanced chrominance signal which leaves the bandpass filter is applied between pins 14 and 15. The maximum signal handling capability of the input circuit is 80 mVpp. Due to the high gain of the chrominance amplifiers, attenuation of the Y signal must be good and both the group delay and the overall delay introduced by the filter must be minimal. DC feedback is used between the last stage (pin 9) and the input to stabilize DC operation of the amplification chain.

Pin 16 - Ground