



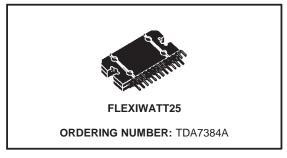
4 x 35W QUAD BRIDGE CAR RADIO AMPLIFIER

- HIGH OUTPUT POWER CAPABILITY:
 - 4 x 40W/4 Ω MAX.
 - $4 \times 35W/4\Omega$ EIAJ
 - $4 \times 25W/4\Omega$ @ 14.4V, 1KHz, 10%
 - $4 \times 22W/4\Omega$ @ 13.2V, 1KHz, 10%
- LOW DISTORTION
- LOW OUTPUT NOISE
- ST-BY FUNCTION
- MUTE FUNCTION
- AUTOMUTE AT MIN. SUPPLY VOLTAGE DE-TECTION
- LOW EXTERNAL COMPONENT COUNT:
 - INTERNALLY FIXED GAIN (26dB)
 - NO EXTERNAL COMPENSATION
 - NO BOOTSTRAP CAPACITORS

PROTECTIONS:

- OUTPUT SHORT CIRCUIT TO GND, TO Vs, ACROSS THE LOAD
- VERY INDUCTIVE LOADS
- OVERRATING CHIP TEMPERATURE WITH SOFT THERMAL LIMITER
- LOAD DUMP VOLTAGE

BLOCK AND APPLICATION DIAGRAM

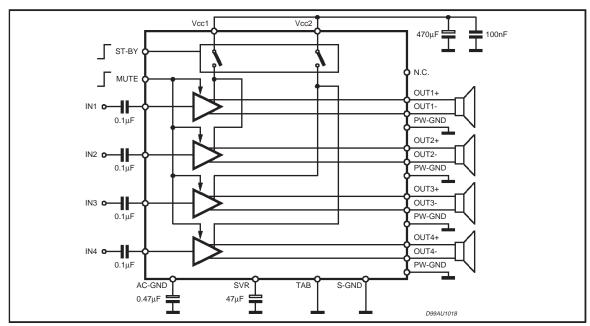


- FORTUITOUS OPEN GND
- REVERSED BATTERY
- ESD

DESCRIPTION

The TDA7384A is a new technology class AB Audio Power Amplifier in Flexiwatt 25 package designed for high end car radio applications.

Thanks to the fully complementary PNP/NPN output configuration the TDA7384A allows a rail to rail output voltage swing with no need of bootstrap capacitors. The extremely reduced components count allows very compact sets.

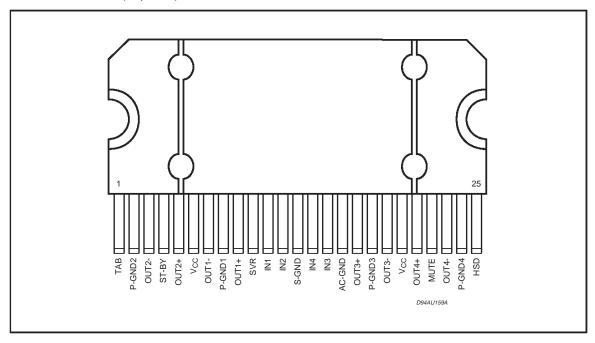


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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Operating Supply Voltage	18	V
V _{CC (DC)}	DC Supply Voltage	28	V
V _{CC (pk)}	Peak Supply Voltage (t = 50ms)	50	V
lo	Output Peak Current: Repetitive (Duty Cycle 10% at f = 10Hz) Non Repetitive (t = 100µs)	4.5 5.5	A A
P _{tot}	Power dissipation, (T _{case} = 70°C)	80	W
Tj	Junction Temperature	150	°C
T _{stg}	Storage Temperature	- 55 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

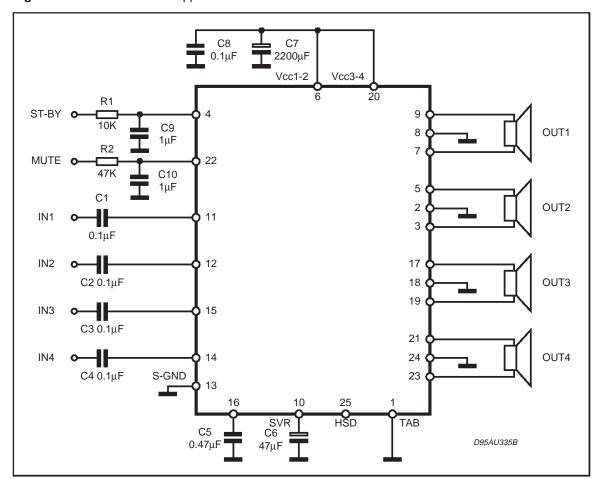
Symbol	Parameter	Value	Unit
R _{th j-case}	Thermal Resistance Junction to Case Max.	1	°C/W

ELECTRICAL CHARACTERISTICS (Vs = 14.4V; f = 1KHz; $R_g = 600\Omega$; $R_L = 4\Omega$; $T_{amb} = 25^{\circ}C$; Refer to the test and application diagram, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
I _{q1}	Quiescent Current	R _L = ∞	120	190	350	mA
Vos	Output Offset Voltage	Play Mode			±80	mV
dV _{OS}	During mute ON/OFF output offset voltage				±80	mV
G∨	Voltage Gain		25	26	27	dB
dG_{v}	Channel Gain Unbalance				±1	dB
P _o	Output Power	V _S = 13.2V; THD = 10% V _S = 13.2V; THD = 0.8% V _S = 14,4V; THD = 10%	20 15 24	22 17 26		W W W
Po EIAJ	EIAJ Output Power (*)	VS = 13.7V	32	35		W
P _{o max.}	Output Power (*)	V _S = 14.4V	38	40		W
THD	Distortion	$P_0 = 4W$		0.04	0.15	%
e _{No}	Output Noise	"A Weighted" Bw = 20Hz to 20KHz		50 70	70 100	μV μV
SVR	Supply Voltage Rejection	$f = 100Hz; V_r = 1Vrms$	50	65		dB
f _{ch}	High Cut-Off Frequency	$P_0 = 0.5W$	100	200		KHz
R _i	Input Impedance		70	100		ΚΩ
C _T	Cross Talk	$f = 1KHz$ $P_O = 4W$ $f = 10KHz$ $P_O = 4W$	60 50	70 60	_ _	dB dB
I _{SB}	St-By Current Consumption	$V_{St-By} = 1.5V$			100	μΑ
I _{pin4}	St-by pin Current	VSt-By = 1.5V to 3.5V			±10	μΑ
$V_{SB out}$	St-By Out Threshold Voltage	(Amp: ON)	3.5			V
$V_{SB\ in}$	St-By in Threshold Voltage	(Amp: OFF)			1.5	V
A_M	Mute Attenuation	P _{Oref} = 4W	80	90		dB
V _M out	Mute Out Threshold Voltage	(Amp: Play)	3.5			V
$V_{M\ in}$	Mute In Threshold Voltage	(Amp: Mute)			1.5	V
V _{AM} in	V _S Automute Threshold	(Amp: Mute) Att \geq 80dB; P _{Oref} = 4W (Amp: Play) Att $<$ 0.1dB; P _O = 0.5W		7.6	6.5 8.5	V
I _{pin22}	Muting Pin Current			11	20	μΑ

^(*) Saturated square wave output.

Figure 1: Standard Test and Application Circuit



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COMPONENTS & TOP COPPER LAYER TDA7384A IC 1 C11 弘 **с**ил ++ 1162-5473 랢 C2 C1 co C# IN S IN S IN S IN S 2 DNO 1 DNO 3 DNO 4 DNO **BOTTOM COPPER LAYER** 113

Figure 2: P.C.B. and component layout of the figure 1 (1:1 scale)

471

Figure 3: Quiescent Current vs. Supply Voltage

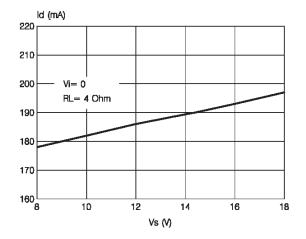


Figure 4: Quiescent Output Voltage vs. Supply Voltage

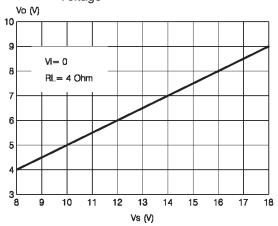


Figure 5: Output Power vs. Supply Voltage

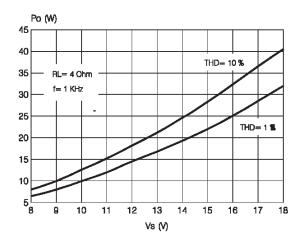


Figure 6: Distortion vs. Output Power

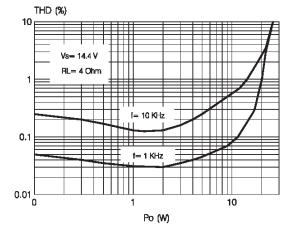


Figure 7: Distortion vs. Frequency

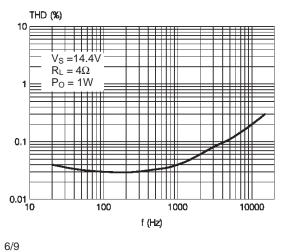
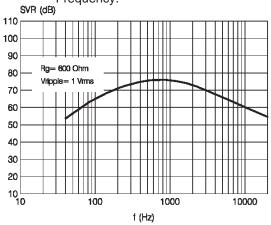


Figure 8: Supply Voltage Rejection vs. Frequency.



n (%)

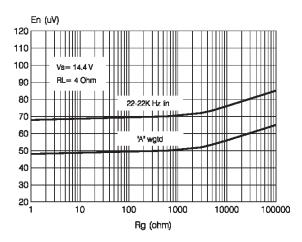
n

80

70

__0 22

Figure 9: Output Noise vs. Source Resistance



60 RL= 4 x 4 0hm 60 50 40 Pdiss 40 30 20 10 10

Figure 10: Power Dissipation & Efficiency vs. Output Power

Pdiss (W)

2 4 6 8 10 12 14 16 18 20

80

70

APPLICATION HINTS (ref. to the circuit of fig. 1) SVR

Besides its contribution to the ripple rejection, the SVR capacitor governs the turn ON/OFF time sequence and, consequently, plays an essential role in the pop optimization during ON/OFF transients. To conveniently serve both needs, ITS MINIMUM RECOMMENDED VALUE IS $10\mu F$.

INPUT STAGE

The TDA7384A'S inputs are ground-compatible and can stand very high input signals (± 8Vpk) without any performances degradation.

If the standard value for the input capacitors $(0.1\mu F)$ is adopted, the low frequency cut-off will amount to 16 Hz.

STAND-BY AND MUTING

STAND-BY and MUTING facilities are both

CMOS-COMPATIBLE. If unused, a straight connection to Vs of their respective pins would be admissible. Conventional/low-power transistors can be employed to drive muting and stand-by pins in absence of true CMOS ports or microprocessors.

Po (W)

R-C cells have always to be used in order to smooth down the transitions for preventing any audible transient noises.

Since a DC current of about 10 uA normally flows out of pin 22, the maximum allowable muting-series resistance (R₂) is $70 \mathrm{K}\Omega$, which is sufficiently high to permit a muting capacitor reasonably small (about 1 μ F).

If R_2 is higher than recommended, the involved risk will be that the voltage at pin 22 may rise to above the 1.5 V threshold voltage and the device will consequently fail to turn OFF when the mute line is brought down.

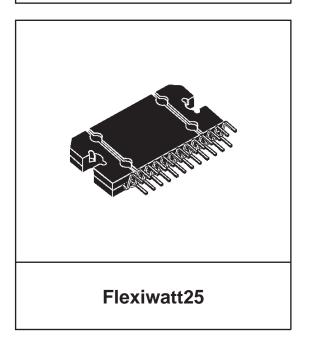
About the stand-by, the time constant to be assigned in order to obtain a virtually pop-free transition has to be slower than 2.5V/ms.



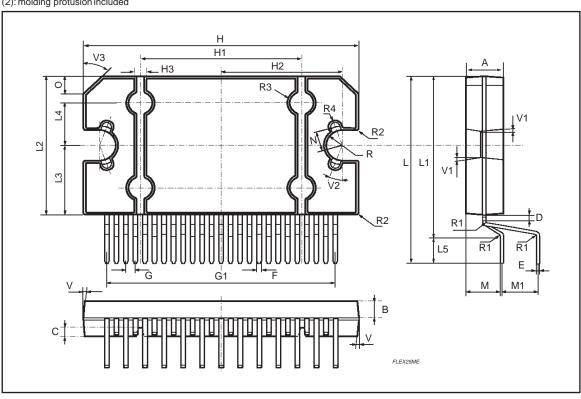
TDA7384A

DIM.	mm			inch			
DIIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Α	4.45	4.50	4.65	0.175	0.177	0.183	
В	1.80	1.90	2.00	0.070	0.074	0.079	
С		1.40			0.055		
D	0.75	0.90	1.05	0.029	0.035	0.041	
Е	0.37	0.39	0.42	0.014	0.015	0.016	
F (1)			0.57			0.022	
G	0.80	1.00	1.20	0.031	0.040	0.047	
G1	23.75	24.00	24.25	0.935	0.945	0.955	
H (2)	28.90	29.23	29.30	1.138	1.150	1.153	
H1		17.00			0.669		
H2		12.80			0.503		
H3		0.80			0.031		
L (2)	22.07	22.47	22.87	0.869	0.884	0.904	
L1	18.57	18.97	19.37	0.731	0.747	0.762	
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626	
L3	7.70	7.85	7.95	0.303	0.309	0.313	
L4		5			0.197		
L5		3.5			0.138		
М	3.70	4.00	4.30	0.145	0.157	0.169	
M1	3.60	4.00	4.40	0.142	0.157	0.173	
N		2.20			0.086		
0		2			0.079		
R		1.70			0.067		
R1		0.5			0.02		
R2		0.3			0.12		
R3		1.25			0.049		
R4	0.50 0.019						
V	5° (Typ.)						
V1	3° (Typ.)						
V2	20° (Typ.)						
V3	45° (Typ.)						

OUTLINE AND MECHANICAL DATA



(1): dam-bar protusion not included (2): molding protusion included



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