Half-Bridge N-Channel MOSFET Driver for DC/DC Conversion

FEATURES

- 5-V Gate Drive
- Undervoltage Lockout
- Internal Bootstrap Diode
- Adaptive Shoot-Through Protection
- Syncronous MOSFET Enable
- Shutdown Control
- Adjustable HighsidePropagation Delay
- Switching Frequency Up to 1 MHz
- Drive MOSFETs In 4.5- to 50-V Systems

APPLICATIONS

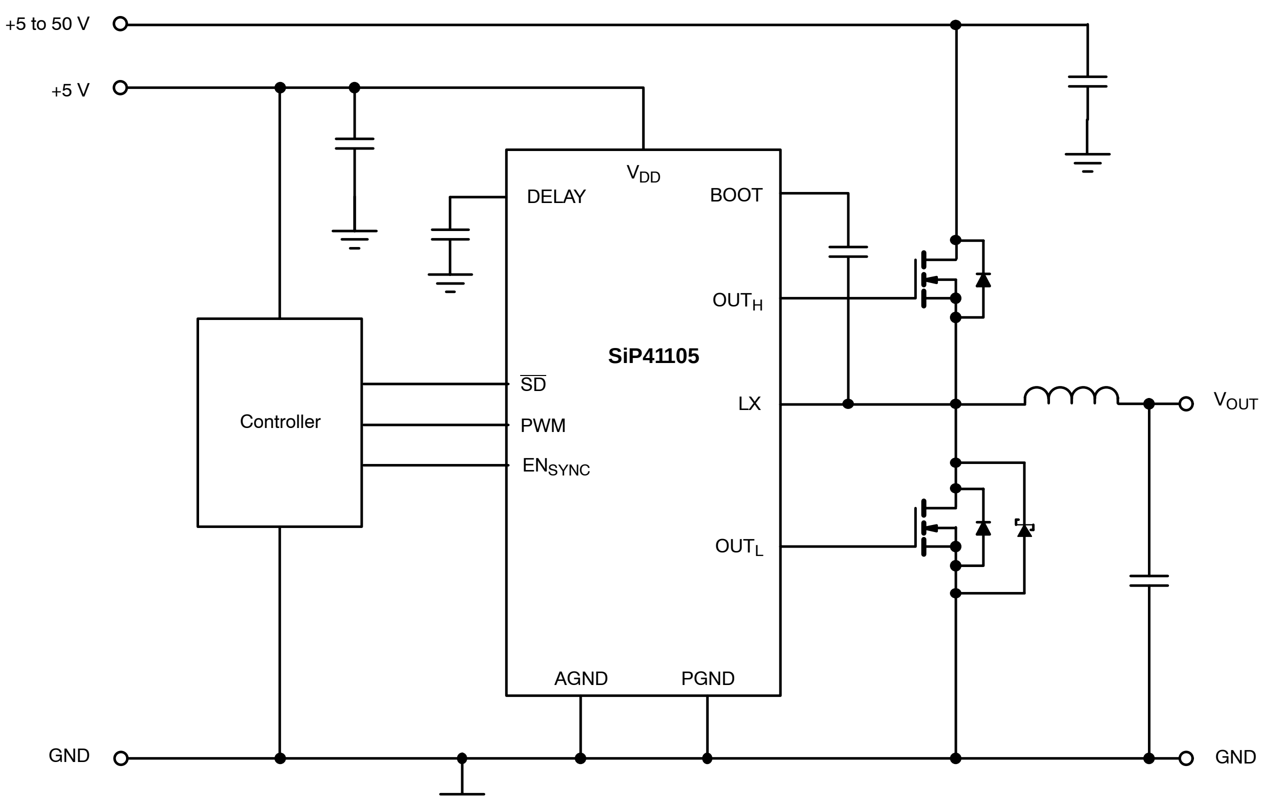
- Multi-Phase DC/DC Conversion
- High Current Synchronous Buck Converters
- High Frequency Synchronous Buck Converters
- Asynchronous-to-Synchronous Adaptations
- Mobile Computer DC/DC Converters
- Desktop Computer DC/DC Converters

DESCRIPTION

SiP41105 is a high-speed half-bridge MOSFET driver with adaptive shoot-through protection for use in high frequency, high current, multiphase dc-dc synchronous rectifier buck power supplies. It is designed to operate at switching frequencies up to 1 MHz. The high-side driver is bootstrapped to allow driving n-channel MOSFETs. SiP41105 comes with adaptive shoot-through protection to prevent simultaneous conduction of the external MOSFETs.

The SiP41105 is available in a 16-Pin TSSOP PowerPAK® package and is specified to operate over the industrial temperature range of −40 °C to 85 °C.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{DD}, PWM, $\overline{SD}$, EN_{SYNC}, DELAY . . . . . 7 V
LX, BOOT . . . . . 55 V
BOOT to LX . . . . . 7 V
Storage Temperature . . . . . −40 to 150°C
Operating Junction Temperature . . . . . 125°C

Power Dissipation[a]
TSSOP-16 PowerPAK . . . . . 2.6 W
Thermal Impedance (Θ_{JA})[a]
TSSOP-16 PowerPAK . . . . . 38°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
a. Derate 26.3 mW/°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{DD} . . . . . 4.5 V to 5.5 V
V_{BOOT} . . . . . 4.5 V to 50 V
C_{BOOT} . . . . . 100 nF to 1 μF
Operating Temperature Range . . . . . −40 to 85°C

SPECIFICATIONS[a]

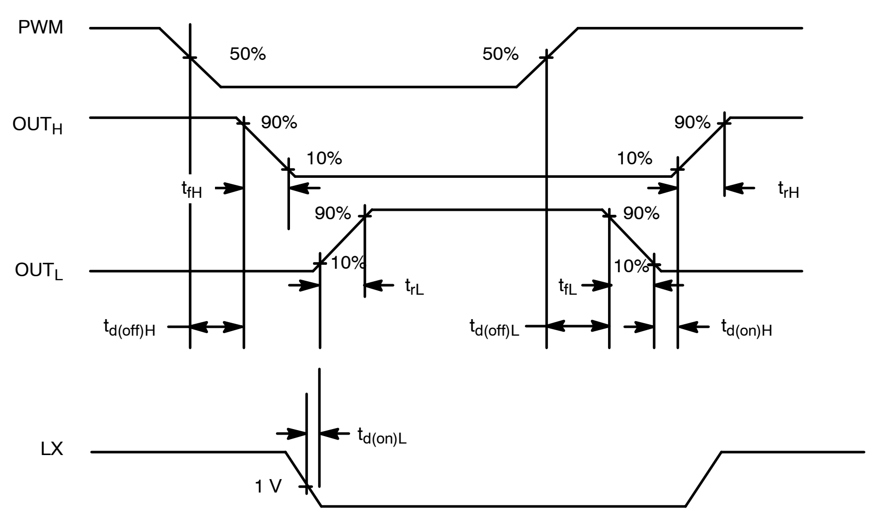
Parameter		Symbol	Test Conditions Unless Specified V_{DD} = 5 V, $V_{BOOT} - V_{LX}$ = 5 V, C_{LOAD} = 3 nF T_A = −40 to 85°C	Limits Min[a]	Typ[b]	Max[a]	Unit
Power Supplies							
Supply Voltage		V_{DD}		4.5		5.5	V
Quiescent Current		I_{DDQ}	f_{PWM} = 1 MHz, C_{LOAD} = 0		2.4	3.0	mA
Shutdown Current		I_{SD}	$\overline{SD}$ = Low			1	μA
Reference Voltage							
Break-Before-Make[c]		V_{BBM}			1		V
PWM Input							
Input High		V_{IH}		4.0		V_{DD}	V
Input Low		V_{IL}				0.5	
Bias Current		I_B			±0.3	±1	μA
$\overline{SD}$, EN_{SYNC} Inputs							
Input High		V_{IH}		2.0		V_{DD}	V
Input Low		V_{IL}				1.0	
Bias Current	EN_{SYNC}	I_B				±1	μA
	$\overline{SD}$		$\overline{SD}$ = 5 V		3.5	7	
High-Side Undervoltage Lockout							
Threshold		V_{UVHS}	Rising or Falling	2.5	3.35	3.75	V
Bootstrap Diode							
Forward Voltage		V_F	I_F = 10 mA, T_A = 25°C	0.70	0.76	0.82	V
MOSFET Drivers							
High-Side Drive Current[c]		$I_{PKH(source)}$			0.9		A
		$I_{PKH(sink)}$			1.1		
Low-Side Drive Current[c]		$I_{PKL(source)}$			0.8		
		$I_{PKL(sink)}$			1.5		
High-Side Driver Impedance		$R_{DH(source)}$			2.5	3.8	Ω
		$R_{DH(sink)}$			2.2	3.3	
Low-Side Driver Impedance		$R_{DL(source)}$			3.4	5.1	
		$R_{DL(sink)}$			1.4	2.1	

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V_{DD} = 5 V, $V_{BOOT} - V_{LX}$ = 5 V, C_{LOAD} = 3 nF T_A = −40 to 85°C	Limits Min[a]	Typ[b]	Max[a]	Unit
MOSFET Drivers						
High-Side Rise Time	t_{rH}	10% – 90%		32	40	ns
High-Side Fall Time	t_{fH}	90% – 10%		36	45	
High-Side Propagation Delay[c]	$t_{d(off)H}$	See Timing Waveforms		20		
	$t_{d(on)H}$	See Timing Waveforms		30		
Low-Side Rise Time	t_{rL}	10% – 90%		45	55	
Low-Side Fall Time	t_{fL}	90% – 10%		20	30	
Low-Side Propagation Delay[c]	$t_{d(off)L}$	See Timing Waveforms		30		
	$t_{d(on)L}$	See Timing Waveforms		30		
LX Timer						
LX Falling Timeout[c]	t_{LX}			420		ns
V_{DD} Undervoltage Lockout						
Threshold Rising	V_{UVLOR}			4.3	4.5	V
Threshold Falling	V_{UVLOF}		3.7	4.1		
Hysteresis				0.4		
Power on Reset Time[c]				2.5		ms
Thermal Shutdown						
Temperature	T_{SD}	Temperature Rising		165		°C
Hysteresis	T_H	Temperature Falling		25		

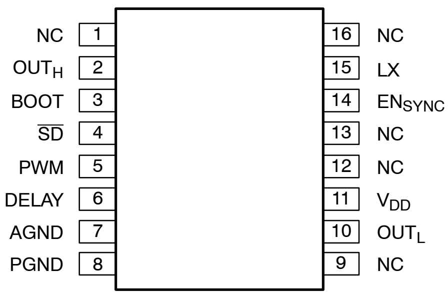
Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (−40° to 85°C).
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at V_{CC} = 5V unless otherwise noted.
c. Guaranteed by design. Add 1.2 ns/pF to $t_{d(on)H}$ with external capacitor.

TIMING WAVEFORMS



PIN CONFIGURATION AND TRUTH TABLE

TSSOP-16 PowerPAK



TRUTH TABLE

PWM	SD	EN_{SYNC}	OUT_H	OUT_L
L	H	L	L	L
H	H	L	H	L
L	H	H	L	H
H	H	H	H	L
X	L	X	L	L

ORDERING INFORMATION

Part Number	Temperature Range	Marking
SiP41105DQP-T1	−40 to 85°C	41105

Eval Kit	Temperature Range
SiP41105DB	−40 to 85°C

PIN DESCRIPTION

Pin Number	Name	Function
1	NC	No Connection
2	OUT_H	High-side MOSFET gate drive
3	BOOT	Bootstrap supply for high-side driver. A capacitor connects between BOOT and LX.
4	$\overline{SD}$	Shuts down the driver IC
5	PWM	Input signal for the MOSFET drivers
6	DELAY	Connection for the highside delay adjustment capacitor.
7	AGND	Analog Ground
8	PGND	Power Ground
9	NC	No Connection
10	OUT_L	Synchronous or low-side MOSFET gate drive
11	V_{DD}	+5-V supply
12	NC	No Connection
13	NC	No Connection
14	EN_{SYNC}	Enables OUT_L, the driver for the synchronus MOSFET
15	LX	Connection to source of high-side MOSFET, drain of the low-side MOSFET, and the inductor
16	NC	No Connection

FUNCTIONAL BLOCK DIAGRAM

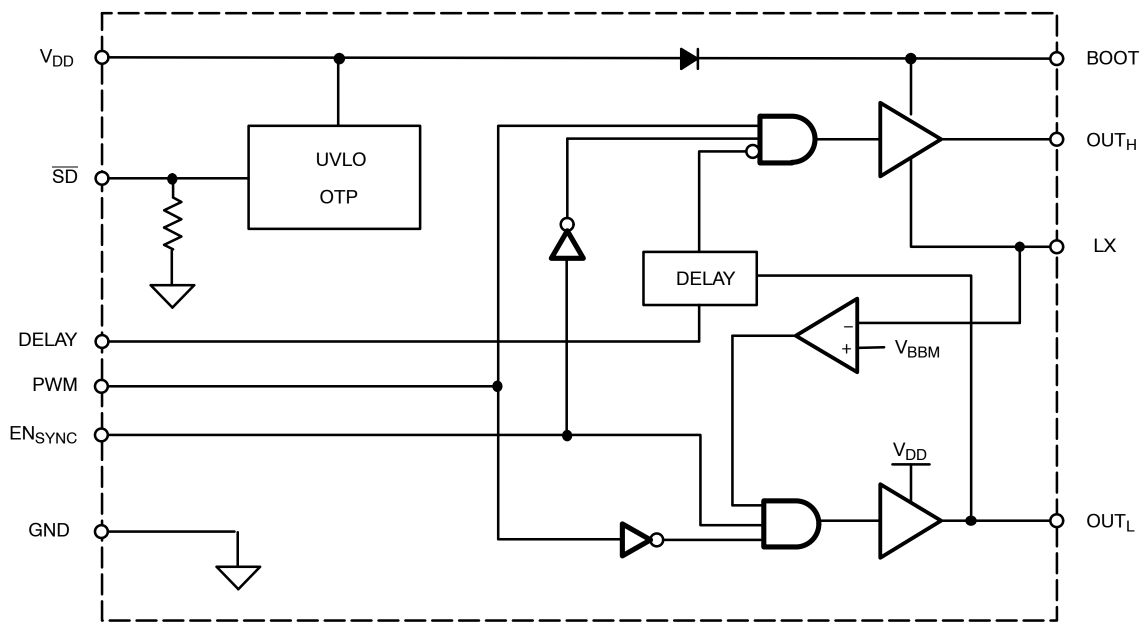


Figure 1.

DETAILED OPERATION

PWM

The PWM pin controls the switching of the external MOSFETs. The driver logic operates in a noninverting configuration. The PWM input stage should be driven by a signal with fast transition times, like those provided by a PWM controller or logic gate, (<200 ns). The PWM input functions as a logic input and is not intended for applications where a slow changing input voltage is used to generate a switching output when the input switching threshold voltage is reached.

Low-Side Driver

The supplies for the low-side driver are V_{DD} and GND. During shutdown, OUT_L is held low.

High-Side Driver

The high-side driver is isolated from the substrate to create a floating high-side driver so that an n-channel MOSFET can be used for the high-side switch. The supplies for the high-side driver are BOOT and LX. The voltage is supplied by a floating bootstrap capacitor, which is continually recharged by the switching action of the output. During shutdown OUT_H is held low.

Bootstrap Circuit

The internal bootstrap diode and a bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode replaces the external Schottky diode needed for the bootstrap circuit; only a capacitor is necessary to complete the bootstrap circuit. The bootstrap capacitor is sized according to,

$$C_{BOOT} = (Q_{GATE}/\Delta V_{BOOT-LX}) \times 10$$

where Q_{GATE} is the gate charge needed to turn on the high-side MOSFET and $\Delta V_{BOOT-LX}$ is the amount of droop allowed in the bootstrapped supply voltage when the high-side MOSFET is driven high. The bootstrap capacitor value is typically 0.1 μF to 1 μF. The bootstrap capacitor voltage rating must be greater than V_{DD} + 5 V to withstand transient spikes and ringing.

Shoot-Through Protection

The external MOSFETs are prevented from conducting at the same time during transitions. Break-before-make circuits monitor the voltages on the LX pin and the OUT_L pin and control the switching as follows: When the signal on PWM goes low, OUT_H will go low after an internal propagation delay. After the voltage on LX falls below 1 V by the inductor action, the low-side driver is enabled and OUT_L goes high after some delay. When the signal on PWM goes high, OUT_L will go low after an internal propagation delay. After the voltage on OUT_L drops below 1 V the high-side driver is enabled and OUT_H will go high after an internal propagation delay. If LX does not drop below 1 V within 400 ns after OUT_H goes low, OUT_L is forced high until the next PWM transition.

Delay

The addition of a capacitor between DELAY and GND will increase the propagation delay time for OUT_H going high. Delay capacitance may be added to prevent shoot through current in the low-side MOSFET due to the finite time between OUT_L going low and the continuing conduction of the low-side MOSFET. Choose a MOSFET with lower gate resistance to reduce this effect. If necessary, choose a capacitor value that prevents MOSFET conduction under worst-case temperature and manufacturing conditions. Propagation delay is increased according to the ratio of 1.2 ns/pF.

Synchronous MOSFET Enable

Under light load conditions, efficiency can be increased by disabling the synchronous MOSFET, thus avoiding the gate charge losses of the synchronous MOSFET. When EN_{SYNC} is low, OUT_L is forced low. When high, the low-side driver operates normally. EN_{SYNC} should be driven by a 5-V signal.

Shutdown

The driver enters shutdown mode when $\overline{SD}$ is low. Shutdown current is less than 1 μA.

V_{DD} Bypass Capacitor

MOSFET drivers draw large peak currents from the supplies when they switch. A local bypass capacitor is required to supply this current and reduce power supply noise. Connect a 1-μF ceramic capacitor as close as practical between the V_{DD} and GND pins.

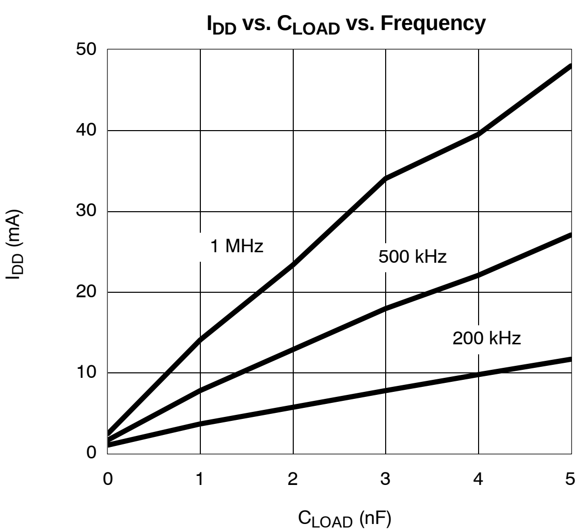
Undervoltage Lockout

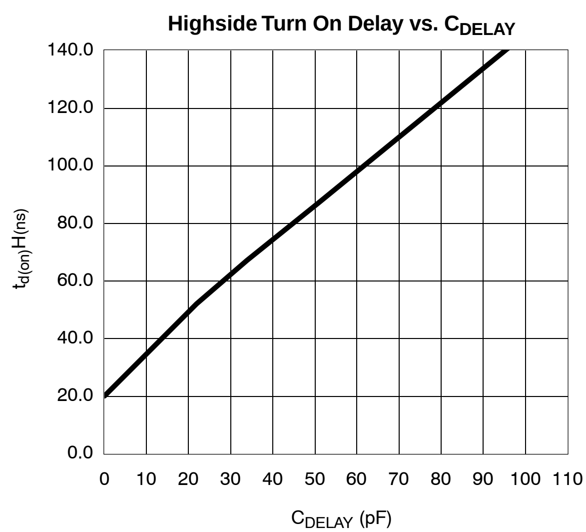
Undervoltage lockout prevents control of the circuit until the supply voltages reach valid operating levels. The UVLO circuit forces OUT_L and OUT_H to low when V_{DD} is below its specified voltage. A separate UVLO forces OUT_H low when the voltage between BOOT and LX is below the specified voltage.

Thermal Protection

If the die temperature rises above 165°C, the thermal protection disables the drivers. The drivers are re-enabled after the die temperature has decreased below 140°C.

TYPICAL CHARACTERISTICS





TYPICAL WAVEFORMS

Figure 2. PWM Signal vs. LX (Rising)

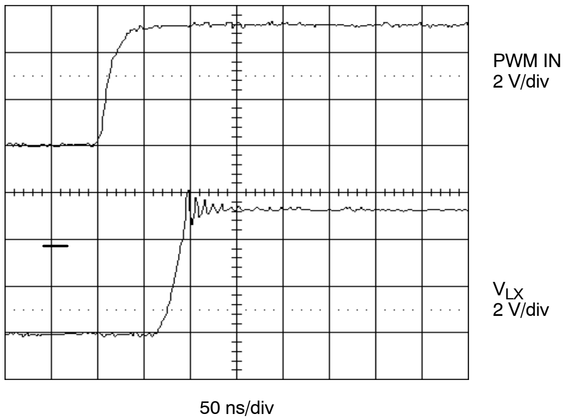


Figure 3. PWM Signal vs. LX (Falling)

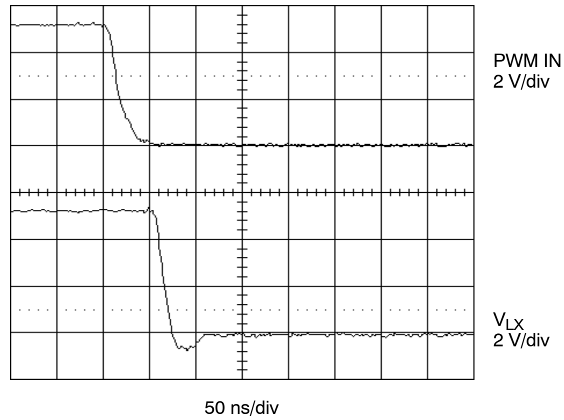


Figure 4. PWM Signal vs. HS Gate and LS Gate (Rising)

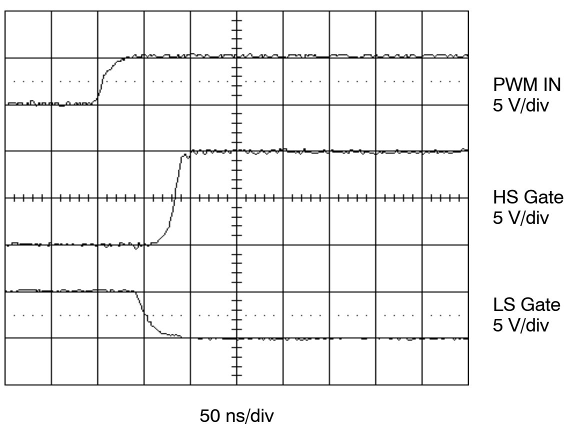


Figure 5. PWM Signal vs. HS Gate and LS Gate (Falling)

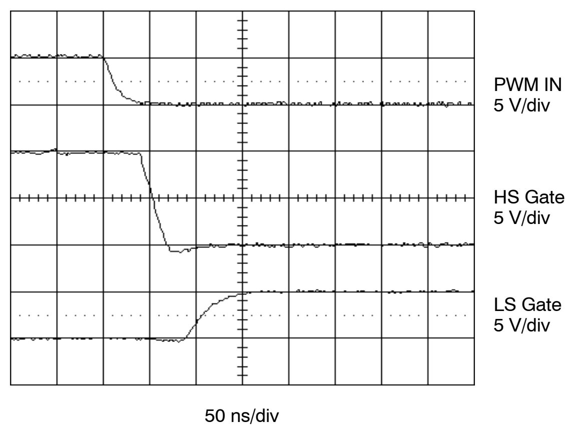
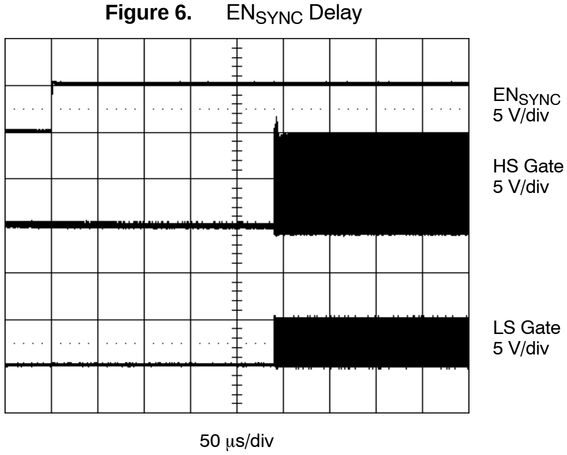


Figure 6. EN_{SYNC} Delay



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