Initial Release

Demo Board Available!

Sequencing Hotswap Controllers
(Negative Supply Rail)

Features

- -10V to 90V or +10V to +90V Operation
- Four PWRGD Flags with Programmable Delays
- Integrated “normally-on” Gate Clamp eliminates components
- UV/OV Lock Out & Power-On-Reset (POR) for Debouncing
- Sense resistor programmed Circuit Breaker & Servo Limit
- Programmable Circuit Breaker Delay
- Inrush control using either: Servo or Feedback Capacitor
- Feedback to RAMP pin saves gate protection components
- 100ms Start Up Timeout Protection for Output Overload
- Programmable Inrush Current di/dt Control
- Programmable Auto-Retry (tens of seconds if desired)
- Auto-Retry or Latched Operation
- Application solution for input voltage step (diode “ORing”)
- Enable through Open Drain interface to UV or OV
- Low Power, 0.6mA Active Mode, 0.4mA Sleep Mode
- Small SOIC-14 Package

Applications

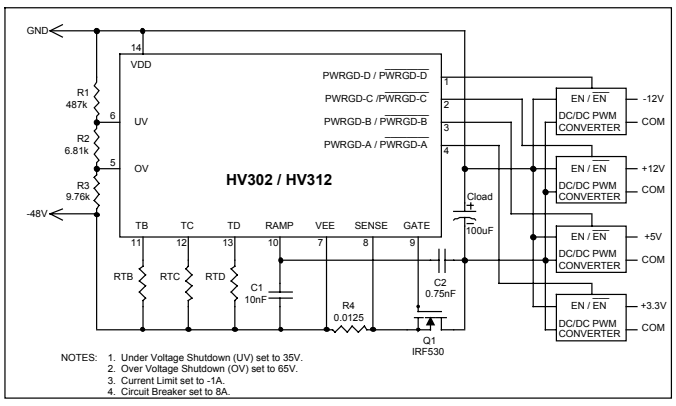
- -48V Telecom and Networking
- -24V Cellular and Fixed Wireless Systems
- -24V PBX Systems
- Power Over LAN (IEEE802.3)
- Distributed Power Systems
- Power Supply Control
- +48V Servers and SANs
- Hotswap Control of Diode ORed Multiple Power Sources
- Cooling Fan Systems

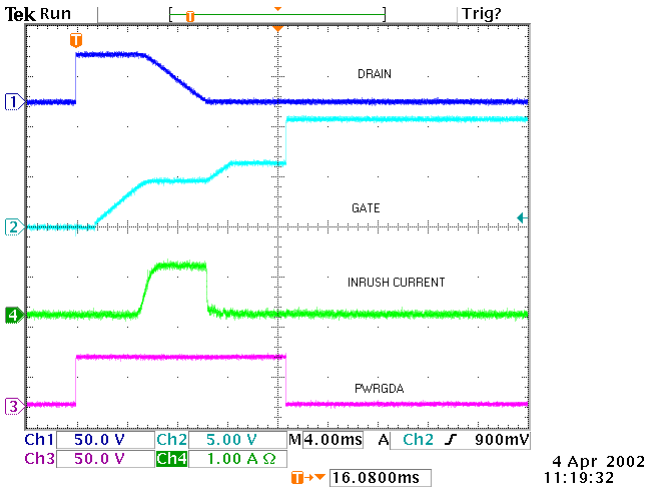
General Description

The HV302 and HV312 Hotswap Controllers perform current limiting, circuit breaker protection, over and under voltage detection power management functions during insertion of cards or modules into live backplanes and connectors. They may be used in systems where active control is implemented in the negative lead of supplies ranging from -10V to -90V or +10V to +90V.

During initial power application the external pass device is held off by a “normally-on” circuit that clamps its gate low. Thereafter UV/OV and power-on-reset work together to suppress gate turn on due to contact bounce. When stable connection has been established for the duration of a programmed time delay, the inrush current is controlled and limited to a programmed level using one of two possible methods; **servo mode** or drain to ramp **feedback capacitor mode**. When charging of the load capacitor is completed, the open drain PWRGD-A flag is asserted. Open drain PWRGD-B, PWRGD-C and PWRGD-D flags are asserted sequentially after the expiration of their respective programmed time delays. Thereafter it transitions to a low power sleep mode and continues to monitor current and input voltage. If full charging of the load capacitor is not achieved within 100ms or the circuit breaker is tripped at any time, the external pass device is turned off and all four PWRGD flags are reset to the inactive state. Thereafter a programmable auto-retry timer will hold the pass device off to allow it to cool before resetting and initiating auto-retry. The auto-retry can be disabled using a single resistor if desired.

Typical Application Circuit and Waveforms





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Absolute Maximum Ratings

V_{EE} reference to V_{DD} pin	+0.3V to -100V
V_{PWRGD} referenced to V_{EE} Voltage	-0.3V to +100V
V_{UV} and V_{OV} referenced to V_{EE} Voltage	-0.3V to +12V
Operating Ambient Temperature	-40°C to +85°C
Operating Junction Temperature	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C

Ordering Information

Active State of Power Good Flags	Package Options
	14 Pin SOIC
HIGH	HV302NG
LOW	HV312NG

Electrical Characteristics (-10V VIN -90V, -40°C T_A +85°C unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Supply (Referenced to V_{DD} pin)						
V_{EE}	Supply Voltage	-90		-10	V	
I_{EE}	Supply Current		600	700	µA	V_{EE} = -48V, Mode = Limiting
I_{EE}	Sleep Mode Supply Current		400	450	µA	V_{EE} = -48V, Mode = Sleep
OV and UV Control (Referenced to V_{EE} pin)						
V_{UVH}	UV High Threshold		1.26		V	Low to High Transition
V_{UVL}	UV Low Threshold		1.16		V	High to Low Transition
V_{UVHY}	UV Hysteresis		100		mV	
I_{UV}	UV Input Current			1.0	nA	$V_{UV} = V_{EE} + 1.9V$
V_{OVH}	OV High Threshold		1.26		V	Low to High Transition
V_{OVL}	OV Low Threshold		1.16		V	High to Low Transition
V_{OVHY}	OV Hysteresis		100		mV	
I_{OV}	OV Input Current			1.0	nA	$V_{OV} = V_{EE} + 0.5V$
Current Limit (Referenced to V_{EE} pin)						
$V_{SENSE-CL}$	Current Limit Threshold Voltage	40	50	60	mV	$V_{UV} = V_{EE} + 1.9V$, $V_{OV} = V_{EE} + 0.5V$
$V_{SENSE-CB}$	Circuit Breaker Current Limit Threshold Voltage	80	100	120	mV	$V_{UV} = V_{EE} + 1.9V$, $V_{OV} = V_{EE} + 0.5V$
Gate Drive Output (Referenced to V_{EE} pin)						
V_{GATE}	Maximum Gate Drive Voltage	8.5	10	12	V	$V_{UV} = V_{EE} + 1.9V$, $V_{OV} = V_{EE} + 0.5V$
I_{GATEUP}	Gate Drive Pull-Up Current	500			µA	$V_{UV} = V_{EE} + 1.9V$, $V_{OV} = V_{EE} + 0.5V$
$I_{GATEDOWN}$	Gate Drive Pull-Down Current	40			mA	$V_{UV} = V_{EE}$, $V_{OV} = V_{EE} + 0.5V$
Ramp Timing Control - Test Conditions: C_{LOAD}=100µF, C_{RAMP}=10nF, $V_{UV} = V_{EE} + 1.9V$, $V_{OV} = V_{EE} + 0.5V$, External MOSFET is IRF530*						
I_{RAMP}	Ramp Pin Output Current		10		µA	V_{SENSE} = 0V
t_{POR}	Time from UV to Gate Turn On	2.0			ms	(See Note 1)
t_{RISE}	Time from Gate Turn On to V_{SENSE} Limit	400			µs	
t_{LIMIT}	Duration of Current Limit Mode		5.0		ms	
$t_{PWRGD-A}$	Time from Current Limit to PWRGD-A		5.0		ms	
$t_{PWRGD-B}$	Maximum Time from PWRGD-A to PWRGD-B	150	200	250	ms	R_{TB} = 120kΩ
$t_{PWRGD-B}$	Minimum Time from PWRGD-A to PWRGD-B	3.0	5.0	8.0	ms	R_{TB} = 3kΩ
$t_{PWRGD-C}$	Maximum Time from PWRGD-B to PWRGD-C	150	200	250	ms	R_{TC} = 120kΩ
$t_{PWRGD-C}$	Minimum Time from PWRGD-B to PWRGD-C	3.0	5.0	8.0	ms	R_{TC} = 3kΩ
$t_{PWRGD-D}$	Maximum Time from PWRGD-C to PWRGD-D	150	200	250	ms	R_{TD} = 120kΩ
$t_{PWRGD-D}$	Minimum Time from PWRGD-C to PWRGD-D	3.0	5.0	8.0	ms	R_{TD} = 3kΩ
V_{RAMP}	Voltage on Ramp Pin in Current Limit Mode		3.6		V	(See Note 2)
$t_{STARTLIMIT}$	Start up Time Limit	80	100	120	ms	
t_{CBTRIP}	Circuit Breaker Delay Time	2.0		5.0	µs	May be extended by external RC circuit
t_{AUTO}	Automatic Retry Delay		16		s	

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Power Good Outputs (Referenced to V_{EE} pin)

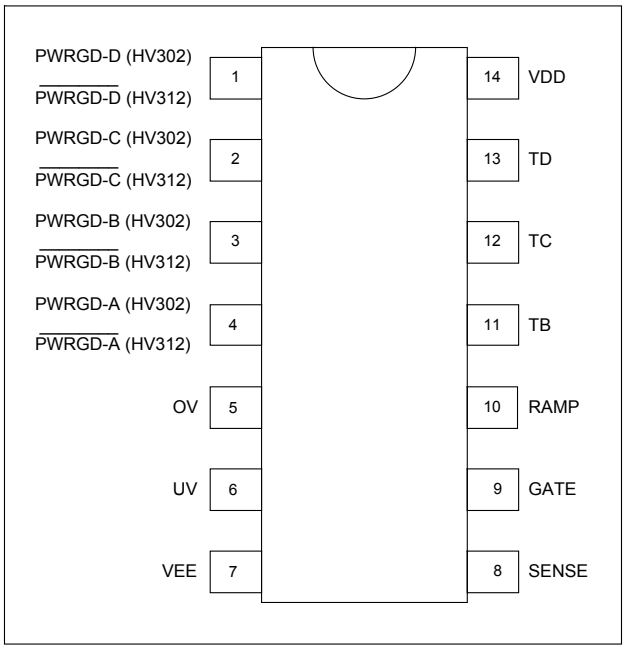
$V_{PWRGD-x(hi)}$	Power Good Pin Breakdown Voltage	90			V	PWRGD-x = HI Z
$V_{PWRGD-x(lo)}$	Power Good Pin Output Low Voltage		0.5	0.8	V	I_{PWRGD} = 1mA, PWRGD-x = LOW
$I_{PWRGD-x(lk)}$	Maximum Leakage Current		<1.0	10	µA	V_{PWRGD} = 90V, PWRGD-x = HI Z

Dynamic Characteristics

$t_{GATEHLOV}$	OV Comparator Transition			500	ns	
$t_{GATEHLUV}$	UV Comparator Transition			500	ns	

Note 1: This timing depends on the threshold voltage of the external N-Channel MOSFET. The higher its threshold is, the longer this timing.
Note 2: This voltage depends on the characteristics of the external N-Channel MOSFET. V_{to} = 3V for an IRF530.
*IRF530 is a registered trademark of International Rectifier.

Pinout



PWRGD Logic

Model	Condition	PWRGD-A/B/C/D	
HV302	INACTIVE (Not Ready)	0	V_{EE}
	ACTIVE (Ready)	1	HI Z
HV312	INACTIVE (Not Ready)	1	HI Z
	ACTIVE (Ready)	0	V_{EE}

Pin Description

PWRGD-D – This Power Good Output Pin is held inactive on initial power application and goes active a programmed time delay after PWRGD-C goes active.

PWRGD-C – This Power Good Output Pin is held inactive on initial power application and goes active a programmed time delay after PWRGD-B goes active.

PWRGD-B – This Power Good Output Pin is held inactive on initial power application and goes active a programmed time delay after PWRGD-A goes active.

PWRGD-A – This Power Good Output Pin is held inactive on initial power application and goes active when the external MOSFET is fully turned on.

OV – This Over Voltage (OV) sense pin, when raised above its high threshold will immediately cause the GATE pin to be pulled low. The GATE pin will remain low until the voltage on this pin falls below the low threshold limit, initiating a new start-up cycle.

UV – This Under Voltage (UV) sense pin, when below its low threshold limit will immediately cause the GATE pin to be pulled low. The GATE pin will remain low until the voltage on this pin rises above the high threshold limit, initiating a new start-up cycle.

V_{EE} – This pin is the negative terminal of the power supply input to the circuit.

V_{DD} – This pin is the positive terminal of the power supply input to the circuit.

TD – The resistor connected from this pin to V_{EE} pin sets the time delay from PWRGD-C going active to PWRGD-D going active.

TC – The resistor connected from this pin to V_{EE} pin sets the time delay from PWRGD-B going active to PWRGD-C going active.

TB – The resistor connected from this pin to V_{EE} pin sets the time delay from PWRGD-A going active to PWRGD-B going active.

RAMP – This pin provides a current output so that a timing ramp voltage is generated when a capacitor is connected.

GATE – This is the Gate Driver Output for the external N-Channel MOSFET.

SENSE – The current sense resistor connected from this pin to V_{EE} Pin programs the servo control current limit and the circuit breaker trip limit.

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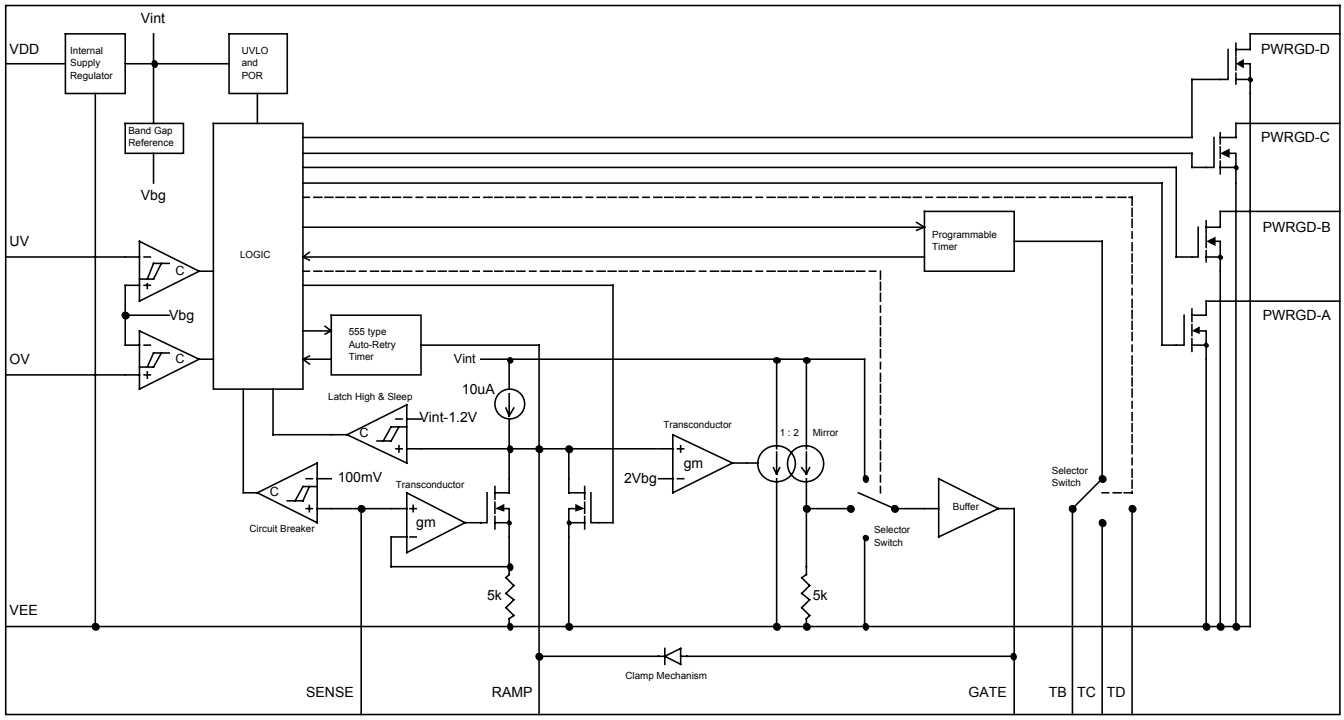
Functional Block Diagram



Functional Description

Insertion into Hot Backplanes

Telecom, Networking, SAN and Server applications require the ability to insert and remove circuit cards from systems without powering down the entire system. All circuit cards have some filter capacitance on the power rails, which is especially true in circuit cards or network terminal equipment utilizing distributed power systems. The insertion can result in high inrush currents that can cause damage to connector and circuit cards and may result in unacceptable disturbances on the system backplane power rails.

The HV302 and HV312 are designed to facilitate the insertion of these circuit cards or connection of terminal equipment by eliminating these inrush currents and powering up these circuits in a controlled manner after full connector insertion has been achieved

Description of Operation

During initial power application, a “normally-on” circuit holds off the external MOSFET, preventing an input glitch while an integrated regulator establishes an internal operating voltage of approximately 10V. Until the proper internal voltage is achieved all circuits are held reset, the PWRGD flags are inactive and the gate to source voltage of the external MOSFET is clamped low.

Once the internal under voltage lock out (UVLO) has been satisfied, the circuit checks the input supply under voltage (UV) and over voltage (OV) sense circuits to ensure that the input voltage is within programmed limits. These limits are determined by the selected values of resistors R1, R2 and R3, which form a voltage divider.

In **Servo Mode** operation, assuming the UV and OV limits are satisfied and while continuing to hold the PWRGD flags inactive and the external MOSFET GATE voltage low, the current source feeding the RAMP pin is turned on. The external ramp capacitor connected to it begins to charge, thus starting an initial time delay determined by the value of the capacitor and the 2Vbg threshold voltage of the RAMP pin. During this time if the OV or UV limits are exceeded, an immediate reset occurs and the capacitor connected to the RAMP pin is discharged.

When the voltage on the RAMP pin exceeds the 2Vbg threshold voltage, the gate drive circuit begins to apply voltage to the gate of the external MOSFET, which begins to turn on when its gate threshold voltage is reached. The resulting output current generates a voltage drop on the sense resistor connected between the SENSE and V_{EE} pins, causing a decrease in the available current charging the capacitor on the RAMP pin. This continuous feedback mechanism allows the output current to rise inverse exponentially over a period of a few hundred microseconds to the sense resistor programmed current limit set point.

When the voltage drop on the sense resistor reaches 50mV the RAMP pin current is reduced to zero and the voltage on the RAMP pin will be fixed, indicating that the circuit is in current limit mode. Depending on the value of the load capacitor and the programmed current limit, charging may continue for some time, but may not exceed a nominal 100ms preset time limit. Once the load capacitor has been charged, the output current will drop, reducing the voltage on the SENSE pin, which in turn will increase the RAMP pin current, thus causing the voltage on the capacitor connected to the RAMP pin to continue rising, thereby providing yet another programmed delay.

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Functional Description - *continued*

In **Feedback Capacitor Mode** operation, assuming the UV and OV limits are satisfied and while continuing to hold the PWRGD flags inactive and the external MOSFET GATE voltage low, the current source feeding the RAMP pin is turned on. The external ramp capacitor (C_{RAMP}) begins to charge and the feedback capacitor (C_{FB}) begins to discharge, thus starting an initial time delay determined by the equivalent value of the capacitors and the 2Vbg threshold voltage of the RAMP pin. During this time if the OV or UV limits are exceeded, an immediate reset occurs, the ramp capacitor is discharged and the feedback capacitor is recharged.

When the voltage on the RAMP pin exceeds the 2Vbg threshold voltage, the gate drive circuit begins to apply voltage to the gate of the external MOSFET, which begins to turn on when its gate threshold voltage is reached. However, the source current from the RAMP pin limits the dv/dt of the feedback capacitor (C_{FB}) which, in turn, programs the inrush current limit (I_{CL}) in accordance with the relationship $I_{CL} = I_{RAMP} \times C_{LOAD}/C_{FB}$ and thus the dv/dt of the load capacitor. At this point essentially all available current from the RAMP pin flows into the feedback capacitor, thus the voltage on the ramp capacitor and the RAMP pin remains essentially constant, thereby limiting and controlling the gate voltage of the external MOSFET (See Programming Current Limit and Circuit Breaker in Design Information section). When the load capacitor is fully charged the current flowing into the feedback capacitor is reduced and the voltage drop across the MOSFET essentially drops to zero, effectively connecting the feedback capacitor in parallel with the ramp capacitor. Now the current from the RAMP pin flows into the parallel-connected capacitors and the voltage on the RAMP pin begins to rise, thereby providing yet another programmed delay.

Whether operating in **Servo Mode** or **Feedback Capacitor Mode**, when the ramp voltage is within 1.2V of the regulated internal supply voltage, the controller will force the GATE terminal to a nominal 10V, the PWRGD-A pin will change to an active state and the Circuit Breaker is enabled. PWRGD-B will change to an active state a programmed delay time after PWRGD-A went active, PWRGD-C will change to an active state a programmed delay time after PWRGD-B went active, PWRGD-D will change to an active state a programmed delay time after PWRGD-C went active and the circuit transitions to a low power sleep mode. While in sleep mode the circuit continues to monitor the current and the OV and UV status.

When the voltage on the SENSE pin rises to 100mV, indicating an over current condition, the circuit breaker will trip in less than 5µs. This time may be extended by the addition of external components.

If due to output overload conditions during startup full charging of the load is not achieved within 100ms or a load fault occurs at any time the circuit breaker is tripped, the MOSFET is turned off by pulling down the GATE to V_{EE} and all four PWRGD flags are reset. Thereafter an auto-retry timer, programmed by the capacitor connected to the RAMP pin, will hold the pass device off to allow it to cool before resetting and restarting. The auto-retry can be disabled using a single resistor if desired (See Auto-Retry and Auto-Retry Disable in Design Information section).

At any time during the start up cycle or thereafter, crossing the UV and OV limits (including hysteresis) will cause an immediate reset of all internal circuitry. When the input supply voltage returns to a value within the programmed UV and OV limits a new start up sequence will be immediately initiated.

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Design Information

Programming Under and Over Voltage Shut Down

The UV and OV pins are connected to comparators with nominal 1.21V thresholds and 100mV of hysteresis (1.21V ± 50mV). They are used to detect under voltage and over voltage conditions at the input to the circuit. Whenever the OV pin rises above its high threshold (1.26V) or the UV pin falls below its low threshold (1.16V) the GATE voltage is immediately pulled low, the PWRGD pin changes to its inactive state and the external capacitor connected to the RAMP pin is discharged.

Calculations can be based on either the desired input voltage operating limits or the input voltage shutdown limits. In the following equations the shutdown limits are assumed.

The under voltage and over voltage shut down thresholds can be programmed by means of the three resistor divider formed by R1, R2 and R3. Since the input currents on the UV and OV pins are negligible the resistor values may be calculated as follows:

$$UV_{OFF} = V_{UVL} = 1.16 = \left|V_{EEUV(off)}\right| \times \frac{R2 + R3}{R1 + R2 + R3}$$

$$OV_{OFF} = V_{OVH} = 1.26 = \left|V_{EEOV(off)}\right| \times \frac{R3}{R1 + R2 + R3}$$

Where $\left|V_{EEUV(off)}\right|$ and $\left|V_{EEOV(off)}\right|$ are Under & Over Voltage Shut Down Threshold points.

If we select a divider current of 100µA at a nominal operating input voltage of 50 Volts then

$$R1 + R2 + R3 = \frac{50V}{100uA} = 500k\Omega$$

From the second equation for an OV shut down threshold of 65V the value of R3 may be calculated.

$$OV_{OFF} = 1.26 = \frac{65 \times R3}{500k\Omega}$$

$$R3 = \frac{1.26 \times 500K\Omega}{65} = 9.69k\Omega$$

The closest 1% value is 9.76kΩ

From the first equation for a UV shut down threshold of 35V the value of R2 can be calculated.

$$UV_{OFF} = 1.16 = \frac{35 \times (R2 + R3)}{500K\Omega}$$

$$R2 = \frac{1.16 \times 500k\Omega}{35} - 9.76k\Omega = 6.81k\Omega$$

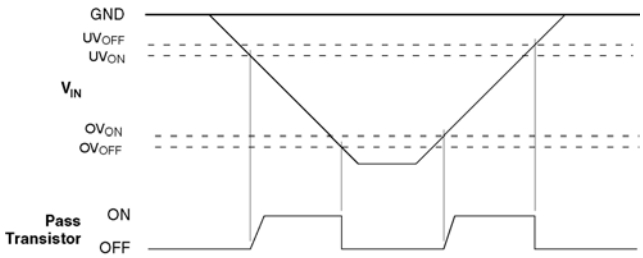
The closest 1% value is 6.81kΩ

Then

$$R1 = 500K\Omega - R2 - R3 = 483k\Omega$$

The closest 1% value is 487kΩ

Under Voltage/Over Voltage Operation



From the calculated resistor values the OV and UV start up threshold voltages can be calculated as follows:

$$UV_{ON} = V_{UVH} = 1.26 = \left|V_{EEUV(on)}\right| \times \frac{R2 + R3}{R1 + R2 + R3}$$

$$OV_{ON} = V_{OVL} = 1.16 = \left|V_{EEOV(on)}\right| \times \frac{R3}{R1 + R2 + R3}$$

Where $\left|V_{EEUV(on)}\right|$ and $\left|V_{EEOV(on)}\right|$ are Under & Over Voltage Start Up Threshold points.

Then

$$\left|V_{EEUV(on)}\right| = 1.26 \times \frac{R1 + R2 + R3}{R2 + R3}$$

$$\left|V_{EEUV(on)}\right| = 1.26 \times \frac{487k\Omega + 6.81k\Omega + 9.76k\Omega}{6.81k\Omega + 9.76k\Omega} = 38.29V$$

And

$$\left|V_{EEOV(on)}\right| = 1.16 \times \frac{R1 + R2 + R3}{R3}$$

$$\left|V_{EEOV(on)}\right| = 1.16 \times \frac{487k\Omega + 6.81k\Omega + 9.76k\Omega}{9.76k\Omega} = 59.85V$$

Therefore, the circuit will start when the input supply voltage is in the range of 38.29V to 59.85V.

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Design Information- *continued*

Programming Current Limit and Circuit Breaker

Feedback Capacitor Mode Operation

In this operating mode the circuit breaker trip current and the inrush current limit can be independently programmed. In fact the circuit breaker can be completely disabled by setting R_{SENSE} = 0Ω.

The circuit breaker will trip in less than 5µs when the voltage on the SENSE pin is raised 100mV above the V_{EE} pin and the value of the sense resistor may be calculated from the following equation:

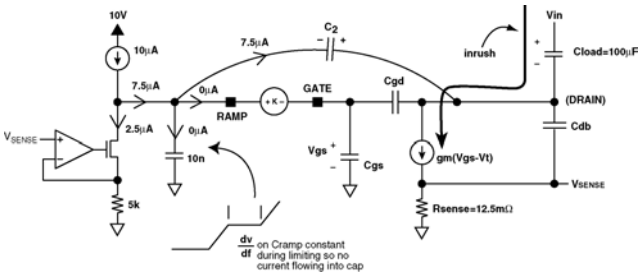
$$R_{SENSE} = \frac{V_{SENSE\text{-}CB}}{I_{CB}} = \frac{100mV}{I_{CB}}$$

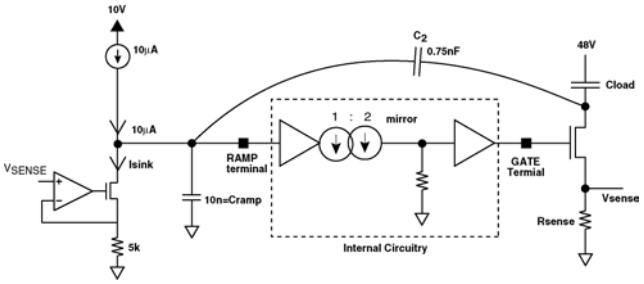
For an 8A circuit breaker:

$$R_{SENSE} = \frac{100mV}{8A} = 12.5m\Omega$$

The power rating of the sense resistor must be greater than or equal to I_{CB} x $V_{SENSE\text{-}CB}$.

The following diagrams depict the equivalent circuitry to clarify the feedback capacitor operation for programming the inrush current limit.





The inrush current limit may be programmed as follows:

Choose inrush current limit, for example I_{CL} = 1A

Calculate $I_{SINK} = \frac{I_{CL} \times R_{SENSE}}{5k\Omega} = \frac{1A \times 12.5m\Omega}{5k\Omega} = 2.5\mu A$

If the Circuit Breaker function is disabled by setting R_{SENSE} = 0Ω, then I_{SINK} = 0A. However, in this example we assume that the Circuit Breaker function is enabled and therefore use I_{SINK} = 2.5µA.

Calculate C2 (feedback capacitor) discharge current

$$I_{C2} = 10\mu A - I_{SINK} = 10\mu A - 2.5\mu A = 7.5\mu A$$

If Auto-Retry is disabled an adjustment must be made to I_{C2}

$$I_{AUTO} = \frac{V_t}{R_{DISABLE}} = \frac{4V}{2.5M\Omega} = 1.6\mu A$$

Where Vt is the maximum threshold voltage of the MOSFET.

Therefore, the adjusted value of I_{C2} is:

$$I_{C2} = 10\mu A - I_{SINK} - I_{AUTO}$$
$$I_{C2} = 10\mu A - 2.5\mu A - 1.6\mu A = 5.9\mu A$$

In this example we assume that Auto-Retry is enabled and therefore use I_{C2} = 7.5µA.

Note that $I_{C2} = C2 \times \frac{dv}{dt}$ and $I_{CL} = C_{LOAD} \times \frac{dv}{dt}$

Since V_{IN} is fixed and V_{RAMP} is constant during limiting, then $\frac{dv}{dt}$ across C_{LOAD} = $\frac{dv}{dt}$ across C2 as they share a common node and their other terminals are at fixed voltages during inrush current limiting. Therefore, $\frac{I_{C2}}{C2} = \frac{I_{CL}}{C_{LOAD}}$ or $C2 = \frac{I_{C2} \times C_{LOAD}}{I_{CL}}$.

As previously calculated and by conservation of charge on RAMP node I_{C2}=7.5µA based on the chosen inrush current limit of I_{CL}=1A. Given that C_{LOAD}=100µF the required value for C2 can be calculated.

Therefore $C2 = \frac{I_{C2} \times C_{LOAD}}{I_{CL}} = \frac{7.5\mu A \times 100\mu F}{1A} = 0.75nF$

Note that during initial power application the RAMP pin is voltage protected by the capacitive AC voltage divider consisting of C_{LOAD}, C2 and C_{RAMP} and the GATE pin is internally clamped.

Servo Control Mode Operation

The circuit breaker will trip in less than 5µs when the voltage on the SENSE pin is raised 100mV above the V_{EE} pin and the value of the sense resistor may be calculated from the following equation:

$$R_{SENSE} = \frac{V_{SENSE\text{-}CB}}{I_{CB}} = \frac{100mV}{I_{CB}}$$

For a 2A circuit breaker:

$$R_{SENSE} = \frac{100mV}{2A} = 50m\Omega$$

The power rating of the sense resistor must be greater than or equal to I_{CB} x $V_{SENSE\text{-}CB}$.

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Design Information- *continued*

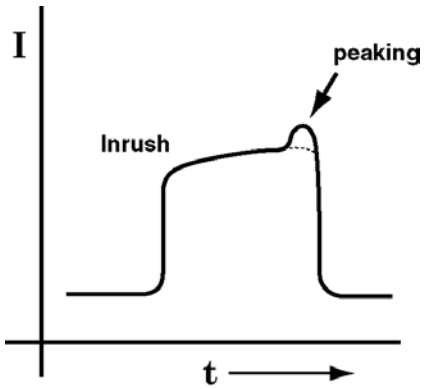
The inrush current limit can be calculated as follows:

$$I_{CL} = \frac{V_{SENSE\text{-}CL}}{R_{SENSE}} = \frac{50mV}{R_{SENSE}}$$

Thus the inrush current limit for a 2A circuit breaker:

$$I_{CL} = \frac{50mV}{50m\Omega} = 1A$$

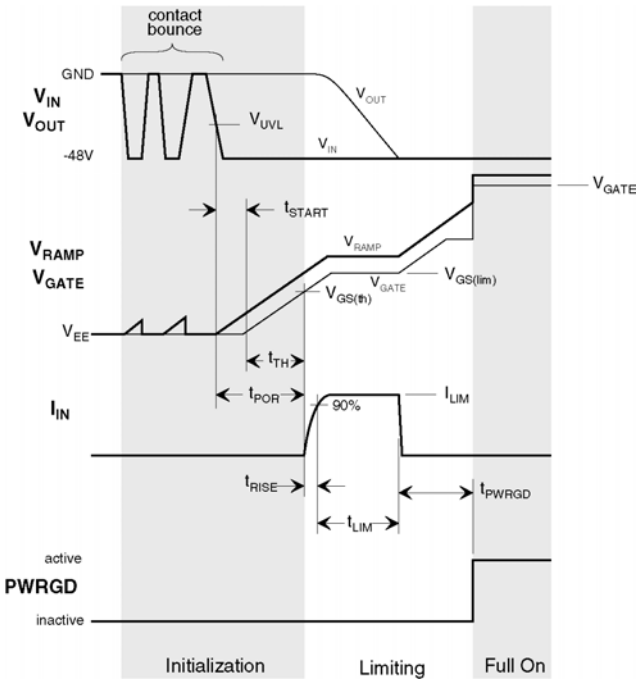
Compensation components from gate to source of the external MOSFET may be required to reduce peaking of the inrush current.



Compensation can be accomplished as follows:

1. Start with a 2nF capacitor from gate to source.
2. Increase capacitor value up to 10nF if needed.
3. If needed, add a 1kΩ resistor in series with the above capacitor.

Servo Mode Timing



The timing functions are defined by the following equations:

$$t_{START} = 2.4\frac{C_{RAMP}}{I_{RAMP}}$$

$$t_{TH} = V_{GS(th)}\frac{C_{RAMP}}{I_{RAMP}}$$

$$t_{POR} = t_{START} + t_{TH}$$

$$t_{RISE} \approx \frac{C_{RAMP}}{g_{fs}\left(\frac{I_{RAMP}}{0.9I_{LIMIT}} - \frac{R_{SENSE}}{R_{FB}}\right)}$$

$$t_{LIMIT} \approx V_{IN}\frac{C_{LOAD}}{I_{LIMIT}}$$

$$t_{PWRGD-A} = \left(V_{INT} - V_{GS(LIMIT)} - 1.2\right)\frac{C_{RAMP}}{I_{RAMP}}$$

These equations assume that the load is purely capacitive and the following definitions apply.

C_{RAMP} is the external capacitor connected to the RAMP pin.

I_{RAMP} is the output current from the RAMP pin, nominally 10µA, when the voltage drop on R_{SENSE} resistor is zero.

V_{INT} is the internally regulated supply voltage and can range from 9V to 11V.

$V_{GS(th)}$ is the gate threshold voltage of the external pass transistor and may be obtained from its datasheet.

$V_{GS(limit)}$ is the external pass transistor gate-source voltage required to obtain the limit current. It is dependent on the pass transistor's characteristics and may be obtained from the transfer characteristics on the transistor datasheet.

g_{fs} is the transconductance of the external pass transistor and may be obtained from its datasheet.

R_{FB} is the internal feedback resistor and is nominally 5KΩ.

I_{LIMIT} is the load current when the voltage drop on R_{SENSE} resistor is 50mV.

These equations may be used to calculate the minimum value of C_{RAMP} for the most critical system performance characteristics.

For maximum contact bounce duration protection choose a value for t_{POR} and use the following equation:

$$C_{RAMP} = \frac{t_{POR} \times I_{RAMP}}{2.4 + V_{GS(limit)}}$$

If control of PWRGD active delay is the critical system parameter, then choose a value for $t_{PWRGD-A}$ and use the following equation:

$$C_{RAMP} = \frac{t_{PWRGD-A} \times I_{RAMP}}{V_{INT} - V_{GS(limit)} - 1.2}$$

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Design Information - *continued*

Start up Overload Protection

Start up must be achieved within a nominal 100ms as indicated by the PWRGD-A pin transition to the active state or the circuit will reset and an Auto-Retry will initiate. If there is an output overload or short circuit during start up, the circuit will be in current limit mode for the 100ms time limit (in servo mode). In feedback capacitor mode the circuit breaker will shutdown the MOSFET before 100ms.

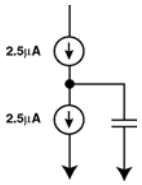
Circuit Breaker Delay

The circuit breaker will trip in less than 5µs when the voltage on the SENSE pin reaches a nominal 100mV. A resistor in series with the SENSE pin and a capacitor connected between the SENSE and VEE pins may be added to delay the rate of voltage rise on the SENSE pin, thus permitting a current overshoot and delaying Circuit Breaker activation. This method is particularly useful when operating in Feedback Capacitor Mode. However, in Servo Mode operation it will result in a current limit leading edge overshoot.

Auto-Retry and Auto-Retry Disable

The Auto-Retry delay time is directly proportional to the capacitance at the RAMP pin. Auto-Retry sequence is activated whenever the 100ms timeout is reached during start up or the Circuit Breaker is tripped.

Auto-Retry can be approximated as a 555-timer with 2.5µA charge up and charge down currents through 8V, to a count of 256.



Therefore,

$$t_{Auto-Retry} = \frac{2 \times 8 \times 256}{2.5\mu A} \times C_{RAMP}$$

For C_{RAMP} = 10nF

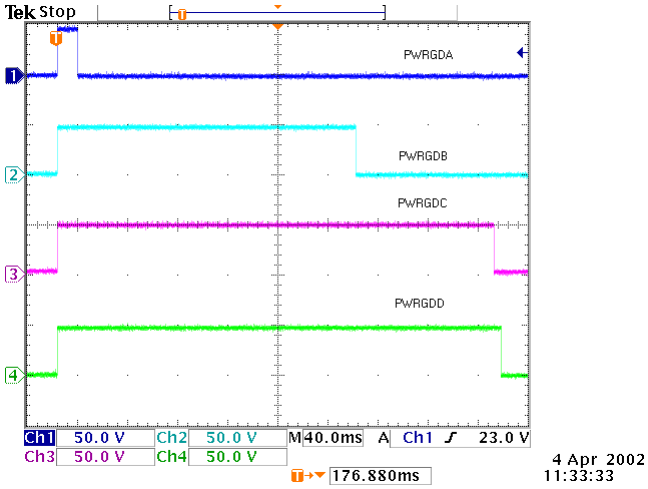
$$t_{Auto-Retry} = \frac{2 \times 8 \times 256}{2.5\mu A} \times 10nF = 16.4s$$

Due to the 2.5µA maximum charge current a resistor which draws more than 2.5µA below 8V will disable Auto-Retry. Try to keep this resistor as big as possible, e.g. 2.5MΩ. For most MOSFETs with maximum Vt of 4V, this will vary the 10µA RAMP current source by only $\frac{4V}{2.5M\Omega} = 1.6\mu A$

PWRGD Flag Delay Programming

Shortly after current limiting ends, PWRGD-A becomes active indicating successful completion of the Hotswap operation. PWRGD-B will change to an active state a programmed delay time after PWRGD-A went active, PWRGD-C will change to an active state a programmed delay time after PWRGD-B went active and PWRGD-D will change to an active state a programmed delay time after PWRGD-C went active. Resistors connected from the respective TB, TC and TD pins to V_{EE} pin are used to program the delay times between the PWRGD flags sequentially going active.

The following waveforms demonstrate the sequencing of the PWRGD flags. These results were obtained with R_{TB} = 120kΩ, R_{TC} = 60kΩ and R_{TD} = 3kΩ



The value of the resistors determines the capacitor charging and discharging current of a triangle wave oscillator. The oscillator output is fed to an 8-bit counter to generate the desired time delay.

The respective delay time is defined by the following equation:

$$t_{TX} = \frac{255 \times 2 \times C_{OSC} \times V_{PP}}{I_{CD}}$$

and

$$I_{CD} = \frac{V_{bg}}{4R_{TX}}$$

Where t_{TX} = Delay Time between respective PWRGD flags
C_{OSC} = 120pF (Internal oscillator capacitor)
V_{PP} = 8.2V (Peak-to-Peak voltage swing of oscillator)
I_{CD} = Charge and Discharge current of oscillator
Vbg = 1.2V (Internal Band Gap Reference)
R_{TX} = Programming resistor at TB, TC or TD pin

Combining the above two equations and solving for R_{TX} yields:

$$R_{TX} = \frac{B_{bg} \times t_{TX}}{2040 \times C_{PP} \times V_{PP}} = \frac{1.2V \times t_{TX}}{2040 \times 120pF \times 8.2V}$$

$$R_{TX} = 0.6 \times 10^{6} \times t_{TX}$$

For a delay time of 200ms we get:

$$R_{TX} = \left(0.6 \times 10^{6}\right) \times \left(200 \times 10^{-3}\right) = 120k\Omega$$

For a delay time of 5ms we get:

$$R_{TX} = \left(0.6 \times 10^{6}\right) \times \left(5 \times 10^{-3}\right) = 3k\Omega$$

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Design Information - *continued*

Supported External Pass Devices

The HV302 and HV312 are designed to support N-Channel MOSFETs and IGBTs.

Selection of External Pass Devices

The $R_{DS(ON)}$ of the device is likely to be selected based on allowable voltage drop at maximum load ($I_{LOAD(MAX)}$) after the Hotswap action has been completed. Thus the required continuous power dissipation rating (P_{CONT}) of the device can be determined from the following equation:

$$P_{CONT} = R_{DS(ON)} \times I^2_{LOAD(MAX)}$$

The peak power rating (P_{PEAK}) should be based on the highest current level, which is always the circuit breaker trip set point (I_{CB}), and on the assumption that a output is shorted. The peak power rating may be calculated from the following equation:

$$P_{PEAK} = V_{IN} \times I_{CB}$$

Given these values an external pass transistor may be selected from the manufacturers data sheet.

Paralleling External Pass Transistors

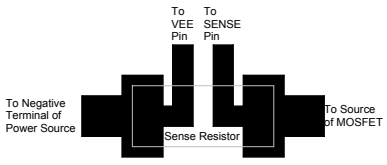
Due to variations in threshold voltages and transconductance characteristics between samples of MOSFETs, reliable 50% current sharing is not achievable. Some measure of paralleling may be accomplished by adding resistors in series with the source of each device; however, it will cause increased voltage drop and power dissipation.

Paralleling of external Pass devices is not recommended!

If a sufficiently high current rated external pass transistor cannot be found then increased current capability may be achieved by connecting independent Hotswap circuits in parallel, since they act as current sources during the load capacitor charging time when the circuits are in current limit. For this application the HV302 with active high PWRGD is recommended where the PWRGD pins of multiple Hotswap circuits can be connected in a wired OR configuration.

Kelvin Connection to Sense Resistor

Physical layout of the printed circuit board is critical for correct current sensing. Ideally trace routing between the current sense resistor and the V_{EE} and SENSE pins should be direct and as short as possible with zero current in the sense traces. The use of Kelvin connection from SENSE pin and V_{EE} pin to the respective ends of the current sense resistor is recommended.



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