Dual Triple DMOS Output Driver with Serial Input Control T6817

T6817
Driver ICs

Application Note

1. Introduction

The T6817 is a fully-protected universal driver interface designed in 0.8-µm BCDMOS technology. It is used to control up to 6 different loads by a microcontroller in automotive and industrial applications.

Each of the 3 high-side and 3 low-side drivers is capable of driving currents up to 600 mA. The drivers are freely configurable and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors, and inductors can be combined. The IC design particularly supports applications of H-bridges to drive DC motors.

Protection against short-circuit conditions, overtemperature, under- and overvoltage is implemented. Various diagnostic functions and a very low quiescent current in standby mode enable a wide range of applications. Automotive qualification with respect to conducted interferences, EMC and 2-kV ESD protection gives added value and enhanced quality for the demands of highly-sophisticated applications.

2. Development Board

The development board includes the following components:

- T6817 design software
- Link cable to PC 25-lead 1:1
- Application note
- Datasheet “T6817: Dual Triple DMOS Output Driver with Serial Input Control”

2.1 Description

By means of the PC-controlled development board, a user can adapt the loads (see Figure 2-2 on page 3) easily via row connector pins. The design software interface controls the development board.

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2.2 Features

- Row connector pins for external loads switched by low- or high-side drivers
- Easy adaptation of loads directly on the T6817 application board
- Direct switch of loads to V_S or GND
- Forward/reverse rotation of DC motors by full-bridge application
- Paralleling of outputs for powerful applications
- PC adaptation via standard SUB-D connectors (plug 3 or plug 4, see Figure 2-2 on page 3)
- PC-controlled functions via software user interface
- 5-V power supply on-board, activable by jumper J7, J8
- Signaling output state by LED, activable by J1 to J6

Figure 2-1. Block Diagram

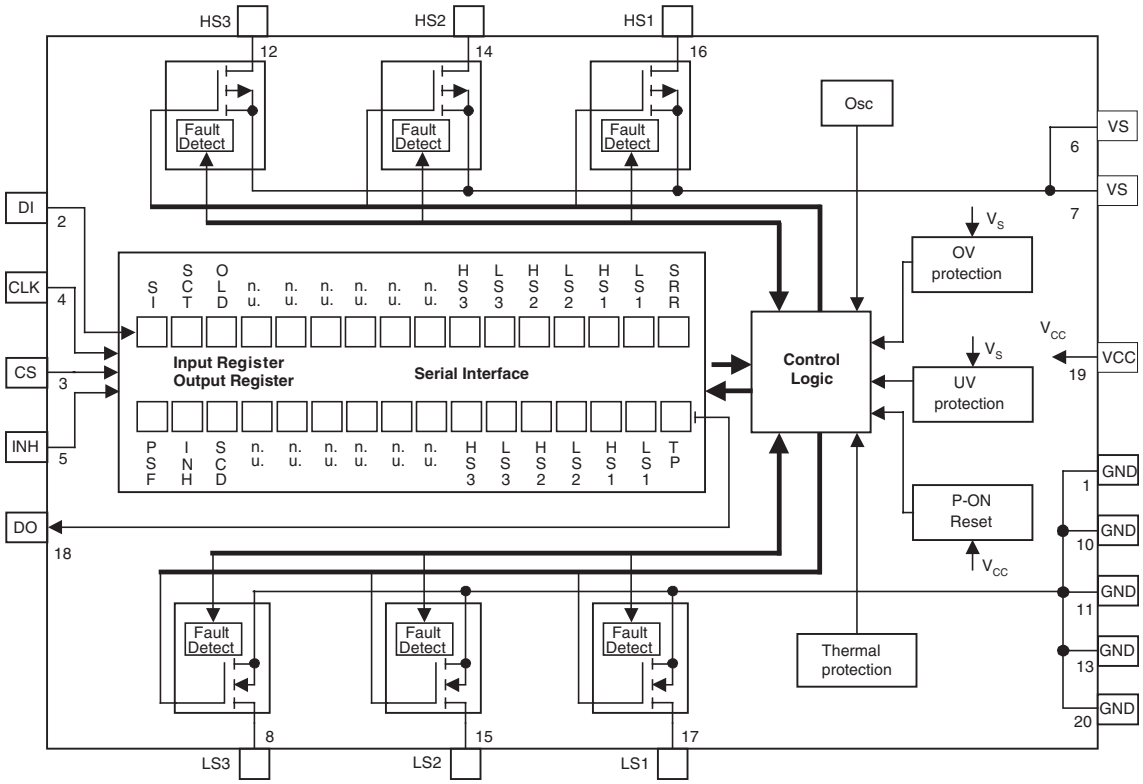


Figure 2-2. T6817 Development Board Schematic

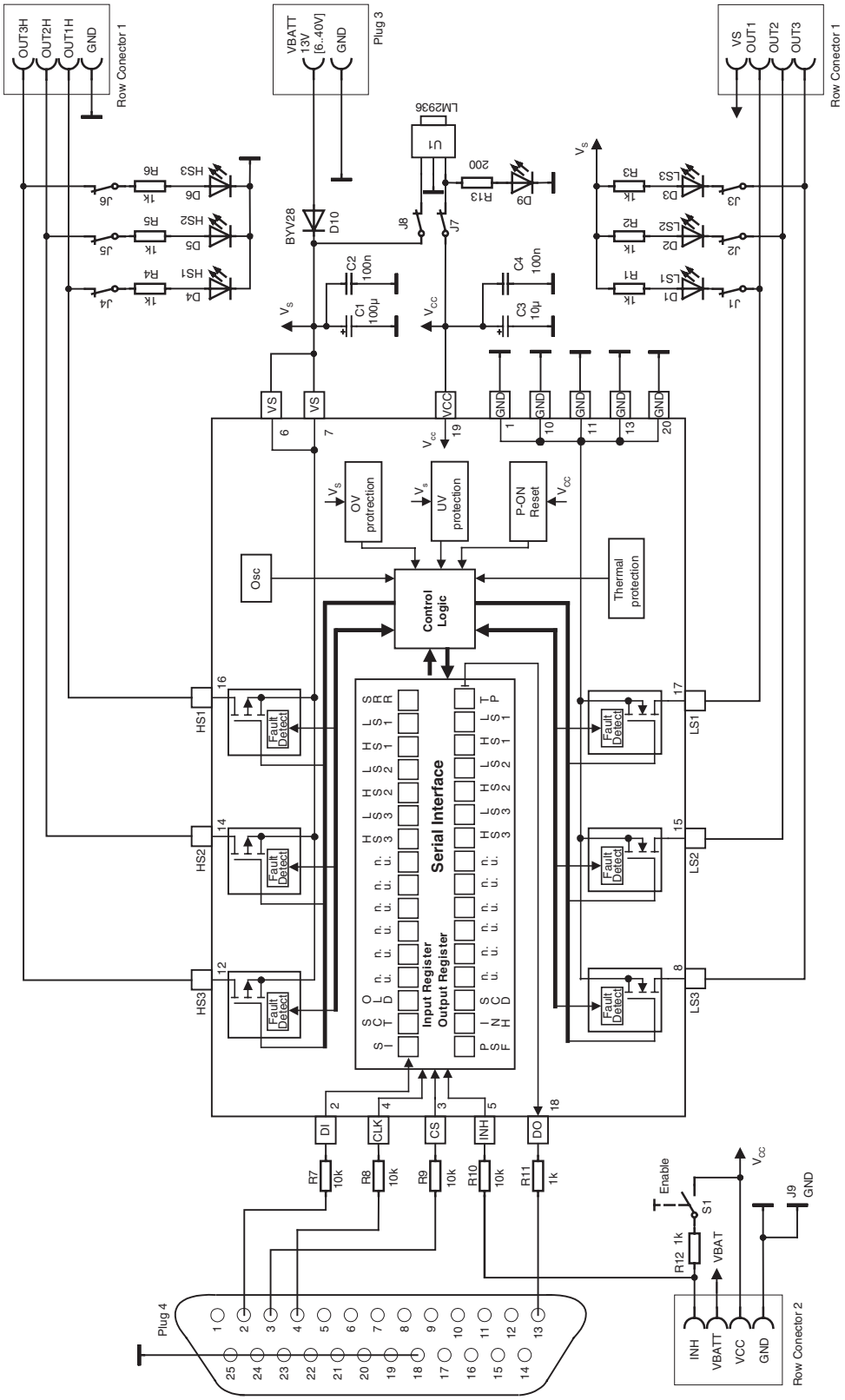


Figure 2-3. ATAB6817 Basic Application Board Component Placement; Top Side, Top View

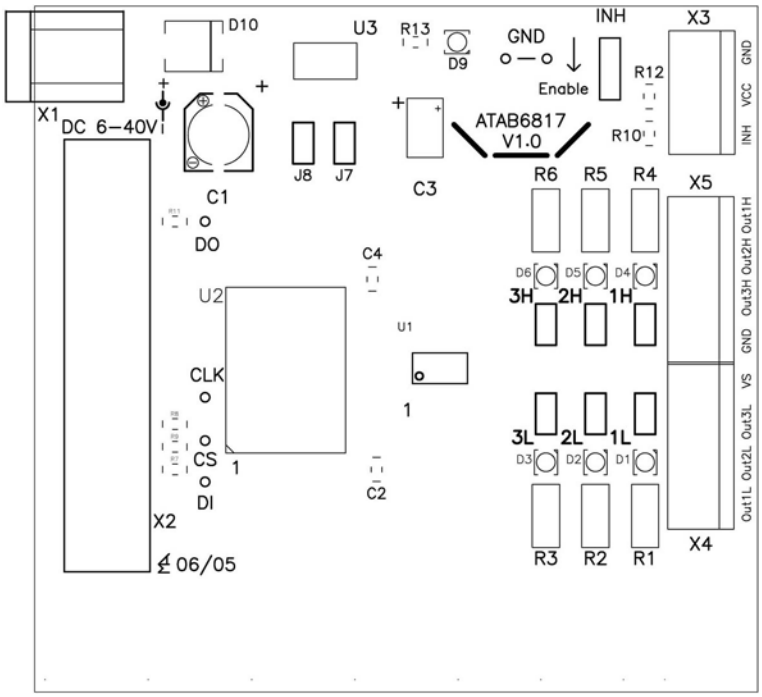


Figure 2-4. ATAB6817 Basic Application Board Top Side, Top View

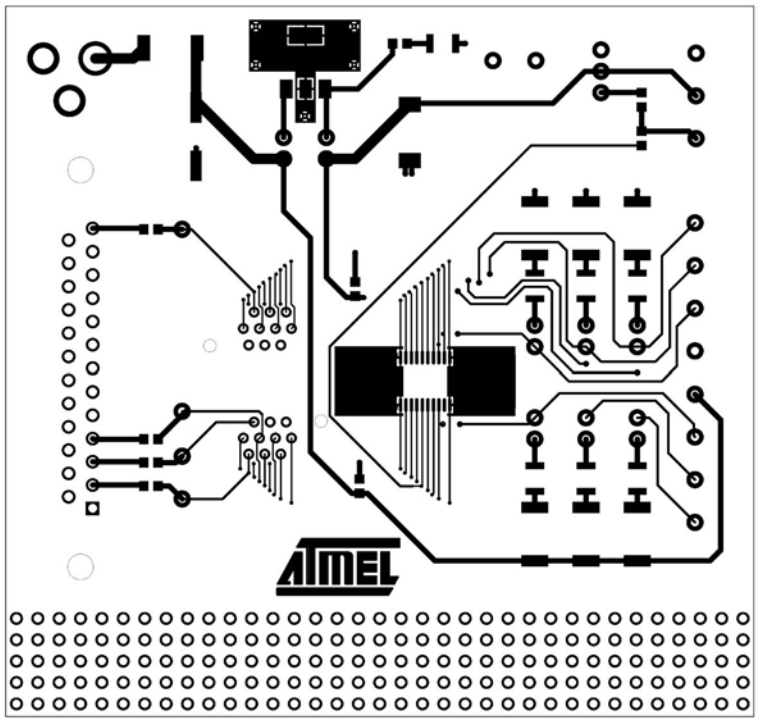
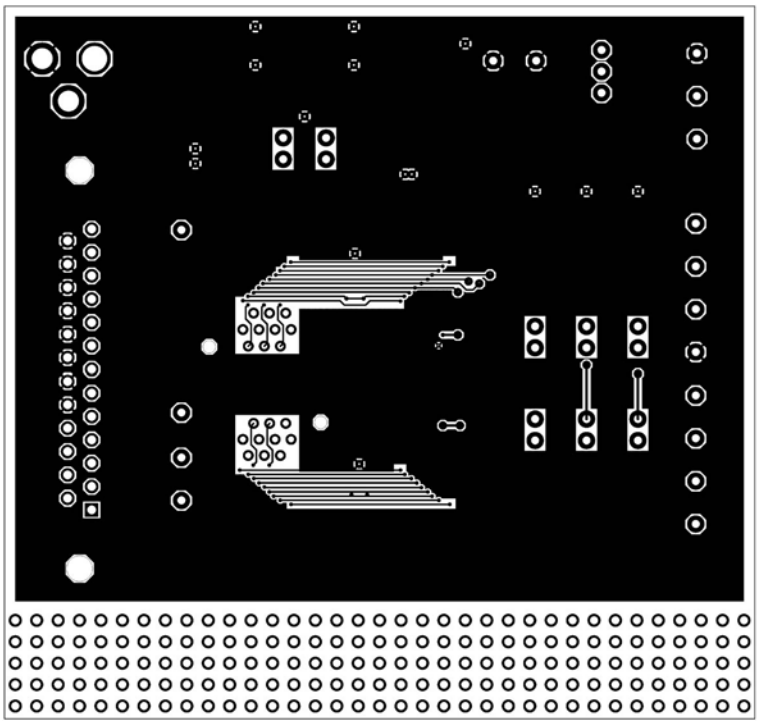


Figure 2-5. ATAB6817 Basic Application Board Bottom Side, Top View (as if PCB were transparent)

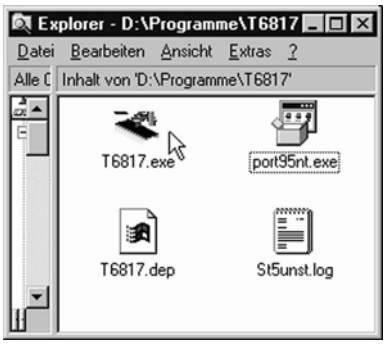


3. Design Software

3.1 Installation

The T6817 development board includes the software T6817. The user can also download the software from the company's website, www.atmel.com. After the download, the installation process can be launched by starting the downloaded *.exe* file. The T6817.exe file is transferred to a user-defined directory (for example, D:\T6817), and the system files are then transferred to the system directories, finishing the installation. The PC parallel port is connected via the enclosed link cable with the development board. Double-clicking on the T6817 icon (refer to Figure 3-1) starts the software user interface.

Figure 3-1. Software Icon



3.2 Description

The T6817 development board along with the software user interface shows the principal functions of the T6817 and enables the designer to directly create a design according to current needs. The software user interface includes all parts of the T6817 and provides convenient control of the T6817 via the development board. Pre-adjustment of the required input data is realized by means of the adjust register (representing the microcontroller) on the left side in the software user interface (see Figure 3-2 on page 7). By clicking the *Send Data* button, the pre-adjusted data (16 bits) is shifted into the input register of the serial data interface and the output drivers are activated in accordance with the 16-bit operation command. For more detailed information regarding the serial data interface, please refer to the datasheet.

The *Send Data Loop* button causes an uninterrupted data transfer. Thus, each output is directly adjusted by switching the accessory bit.

The *Reset* button resets all bits to the start condition. The software is switched off by clicking on the *End* button.

If available, up to three parallel interface ports (LPT1, LPT2 and LPT3) can be selected to establish the proper connection.

By default, 3 input registers are set with the following status:

- SI = Software inhibit is set high for normal operation
- SCT = Short-circuit and overvoltage time delay is set high for a 100 ms/15 ms delay
- OLD = Open-load detection is off when set high

Before the first dataword is sent, the IC is in standby (inhibit) mode. As soon as the 1st dataword is sent, the IC reports the previous condition, that is, the INH bit register is set in the output. After the second dataword, the INH bit disappears.

1. Set inhibit switch on
2. Select *Send Data Loop*
3. Select load to operate

3.3 Ordering Information

Please contact your appropriate Atmel Sales Office or Distributor.

Figure 3-2. Software User Interface

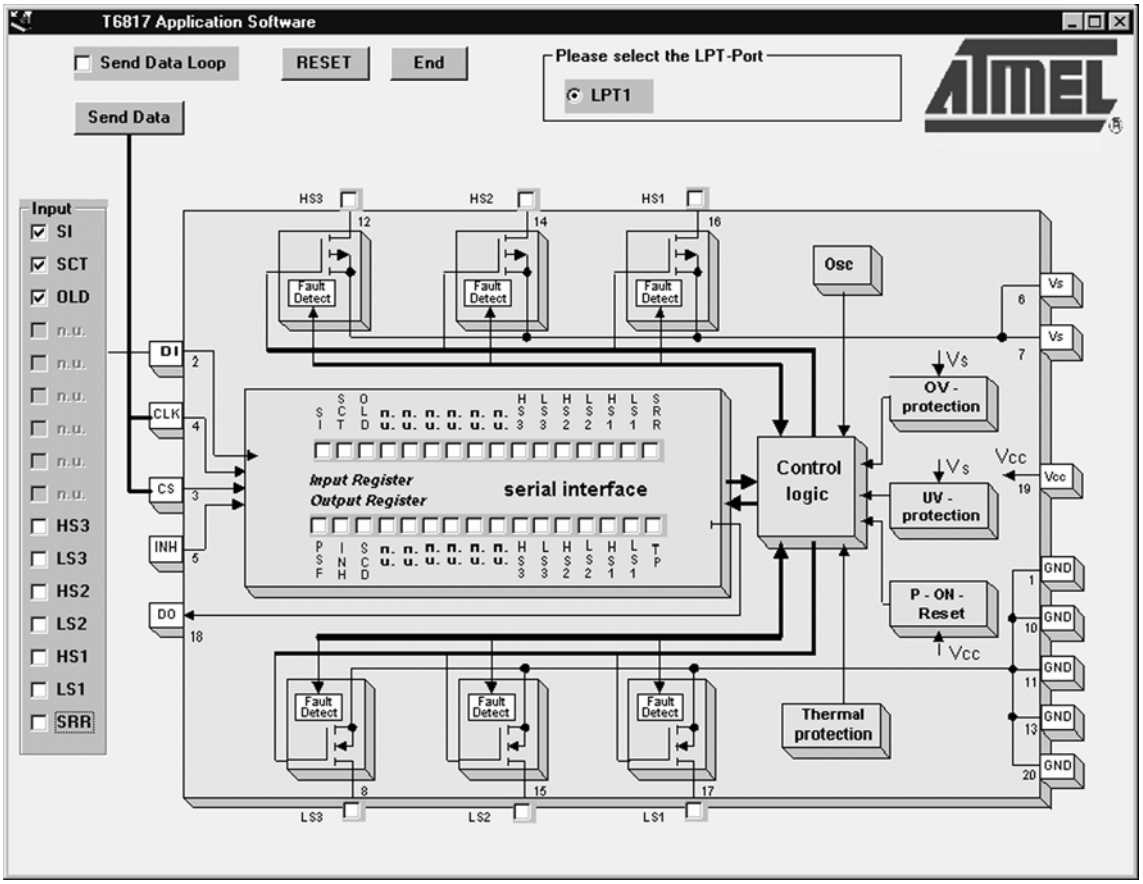


Table 3-1. Functions of the Serial Interface Register Bits

Bit	Input Register	Function
0	SRR	Status register reset (high = reset, the bits PSF, SCD, and overtemperature shutdown in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	n.u.	Not used
8	n.u.	Not used
9	n.u.	Not used
10	n.u.	Not used
11	n.u.	Not used
12	n.u.	Not used
13	OLD	Open-load detection (low = on)
14	SCT	Programmable time delay for short-circuit and overvoltage shutdown (short-circuit shut-down delay high/low = 100 ms/12.5 ms, overvoltage shutdown delay high/low = 15 ms/3.5 ms)
15	SI	Software inhibit; low = standby, high = normal operation (data transfer is not affected by the standby function because the digital part is still powered)

4. Applications

4.1 Demonstration Application

A typical demonstration application consists of a dual full bridge arrangement with microcontroller and watchdog to control two DC motors. Such a dual H-bridge arrangement with common mid rail allows for independent control of the motors for both directions of rotation. Enter the appropriate dataword according to Table 4-1 on page 9 to set the desired function.

When being operated in a safety-critical environment, the use of a separate watchdog IC (such as U5021M) is recommended.

If *OLD* is activated, the open load detection is active for all output stages that are currently switched off. A pull-up current for each high-side switch and a pull-down current for each low-side switch is turned on (open-load detection current I_{HS1-3}, I_{LS1-3}). If V_{VS} - V_{HS1-3} or V_{LS1-3} is lower than the open-load detection threshold, an open-load is detected: the corresponding bit of the output in the output register is set to high. Please note that for the proposed demonstration application all low-side drivers of H-bridges are detected as open loads. This behavior is caused by the low-side open-load detection current being larger than its high-side counterpart. This configuration also ensures that with half- or H-bridge applications the open-load detection works in a well-defined way. If, for example, an open load at motor M1 should be detected, HS1 or HS2 has to be switched on, while the diametrical low-side output register LS2 and LS1, respectively, has to be evaluated.

If INH is activated (by software inhibit bit SI or hardware inhibit), all activated loads are switched off, but the input and output registers remain set.

Short-circuit detection can easily be demonstrated by intentionally false activation of the H-bridge components, for example, HS1 and LS1. The SCD bit in the output register will be set and can be reset by activating the SRR bit. Please note that such activation of SRR just initiates a reset pulse, not a permanent reset state.

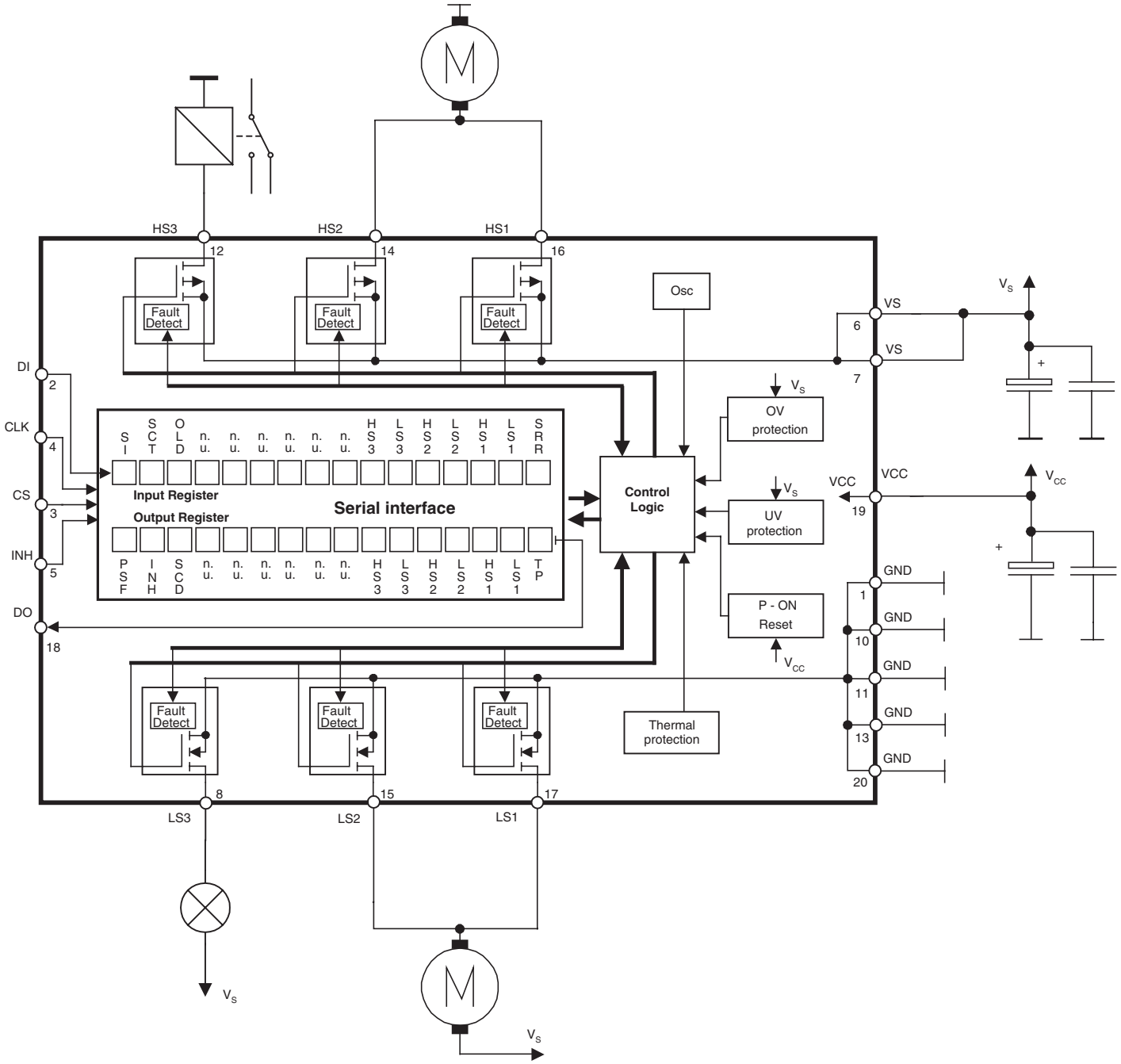
If any high-side driver is connected to a low-side one to form a half-bridge, switching from HS active to LS active or vice versa with a single programming sequence may cause some shoot-through current peak across both drivers during the switching operation. Those peaks can last for several hundred microseconds, determined by the controlled slew rates in the course of switching. Thanks to the internal short-circuit protection such shoot-through currents will not have any negative impact on the circuit's long-term reliability. However, these current peaks may cause distortions on the power supply line; therefore, it is recommended to avoid shoot-through conditions by means of providing HS and LS control commands subsequently with adequate timing.

Over- and undervoltage detection can be demonstrated with a variable power supply. In both cases, as soon as the thresholds are exceeded (after the delay times t_{dUV} and the programmed t_{dOV}), all activated loads are switched off, and the PSF bit in the output register is set. If the voltage returns to the normal level, the loads are switched on again, but the PSF bit needs to be reset by SRR activation.

Table 4-1. Configuration Table of the Required Datawords to Set Certain Functions of the Circuit (see Figure 4-1 on page 10)

	Bit 15 (SI)	Bit 14 (SCT)	Bit 13 (OLD)	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
M1 Forward						H			H	
M1 Reverse							H	H		
M2 Forward				H			H			
M2 Reverse					H	H				

Figure 4-1. Application with Microcontroller and Watchdog



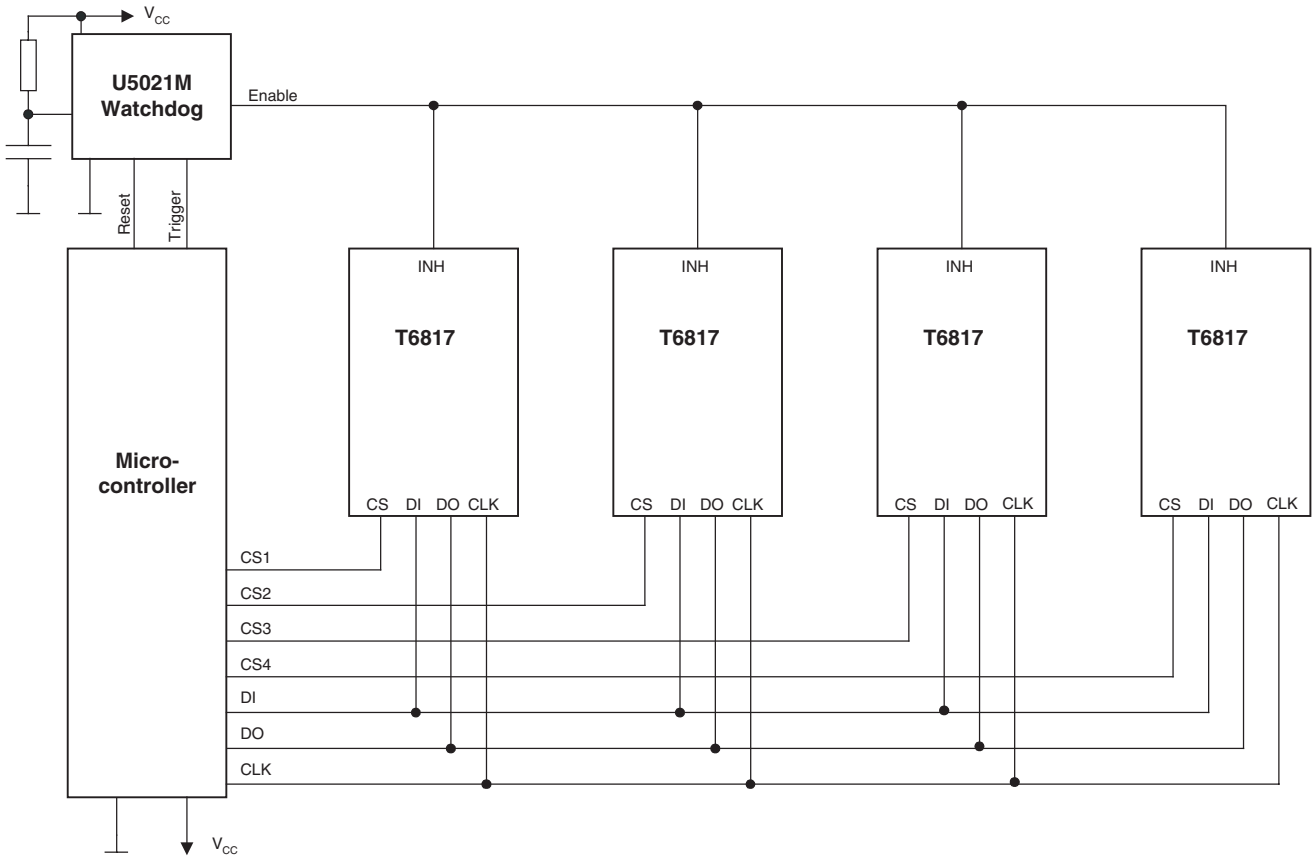
4.2 Parallel Operation of Several T6817s

In applications with a high number of loads, a straightforward parallel operation of the T6817 via the microcontroller is possible.

Separate control of the T6817's serial data interface is provided by chip select pins CS1 - CS4 (for the function of the serial data interface, please refer to the datasheet).

For simultaneous operation of the serial data interfaces (that is, CS1 through CS4 are active at the same time), each of the data outputs (DO) needs to communicate with a dedicated microcontroller input pin.

Figure 4-2. Parallel Operation with Microcontroller and Watchdog



4.3 Daisy Chaining of Several T6817s

In applications with a larger number of loads, there is a second possibility to connect several T6817 to the microcontroller. The daisy-chain arrangement requires only one CS line, the data signal is handed over step by step from one T6817 to the next as long as the CS signal stays low. It is quite evident that such advantage is purchased with slower reaction times, as several programming cycles are needed to load the desired setting into each T6817.

The DI pin of the first IC acts as input for all ICs while the DO of the last IC represents the output for the whole chain. The data word intended for the last IC has to be put in first, followed by the word for the IC before, and so on. In contrary to other ICs of the Atmel driver family, only *n* shifts total will be needed for a number of *n* ICs, as any DI information is transferred immediately to the output register.

Table 4-2 clarifies this method: the n = 3 data words A, B, C are to be shifted into the driver ICs number 1, 2 and 3, while the initial contents of the registers are shown as X. It can be seen that the desired status of the input registers DI is reached after n = 3 shift operations.

Figure 4-3. Daisy Chain Operation with Microcontroller and Watchdog

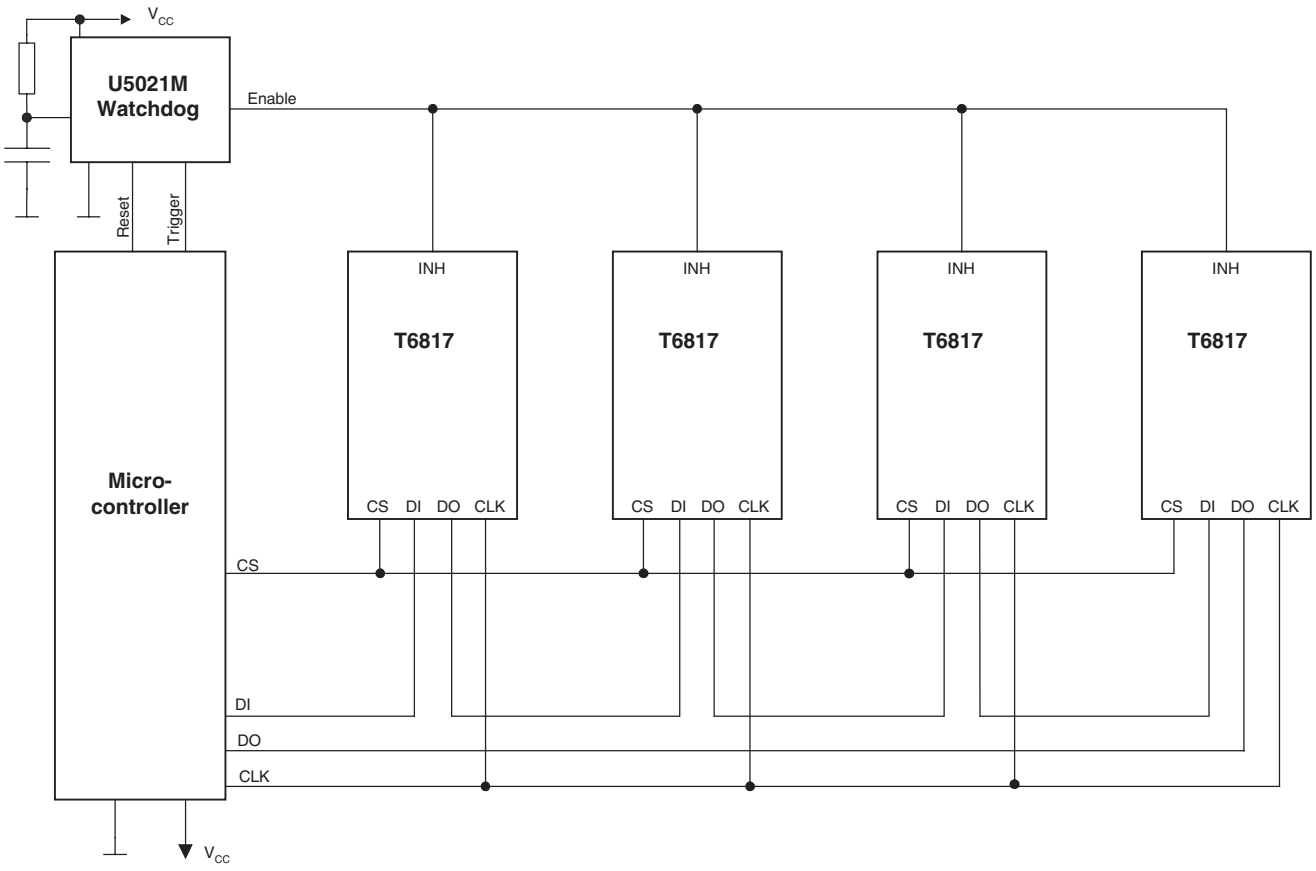


Table 4-2. Principal Method of Shifting Data Words Through Daisy-chained ICs

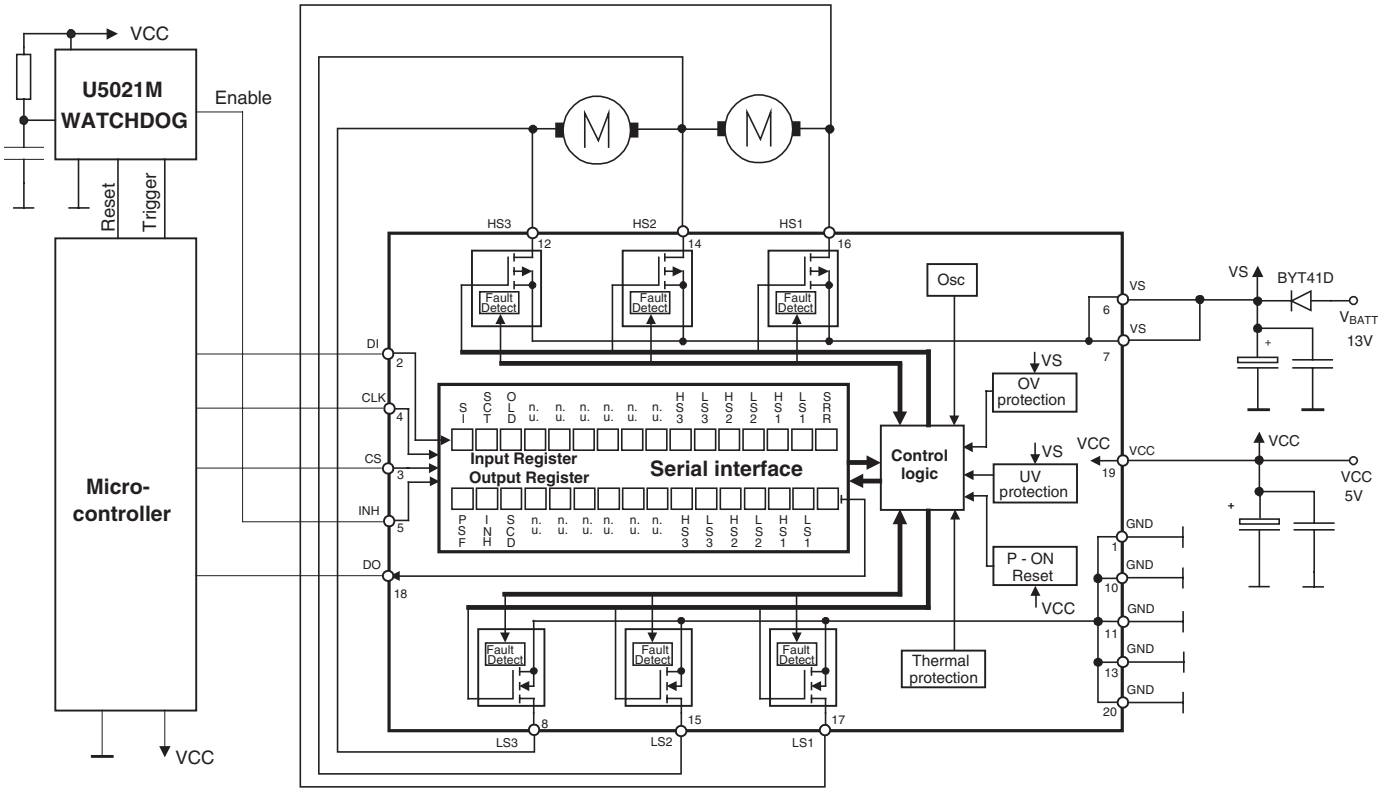
I/O Cycle	0			1			2		
IC number	1	2	3	1	2	3	1	2	3
DI	A	X	X	B	A	X	C	B	A
DO	X	X	X	A	X	X	B	A	X

4.4 Paralleling of Outputs

For more powerful applications with currents up to 1.2A (see Figure 4-4), parallel operation of output stages is possible under the following restrictions:

- Paralleling of LS1 - LS3 is permitted
- Paralleling 2 of the high-side stages HS1, HS2 or HS3 is permitted
- Maximum power dissipation has to be considered

Figure 4-4. DC Motor Application with Parallel Outputs



5. Thermal Considerations

5.1 Cooling Area Design

It is strongly recommended that the IC be connected to a cooling area on-board. All thermal pins (4 GND pins) are directly connected to the cooling area. Figure 5-1 shows the cooling arrangement with the SSO20 package of the T6817. The increase or decrease of the cooling area extension has to be done according to the required power dissipation (see Figure 5-2). The cooling area extension is calculated as follows: $2 \times L^2$ = cooling area extension [mm^2].

The effect of the cooling area on the PCB can be further improved if the bottom side of the PCB is ground-plated and thermal vias are placed along the cooling area. A via diameter of 0.3 mm to 0.4 mm and a spacing of 1 mm to 1.5 mm has proven to be most suitable. Some care should be taken of the copper area's planarity, solder bumps arising at the thermal vias should especially be avoided.

Figure 5-1. Recommended Cooling Area Extension

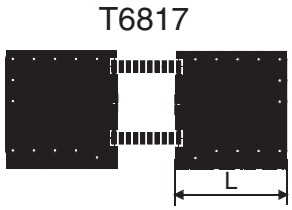
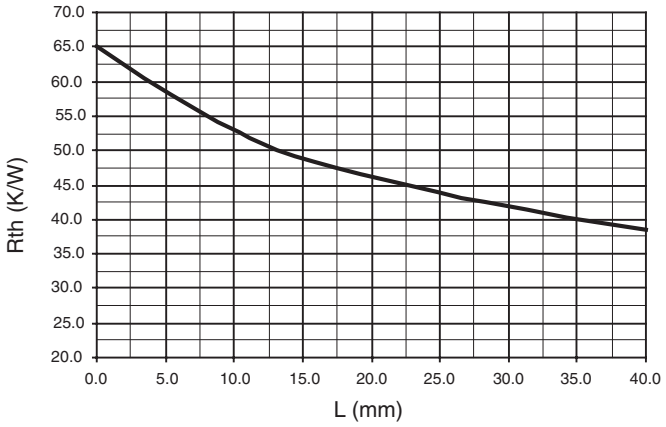


Figure 5-2. Thermal Resistance versus Adapted Cooling Area Size on Board



6. Overload Considerations

6.1 Driver Output Shorted to V_S

During normal operation, the T6817 is protected against short circuits by an overcurrent limitation. However, some attention has to be turned to certain states of abnormal operating conditions that might occur in practice. In particular, we have to consider the case of a high-side output shorted to V_{out} while the IC is not connected to supply voltage V_S. Under these conditions, an unwanted backward current flows from the shorted output, via the voltage supply pin, to the capacitor C1 (see Figure 6-1).

The backward current I_b flows from HSx to the V_S pin until the capacitor C1 is charged to V_{out} (minus drop across the diode). Its value is strongly influenced by the capacitance of C1, but also the quality of C1 (ESR) and any parasitic resistance will have an impact. The recommended range for C1 is 22 µF to 100 µF. As stated in the datasheet, the maximum reverse current is 17A for a duration of 150 µs. The graph illustrated in Figure 6-2 shows the typical voltage and reverse current gradients for a capacitor value of 100 µF.

Figure 6-1. Current Flow in Case of HSx Shorted to V_{out}

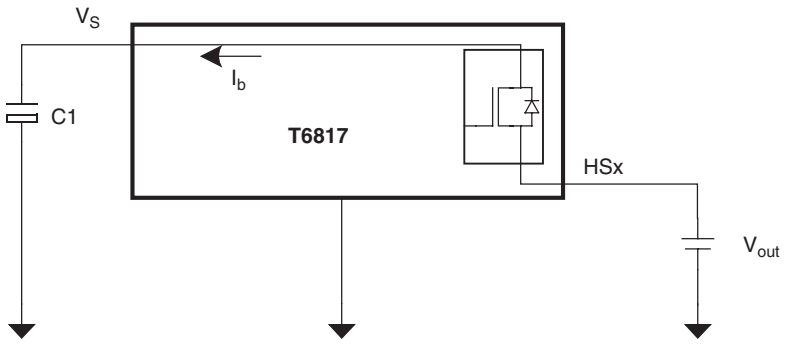
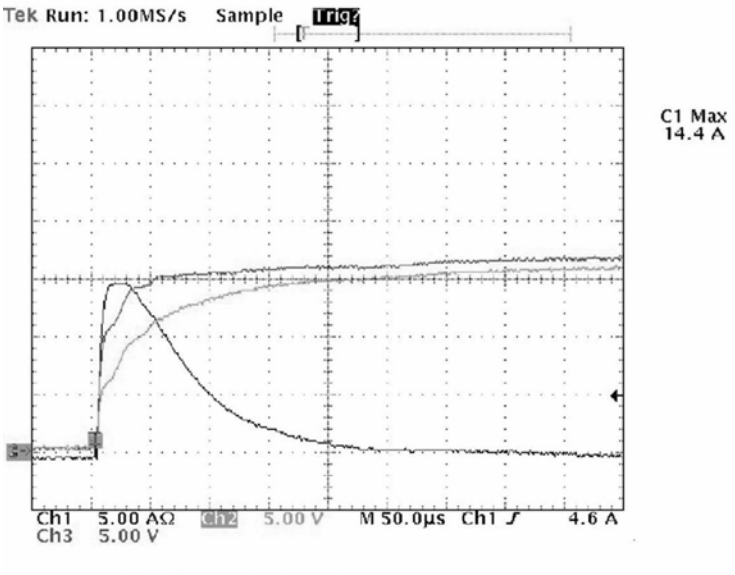


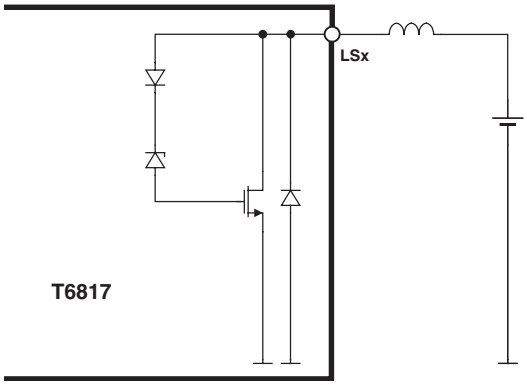
Figure 6-2. Current and Voltage Gradients
for V_{out} = 16V, C1 = 100 µF; Channel 1 = I_b, Channel 2 = V_{Vs}, Channel 3 = V_{out}



6.2 Inductive Shutdown

Any driver IC faces a challenge if an inductive load is connected to its outputs, as the energy stored in the inductance leads to a voltage peak when the load is switched off. In the case of low-side driver outputs, the voltage peak has positive polarity, while for the high-side outputs such peak is negative. In order to prevent any damage of the IC's output stages, some protective means have to be implemented. Figure 6-3 illustrates the principal protection circuit of the low-side outputs, while the arrangement for the high-side outputs can be found in Figure 6-5 on page 17.

Figure 6-3. Principal Clamping Structure at Low-side Output



The clamping structures at the output stages limit the voltage peak and provide a path for the current after switching off. The maximum inductive shutdown energy for T6817 is specified as 15 mJ. This value applies for both low-side and high-side outputs. The energy W_L stored in the inductor L during the switched-on state can be calculated with the following formula:

$$w_L = \frac{L \times I_L^2}{2}$$

Figure 6-4. Inductive Pulse at Low-side Output;
Channel 1: Gradient of I_{out}, Channel 2: Gradient of V_{out}, Pulse Energy:
W_L = 10 mJ. Please note that the maximum pulse energy for T6817 is 15 mJ

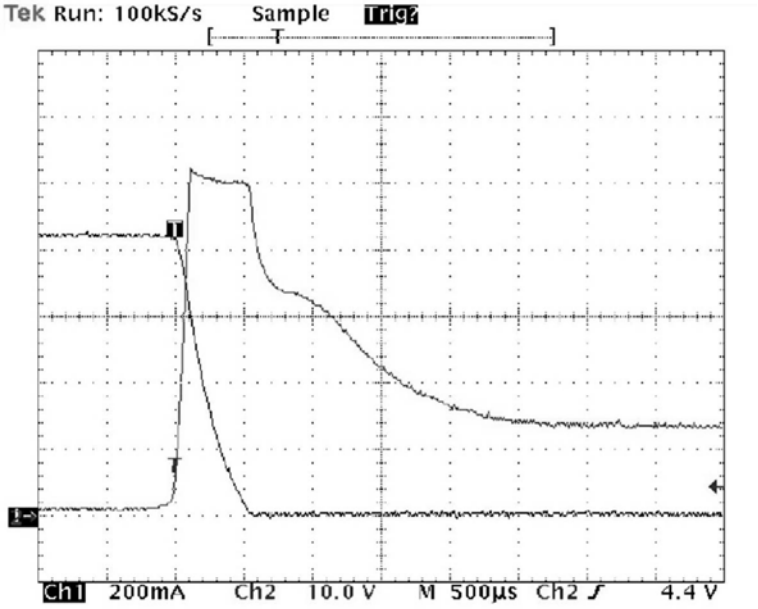
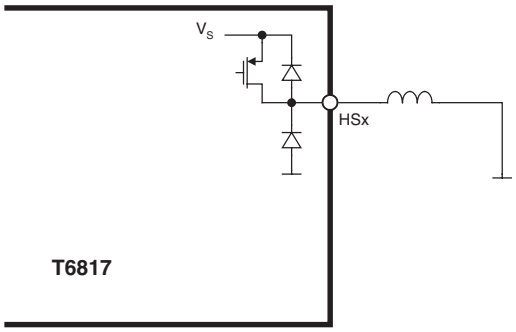


Figure 6-5. Principal Clamping Structure at High-side Output



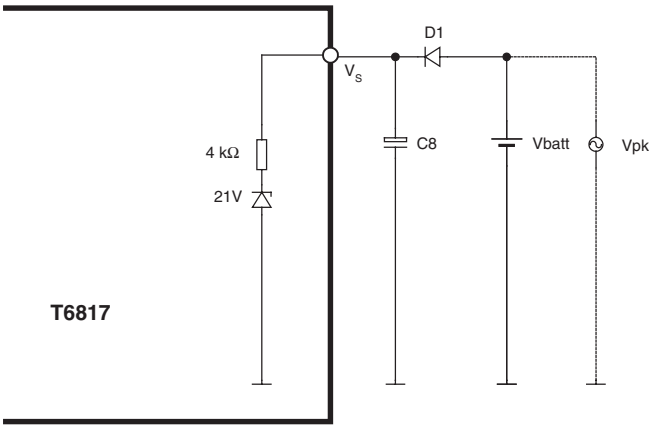
6.3 Discharger Circuit

Many typical applications use an inverse-polarity protection diode (such as D1 in Figure 2-2 on page 3) in the power supply feed to prevent any damage if V_S is applied with the wrong polarity. Despite being a recommended way of doing this, such a concept also involves a certain danger.

During inhibit mode, the IC consumes only an extremely low current I_{VS}, such as 40 µA at maximum. Any peaks on the supply voltage (V_{pk} in Figure 6-6 on page 18) will gradually charge the blocking capacitor (C1 in Figure 6-6 on page 18). D1 prevents the capacitor from discharging via the power supply; due to the extremely small quiescent current, discharging via the IC can be neglected, too.

This only means that during long periods of inhibit mode, the IC's supply voltage could increase continuously – until finally the maximum supply voltage limit of 40V would be exceeded and the IC could be damaged. The T6817 therefore features a discharger circuit that avoids such unwanted effects. If V_S exceeds a threshold value of approximately 21V, the blocking capacitor is discharged via an integrated resistor until V_S again falls below the threshold.

Figure 6-6. Functional Principle of the Discharger Circuit



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
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Fax: (852) 2722-1369

Japan

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1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
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Tel: 1(408) 441-0311
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Fax: (49) 71-31-67-2340

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