



P-Channel 2.5-V (G-S) MOSFET

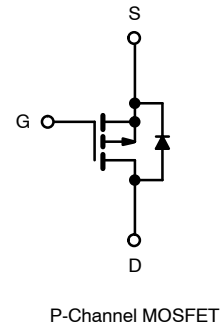
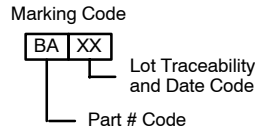
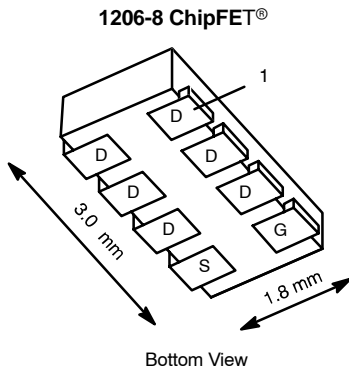


Pb-free
Available

PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)
-20	0.055 @ V _{GS} = -4.5 V	-5.3	11
	0.06 @ V _{GS} = -3.6 V	-5.1	
	0.083 @ V _{GS} = -2.5 V	-4.3	

FEATURES

- TrenchFET® Power MOSFET
- 2.5-V Rated



Ordering Information: Si5441DC
Si5441DC-T1—E3 (Lead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	-20		V	
Gate-Source Voltage	V _{GS}	± 12			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	-5.3	-3.9	A
		T _A = 85 °C	-3.8	-2.8	
Pulsed Drain Current	I _{DM}	-20		A	
Continuous Source Current ^a	I _S	-2.1	-1.1		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	2.5	1.3	W
		T _A = 85 °C	1.3	0.7	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 5 sec	40	50	°C/W
		Steady State	80	95	
Maximum Junction-to-Foot (Drain)	R _{thJF}	15	20		

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

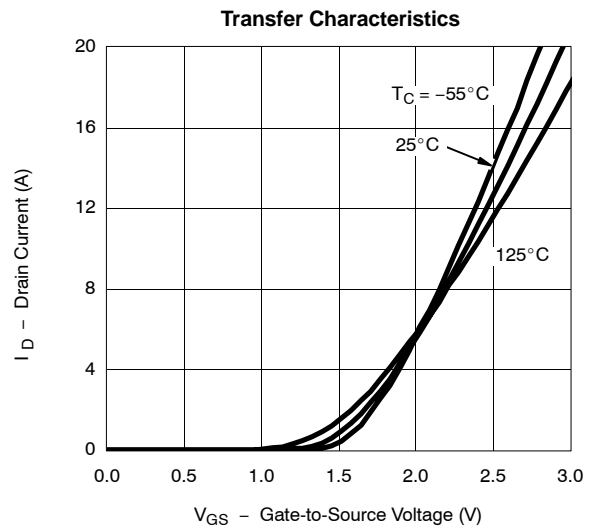
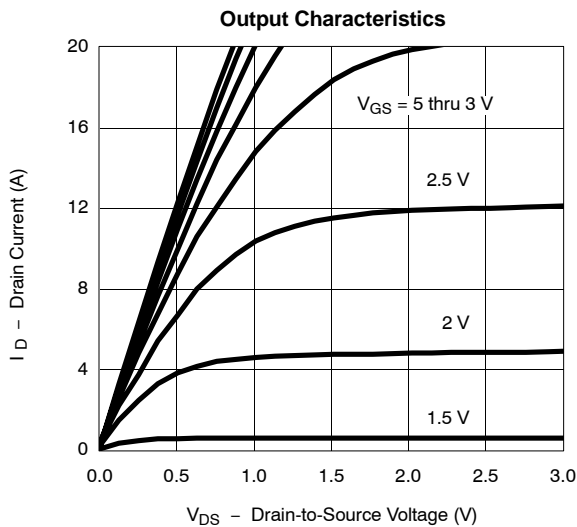
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.6		-1.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 85 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -3.9 A		0.046	0.055	Ω
		V _{GS} = -3.6 V, I _D = -3.7 A		0.050	0.06	
		V _{GS} = -2.5 V, I _D = -3.1 A		0.070	0.083	
Forward Transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -3.9 A		12		S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.1 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -3.9 A		11	22	nC
Gate-Source Charge	Q _{gs}			3.0		
Gate-Drain Charge	Q _{gd}			2.5		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		20	30	ns
Rise Time	t _r			35	55	
Turn-Off Delay Time	t _{d(off)}			65	100	
Fall Time	t _f			45	70	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -1.1 A, di/dt = 100 A/μs		30	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

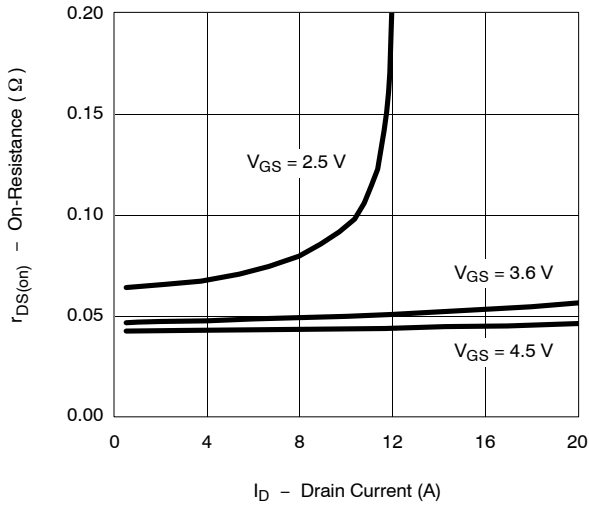
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

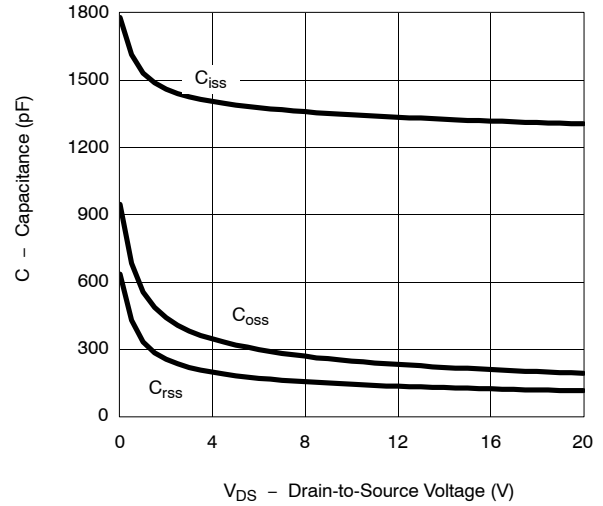


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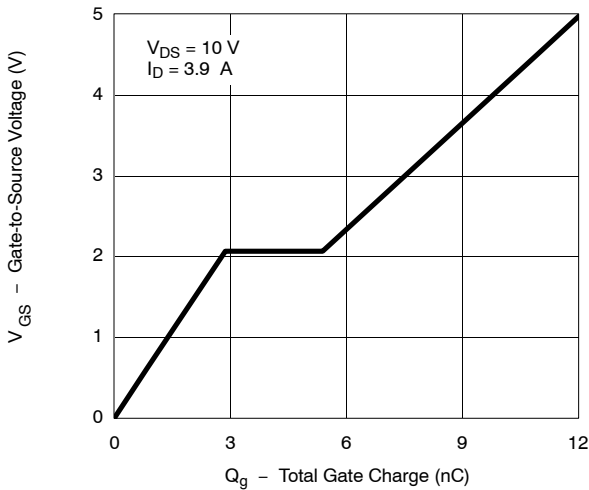
On-Resistance vs. Drain Current



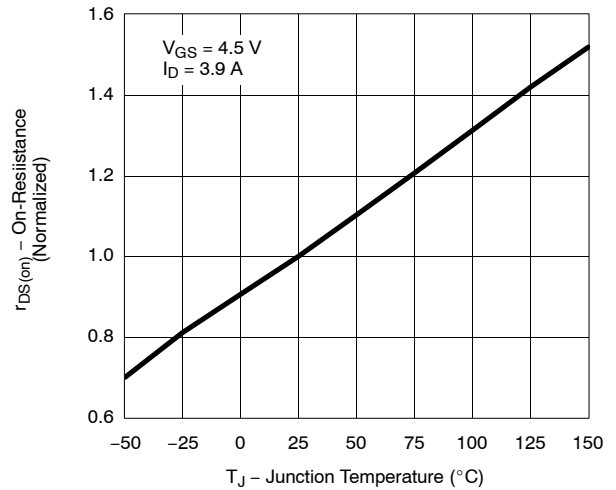
Capacitance



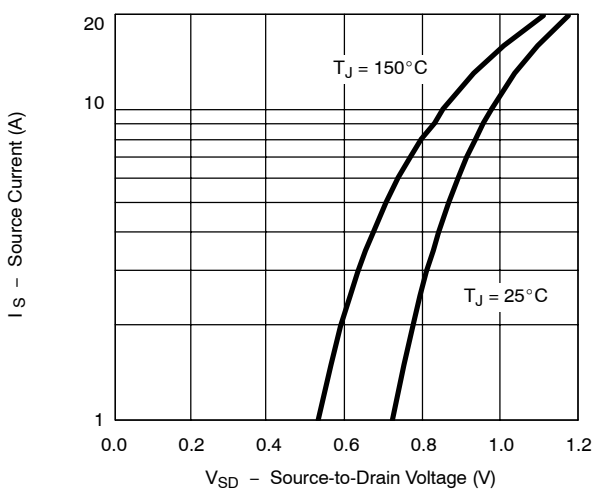
Gate Charge



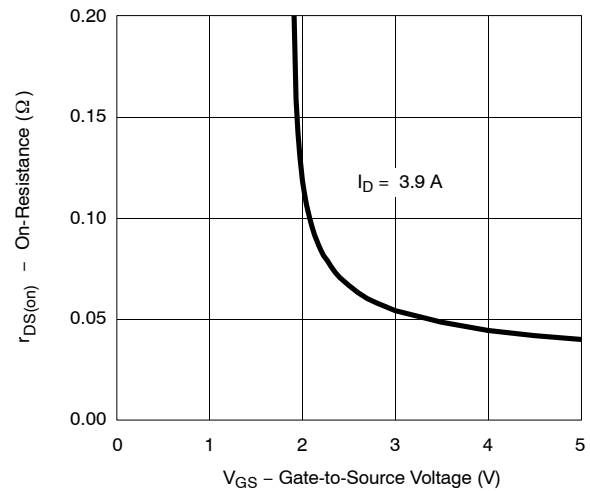
On-Resistance vs. Junction Temperature



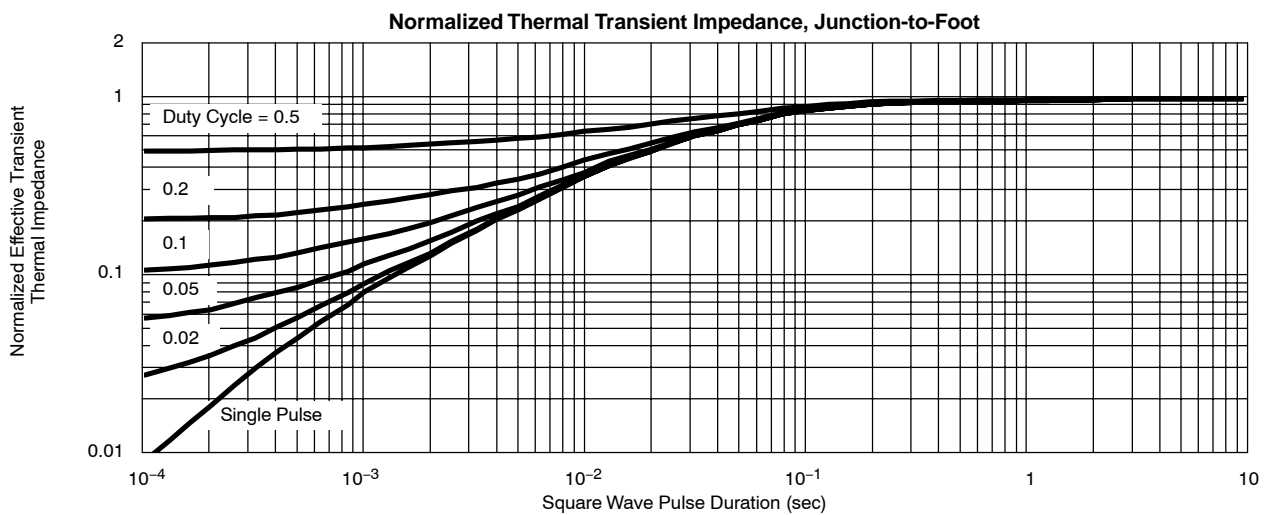
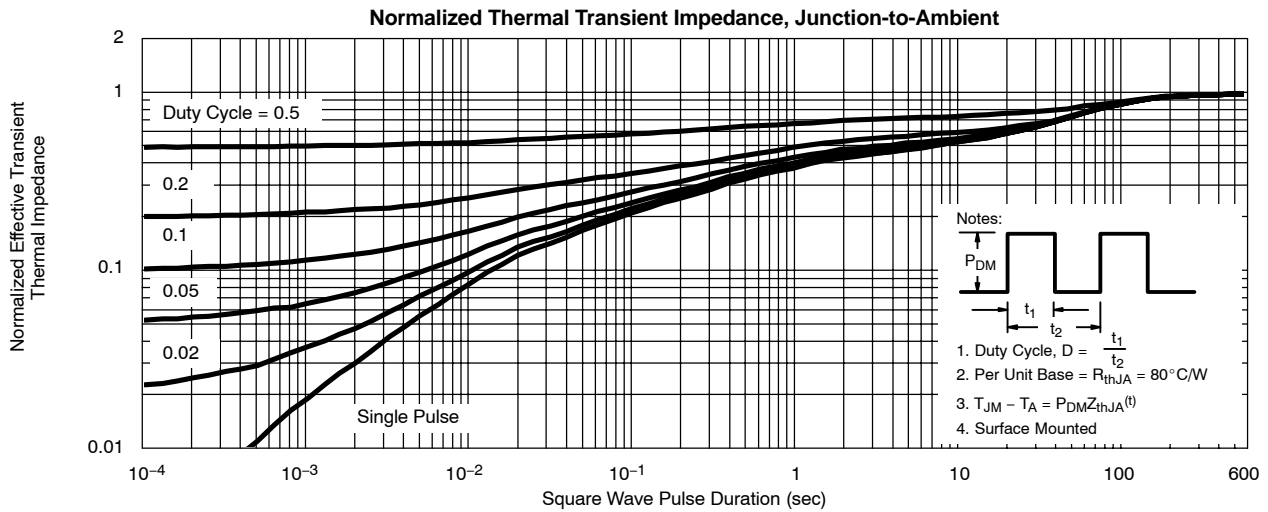
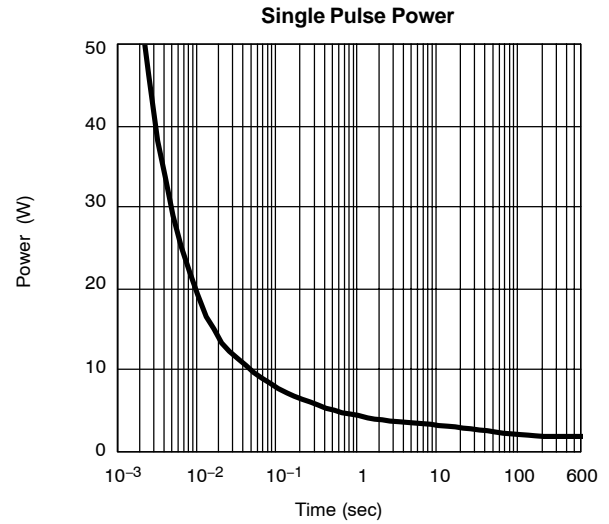
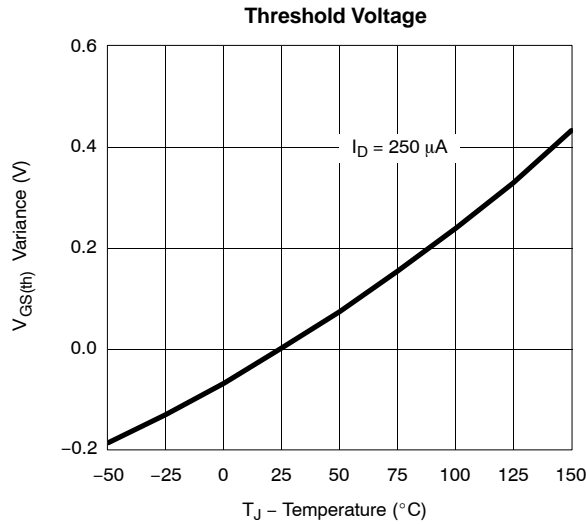
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?71055>.