AAT1154
1MHz 3A Buck DC/DC Converter

SwitchReg™

General Description

The AAT1154 SwitchReg™ is a member of AnalogicTech™'s Total Power Management™ IC product family. The Step-down switching converter is ideal for applications where high efficiency, small size, and low ripple are critical. Able to deliver 3A with an internal power MOSFET, the current-mode controlled IC provides high efficiency. Fully internally compensated, the AAT1154 simplifies system design and lowers external part count.

The AAT1154 is available in an SOP-8 package, rated over -40 to 85°C.

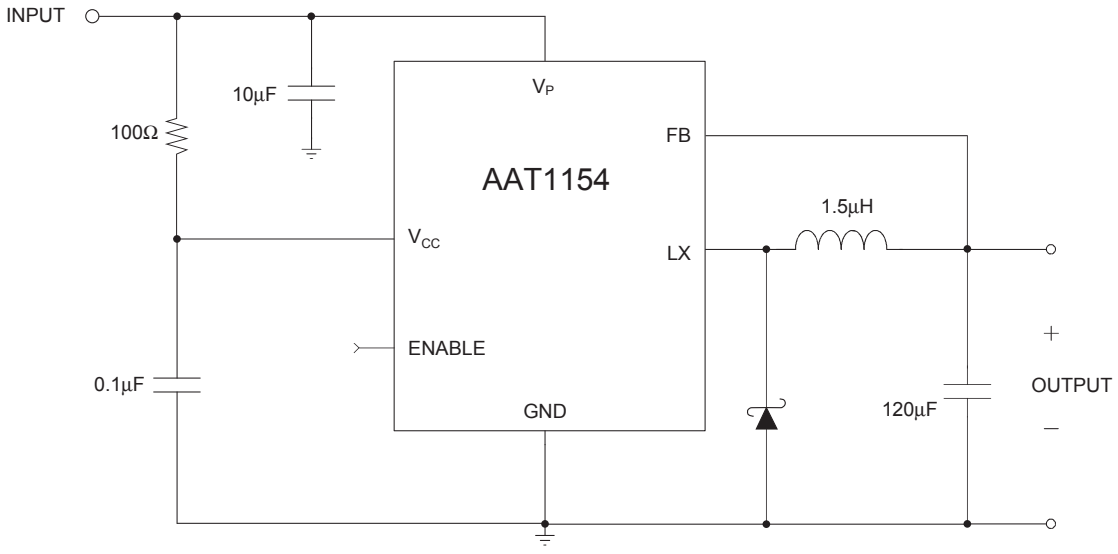
Features

- V_{IN} Range: 2.7-5.5Volts
- Fixed or adjustable V_{OUT}: 1.0V - 4.2V
- 3A output current
- Up to 95% efficiency
- Integrated low on resistance power switch
- Internally compensated current mode control
- 1MHz switching frequency
- Fixed or adjustable V_{OUT}: 1.0 to 4.2V
- Constant PWM mode
- Low output ripple with light load
- Internal softstart
- Current limit protection
- Over-Temperature protection
- SOP-8 package
- -40 to 85°C Temperature Range

Applications

- Computer Peripherals
- Set Top Boxes
- Network Cards
- Cable/DSL Modems
- High efficiency conversion from 5V or 3.3V supply

Typical Application

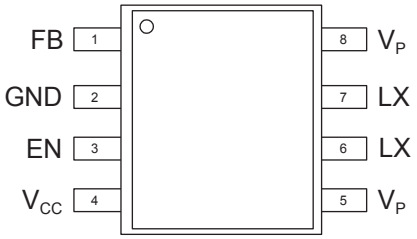


Pin Descriptions

Pin #	Symbol	Function
1	FB	Feedback input pin. This pin must be connected to the converter's output. It is used to set the output of the converter to regulate to the desired value.
2	GND	Ground connection.
3	EN	Enable input pin. When connected high, AAT1154 is in normal operation. When connected low, it is powered down. This pin should not be left floating.
4	VCC	Power supply. It supplies power for the internal circuitry.
5, 8	VP	Input Supply Voltage for converter power stage.
6, 7	LX	Inductor connection pins. These pins should be connected to the output inductor. Internally, pins 6 & 7 are connected to the drain of the P-channel switch.

Pin Configuration

SO-8



Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Description	Value	Units
V_{CC}, V_P	V_{CC}, V_P to GND	6	V
V_{LX}	LX to GND	-0.3 to V_P+0.3	V
V_{FB}	FB to GND	-0.3 to V_{CC}+0.3	V
V_{EN}	EN to GND	-0.3 to V_{CC}+0.3	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
V_{ESD}	ESD Rating [1] - HBM	3000	V

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Note 1: Human body model is a 100pF capacitor discharged through a 1.5K resistor into each pin.

Thermal Characteristics

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance [2]	110	°C/W
P_D	Maximum Power Dissipation (T_A = 25°C) [2, 3]	909	mW

Note 2: Mounted on a demo board (FR4, in still air).

Note 3: Derate 9.1mW/°C above 25°C.

Recommended Operating Conditions

Symbol	Description	Rating	Units
T	Ambient Temperature Range	-40 to +85	°C

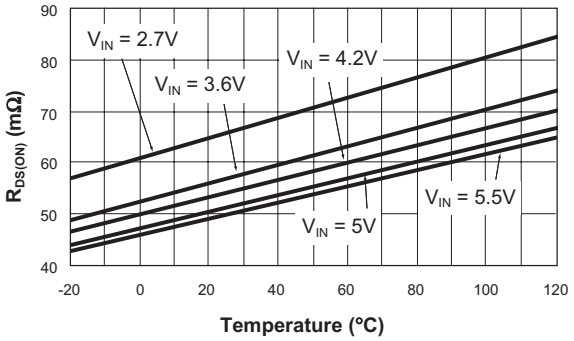
Electrical Characteristics

(V_{IN} = V_{CC} = V_P = 5V, T_A= -40 to 85°C unless otherwise noted. Typical values are at T_A = 25°C)

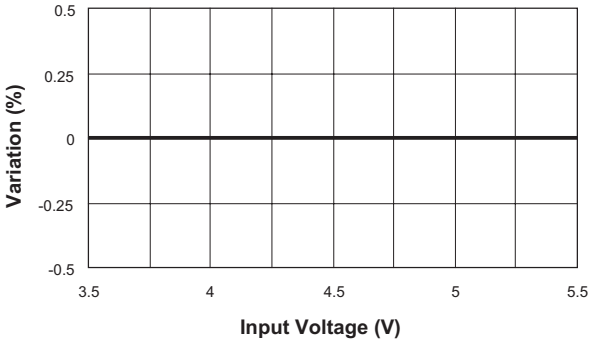
Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2.7		5.5	V
V_{OUT}	Output Voltage Tolerance	V_{IN} = V_{OUT} + 0.2 to 5.5V, I_{OUT} = 0 to 3A	-5.0		5.0	%
V_{UVLO}	Under Voltage Lockout	V_{IN} Rising			2.5	V
		V_{IN} Falling	1.2			V
$V_{UVLO(HYS)}$	Under Voltage Lockout Hysteresis			250		mV
I_Q	Quiescent Supply Current	No Load, V_{FB}= 0 V		630	1000	µA
I_{SHDN}	Shutdown Current	V_{EN} = 0 V, V_{IN}= 5.5V			1.0	µA
I_{LIM}	Current Limit	T_A = 25°C	4.4			A
$R_{DS(ON)L}$	High Side Switch On Resistance	T_A = 25°C		60		mΩ
η	Efficiency	I_{OUT} = 1.0 A		92		
ΔV_{OUT} (V_{OUT}*ΔV_{IN})	Load Regulation	I_{LOAD} = 0 - 3A		±2.6		%
$\Delta V_{OUT}/V_{OUT}$	Line Regulation	V_{IN}= 2.7 to 5.5V		0.75		%/V
F_{OSC}	Oscillator Frequency	T_A = 25°C		1		MHz
$V_{EN(L)}$	Enable Threshold Low				0.6	V
$V_{EN(H)}$	Enable Threshold High		1.4			V
T_{SD}	Over Temp Shutdown Threshold			140		°C
T_{HYS}	Over Temp Shutdown Hysteresis			15		°C

Typical Characteristics

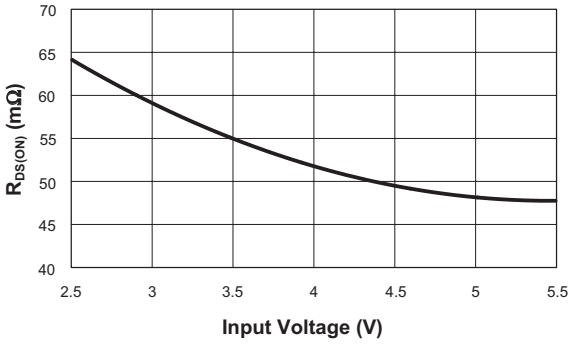
$R_{DS(ON)}$ vs. Temperature



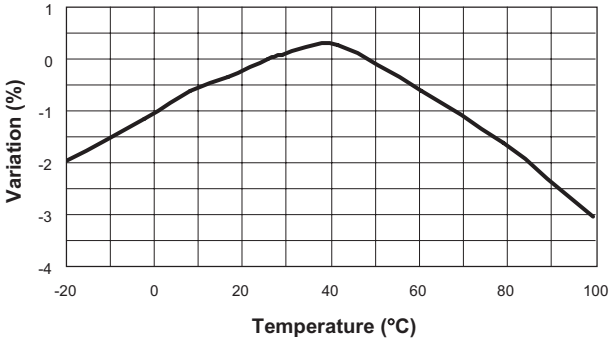
Oscillator Frequency Variation vs. Supply Voltage



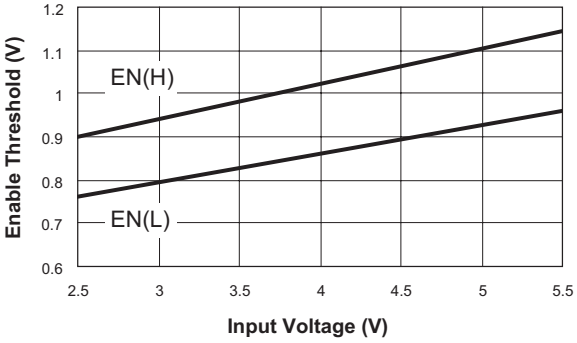
$R_{DS(ON)}$ vs. V_{IN}, I_{DS} = 1A



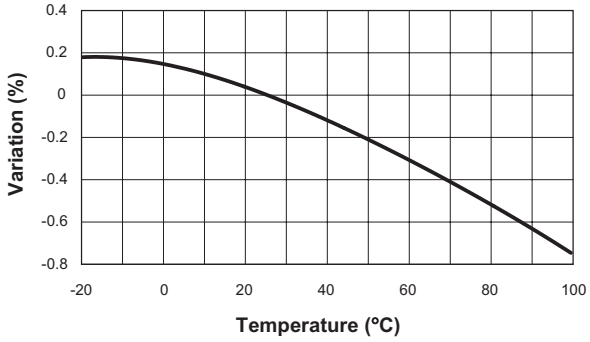
Oscillator Frequency Variation vs. Temperature V_{IN} = 5V



Enable Threshold vs. Input Voltage

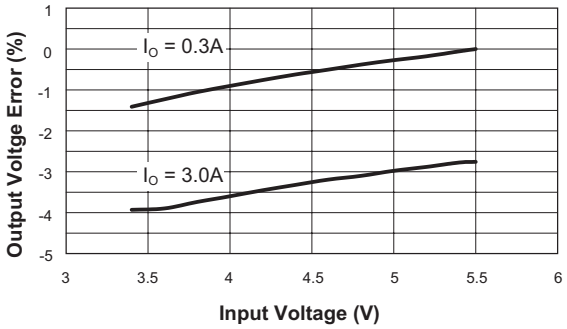


Output Voltage vs. Temperature I_{OUT}=2A

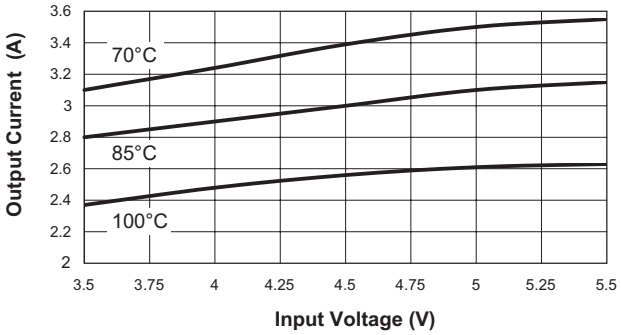


Typical Characteristics

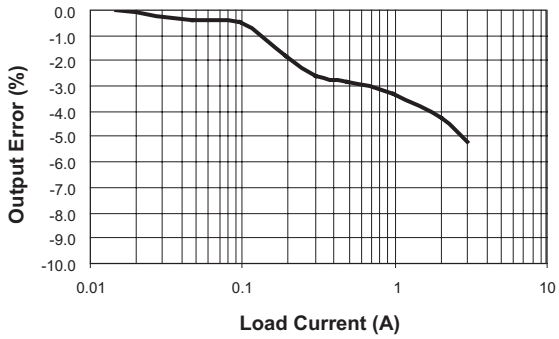
Line Regulation
V_{OUT}=3.3V



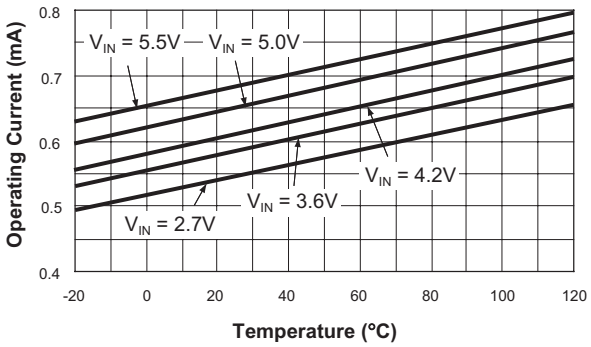
Over Temp Current vs. Input Voltage
V_{OUT} = 3.3V



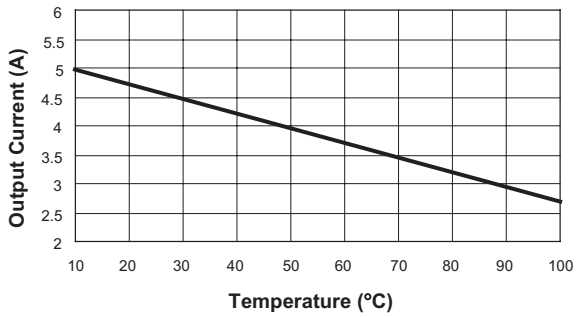
Load Regulation
V_{IN} = 5.0V, V_{IN} = 3.3V



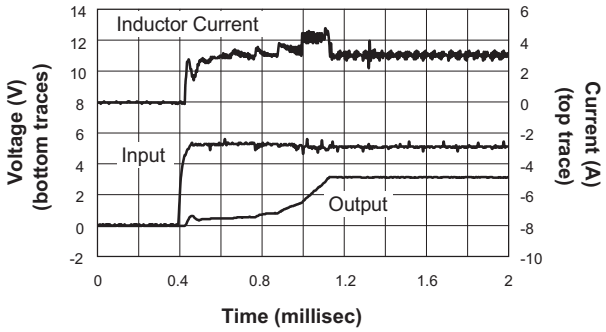
Non-Switching Operating Current vs. Temperature
FB = 0V



Over Temp Shutdown Current vs. Temperature
V_{OUT} = 3.3V, V_{IN} = 5.0V, L = 1.5µH

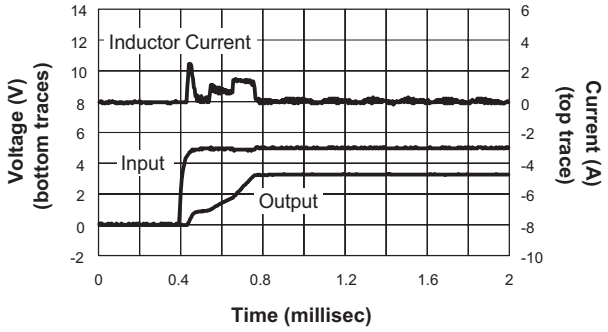


Inrush and Output Overshoot Characteristic
3A Load

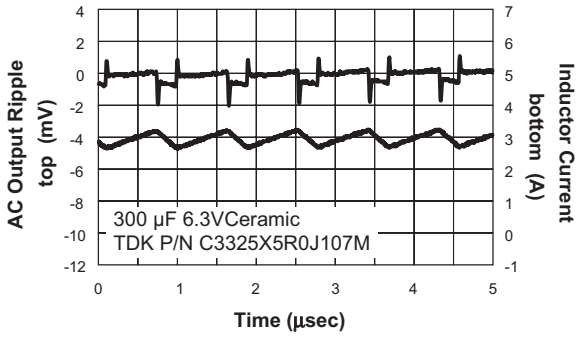


Typical Characteristics

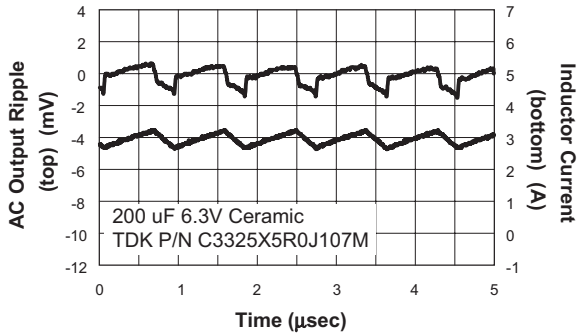
Inrush and Output Overshoot Characteristic
No Load



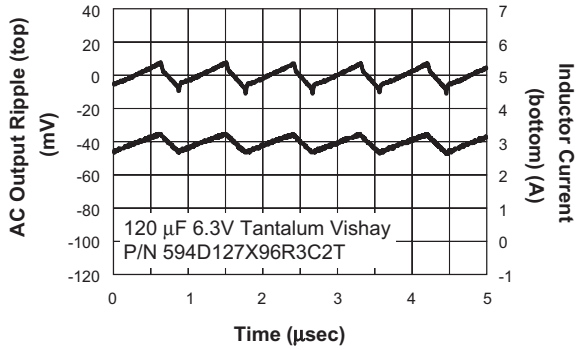
Output Ripple
I_{OUT} = 3.0A, V_{OUT} = 3.3V, V_{IN} = 5.0V



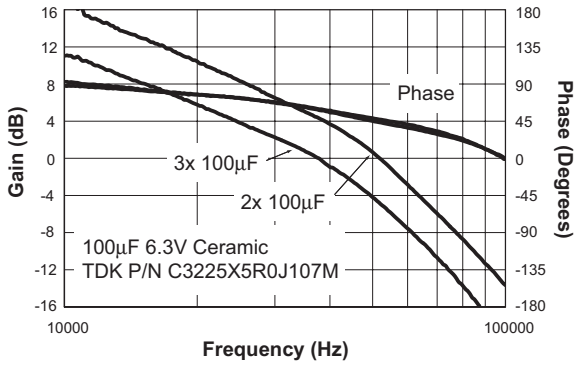
Output Ripple
I_{OUT} = 3.0A, V_{OUT} = 3.3V, V_{IN} = 5.0V



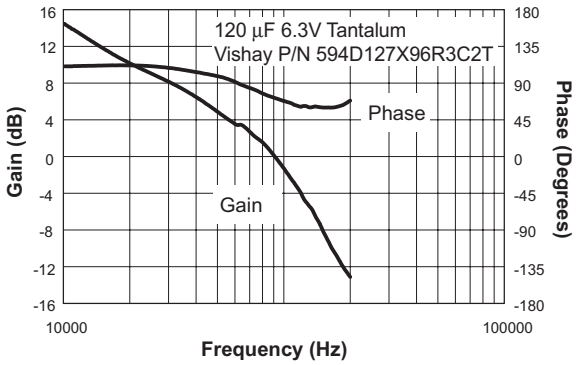
Tantalum Output Ripple
I_{OUT} = 3.0A, V_{OUT} = 3.3V, V_{IN} = 5.0V



Loop Crossover Gain and Phase

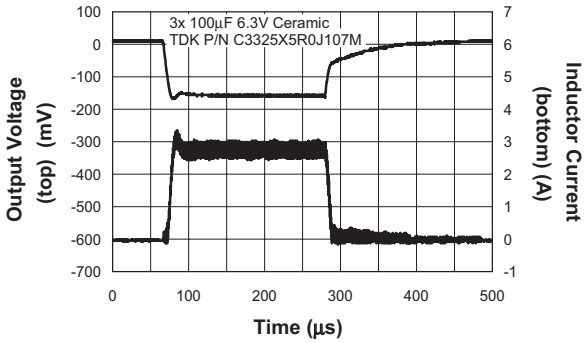


Loop Crossover Gain and Phase

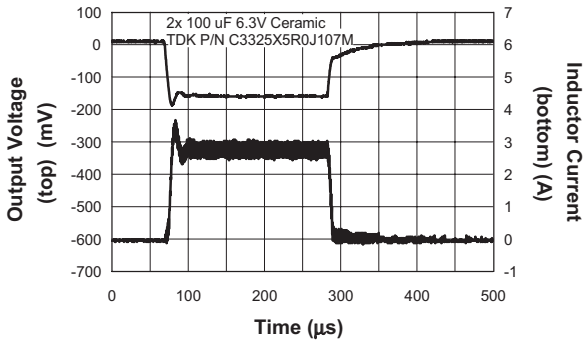


Typical Characteristics

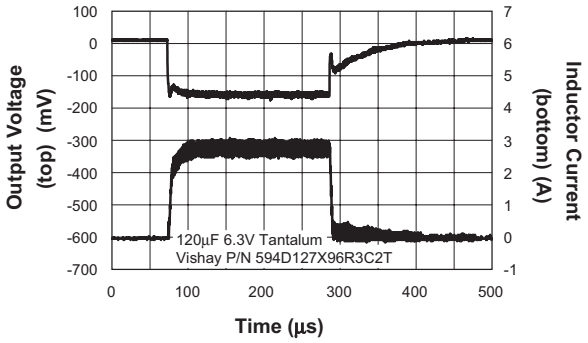
Transient Response
I_{OUT} = 0 to 3.0A, V_{OUT} = 3.3V, V_{IN} = 5.0V



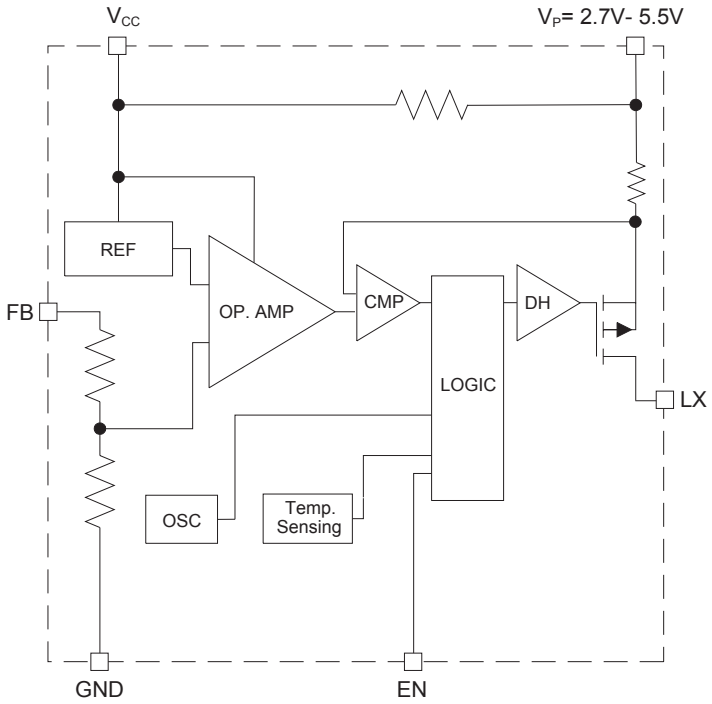
Transient Response
I_{OUT} = 0 to 3.0A, V_{OUT} = 3.3V, V_{IN} = 5.0V



Tantalum Transient Response
I_{OUT} = 0 to 3.0A, V_{OUT} = 3.3V, V_{IN} = 5.0V



Functional Block Diagram



Applications Information

Main Control Loop

The AAT1154 is a peak current mode buck converter. The inner wide bandwidth loop controls the inductor peak current. The inductor current is sensed as it flows through the internal P-Channel MOSFET. A fixed slope compensation signal is then added to the sensed current to maintain stability for duty cycles greater than 50%. The inner loop appears as a voltage programmed current source in parallel with the output capacitor.

The voltage error amplifier output programs the current loop for the necessary inductor current to force a constant output voltage for all load and line conditions. The feedback resistive divider is internal, dividing the output voltage to the error amplifier reference voltage of 1.0V. The error amplifier has a limited DC gain. This eliminates the need for external compensation components while still providing sufficient DC loop gain for good load regulation. The crossover frequency and phase margin are set by the output capacitor value.

Duty cycle extends to 100% as the input voltage approaches the output voltage. Thermal shutdown protection disables the device in the event of a short circuit or overload condition.

Soft Start/Enable

Soft-start controls the current limit when the input voltage or enable is applied. It limits the current surge seen at the input and eliminates output voltage overshoot.

The enable input, when pulled low, forces the device into a low power non-switching state. The total input current during shutdown is less than 1µA.

Power and Signal Source

Separate small signal ground and power supply pins isolate the internal control circuitry from switching noise. In addition, the low pass filter R1 and C3 in figure 3 filters noise associated with the power switching.

Current Limit and Over Temp Protection

The AAT1154 over temp and current limit circuitry protects the AAT1154 as well as the external Schottky diode during overload, short circuit and excessive ambient temperature conditions. The junction over temp threshold is 140°C nominal and has 15°C of hysteresis. Typical graphs of the over temp load current vs. input voltage and ambient temperature are shown in the Typical Characteristics section.

Inductor

The output inductor is selected to limit the ripple current to 20-40% of the full load current at the maximum input voltage. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the inductor saturation characteristics. The inductor should not show any appreciable saturation under all normal load conditions. During overload and short circuit conditions the inductor can exceed its peak current rating without affecting the converter performance. Some inductors may have sufficient peak and average current ratings yet result in excessive losses due to a high DC resistance (DCR). The losses associated with the DCR and its affect on the total converter efficiency must be considered.

For a 3 Amp load and the ripple current set to 30% at the maximum input voltage, the maximum peak to peak ripple current is 0.9Amp. Assuming a 5V ± 5% input voltage and 30% ripple the output inductance required is

$$L = \frac{V_{OUT}}{I_{OUT} \cdot k \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

$$= \left(\frac{3.3V}{3.0A \cdot 0.3 \cdot 1MHz}\right) \cdot 1 - \left(\frac{3.3V}{5.25V}\right)$$

$$= 1.36\mu H$$

The factor "k" is the fraction of the full load (30%) selected for the ripple current at the maximum input voltage.

The corresponding inductor RMS current is:

$$I_{RMS} = \sqrt{\left(I_O^2 + \frac{\Delta I^2}{12}\right)} \approx I_O = 3A$$

ΔI is the peak to peak ripple current which is fixed by the inductor selection above. For a peak to peak current of 30% of the full load current the peak current at full load will be 115% of the full load. The 1.5µH inductor selected from the Sumida CDRH6D38 series has a 11mΩ DCR and a 4.0 Amp DC current rating with a height of 4 mm. At full load the inductor DC loss is 99 mW for a 1 % loss in efficiency.

Schottky Freewheeling Diode

The Schottky average current is the load current times one minus the duty cycle. For V_{IN} at 5 Volts and Vout at 3.3 Volts the average diode current is

$$I_{AVG} = I_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = 3A \cdot \left(1 - \frac{3.3V}{5.0V}\right) = 1A$$

With a 125°C maximum junction temperature and a 120°C/W thermal resistance the maximum average current is

$$I_{AVG} = \frac{T_{J(MAX)} - T_{AMB}}{\theta_{J-A} \cdot V_{FWD}} = \frac{125°C - 70°C}{120°C/W \cdot 0.4V} = 1.14A$$

For overload, short circuit, and excessive ambient conditions the AAT1154 enters the over-temperature shutdown mode protecting the AAT1154 as well as the output Schottky. In this mode the output current is limited internally until the junction temperature reaches the temperature limit (see over temp characteristics graphs). The diode reverse voltage must be rated to withstand the input voltage.

Diodes Inc.	B340LA	0.45V@3A
ROHM	RB050L-40	0.45@3A
Micro Semi	5820SM	0.46V@3A

3 Amp Surface Mount Schottky Diodes

Input Capacitor Selection

The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the AAT1154. A low ESR/ESL ceramic capacitor is ideal for this function. To minimize the stray inductance the capacitor should be placed as close as possible to the IC. This also keeps the high frequency content of the input current localized, minimizing the radiated and conducted EMI while facilitating optimum performance of the AAT1154. The proper placement of the input capacitor C1 is shown in the layout in figure 1. Ceramic X5R or X7R capacitors are ideal. The size required will vary depending on the load, output voltage, and input voltage source impedance characteristics. Typical values range from 1µF to 10 µF. The input capacitor RMS current varies with the input voltage and the output voltage. It is highest when the input voltage is double the output voltage where it is one half of the load current.

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

A high ESR tantalum with a value about 10 times the input ceramic capacitor may also be required when using a 10µF or smaller ceramic input bypass capacitor. This dampens out any input oscillations that may occur due to the source inductance resonating with the converter input impedance

Output Capacitor

With no external compensation components, the output capacitor has a strong effect on the loop stability. Larger output capacitance will reduce the crossover frequency with greater phase margin. A 200µF ceramic capacitor provides sufficient bulk capacitance to stabilize the output during large load transitions and has ESR and ESL characteristics necessary for very low output ripple. The RMS ripple current is given by

$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT} + V_{FWD}) \cdot (V_{IN} - V_{OUT})}{L \cdot F \cdot V_{IN}}$$

For a ceramic output capacitor the dissipation due to the RMS current and output ripple associated with are negligible.

Tantalum capacitors, with sufficiently low ESR to meet output ripple requirements, generally have an RMS current rating much greater than that actually seen in this application. The maximum tantalum output capacitor ESR is

$$ESR \leq \frac{V_{RIPPLE}}{\Delta I}$$

Where ΔI is the peak to peak inductor ripple current.

Due to the ESR zero associated with the tantalum capacitor, smaller values than those required with ceramic capacitors provide more phase margin a with greater loop crossover frequency.

Layout

Figures 1 and 2 display the suggested PCB layout for the AAT1154. The following guidelines should be used to help insure a proper layout.

1. The connection from the input capacitor to the Schottky anode should be as short as possible.
2. The input capacitor should connect as closely as possible to V_{POWER} (pins 5 and 8) and GND (pin 2).
3. C1, L1, and CR1 should be connected as closely as possible. The connection from the cathode of the Schottky to the LX node should be as short as possible.
4. The feedback trace (pin 1) should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high current load trace can degrade DC load regulation.
5. The resistance of the trace from the load return to the gnd (pin 2) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal reference ground and the load rtn.
6. R1 and C3 are required in order to provide a cleaner power source for the AAT1154 control circuitry.

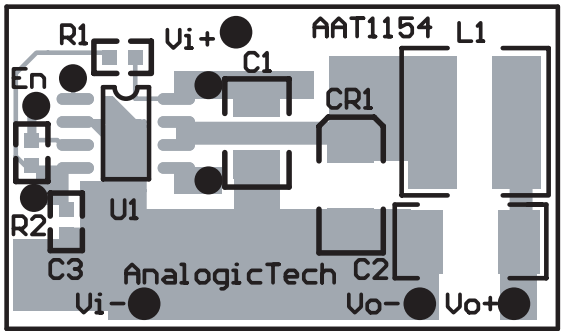


Figure 1. AAT1154 Fixed Output Top Side Layout

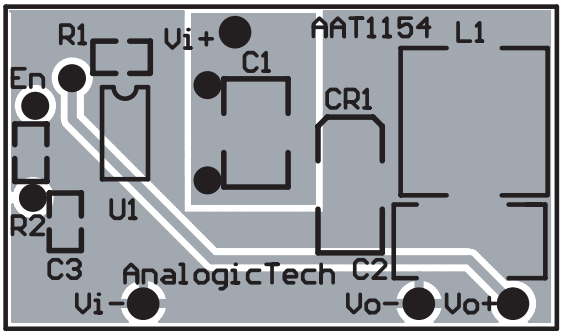


Figure 2. AAT1154 Fixed Output Bottom Side Layout

Thermal

The losses associated with the AAT1154 output switching MOSFET are due to switching losses and conduction losses. The conduction losses are associated with the $R_{DS(ON)}$ characteristics of the output switching device. At the full load condition, assuming continuous conduction mode (CCM), an accurate calculation of the $R_{DS(ON)}$ losses can be derived from the following equations.

$$P_{ON} = I_{RMS}^2 \cdot R_{DS(ON)}$$

$R_{DS(ON)}$ losses

$$I_{RMS} = \sqrt{\left(I_O^2 + \frac{\Delta I^2}{12}\right) \cdot D}$$

Internal switch RMS current

D is the duty cycle and V_F is the forward drop of the Schottky diode.

$$D = \frac{V_O + V_F}{V_{IN} + V_F}$$

I_Q is the peak to peak inductor ripple current.

A simplified form of calculating the $R_{DS(ON)}$ and switching losses is given by

$$P = \frac{I_O^2 \cdot R_{DS(ON)}\, V_o}{V_{IN}} + t_{SW} \cdot F \cdot I_O + I_Q \cdot V_{IN}$$

where I_Q is the AAT1154 quiescent current.

Once the total losses have been determined the junction temperature can be derived. The thermal resistance (Θ_{JA}) for the SO-8 package mounted on an FR4 printed circuit board in still air is 110°C/W.

$$T_J = P \cdot \Theta_{JA} + T_{AMB}$$

T_{AMB} is the maximum ambient temperature and T_J is the resultant maximum junction temperature.

Design Example

I_{OUT} 3A

I_{RIPPLE} 30% of full load at max Vin

V_{OUT} 3.3V

V_{IN} 5V ± 5%

F_S 1MHz

T_{MAX} = 70°C

Inductor Selection

$$L = \frac{V_{OUT}}{I_O \cdot k \cdot F} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= \frac{3.3V}{3A \cdot 0.3 \cdot 1MHz} \cdot \left(1 - \frac{3.3V}{5V}\right) = 1.25\mu H$$

Use standard value of 1.5 µH

Sumida inductor Series CDRH6D38.

$$\Delta I = \frac{V_O}{L \cdot F}\left(1 - \frac{V_O}{V_{IN}}\right) =$$

$$\frac{3.3V}{1.5\mu H \cdot 1MHz}\left(1 - \frac{3.3V}{5.25V}\right) = 0.82A$$

$$I_{PK} = I_{OUT} + \frac{\Delta I}{2} =$$

3A + 0.41A = 3.41A

AAT1154 Junction Temperature

$$P_{ON} = \frac{I_O^2 \cdot R_{DS(ON)} \cdot V_O}{V_{IN}} + \left(\frac{t_{SW} \cdot F \cdot I_O}{2} + I_Q\right) \cdot V_{IN} =$$

$$\frac{3^2 \cdot 65m\Omega \cdot 3.3V}{5V} + \left(\frac{20ns \cdot 1MHz \cdot 3A}{2} + 750\mu A\right) \cdot 5V =$$

0.539 Watts

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P =$$

$$70°C + 110°C/W \cdot 0.54W = 129°C$$

Diode

$$I_{DIODE} = I_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right) =$$

$$3A \cdot \left(1 - \frac{3.3V}{5V}\right) = 1.02A$$

$$V_{FW} = 0.35V$$

$$P_{DIODE} = V_{FW} \cdot I_{DIODE} =$$

$$0.35V \cdot 1.01A = .354W$$

Given a case to ambient thermal resistance of 120°C/W from the manufacturer's data sheet, $T_{J(MAX)}$ of the diode is

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P =$$

$$70°C + 120°C/W \cdot 0.354W =$$

112°C

Output Capacitor

The output capacitor value required for sufficient loop phase margin depends on the type of capacitor selected. For a low ESR ceramic capacitor a minimum value of 200µF is required. For a low ESR tantalum capacitor lower values are acceptable. While the relatively higher ESR associated with the tantalum capacitor will give more phase margin and a more damped transient response, the output voltage ripple will be higher.

The 120µF Vishay 594D tantalum capacitor has an ESR of 85 mΩ and a ripple current rating of 1.48 Arms in a C case size. Although smaller case sizes are sufficiently rated for this ripple current, their ESR level would result in excessive output ripple.

The ESR requirement for a tantalum capacitor can be estimated by

$$ESR \le \frac{V_{RIPPLE}}{\Delta I} = \frac{100mV}{0.82A} = 121m\Omega$$

$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT} + V_{FWD}) \cdot (V_{IN} - V_{OUT})}{L \cdot F \cdot V_{IN}} =$$

$$\frac{1}{2 \cdot \sqrt{3}} \cdot \frac{3.65V \cdot 1.7V}{1.5\mu H \cdot 1MHz \cdot 5V} = 240mArms$$

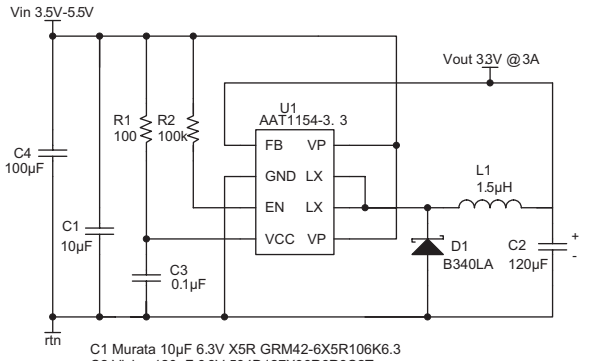
Two or three 1812 X5R 100uF 6.3V ceramic capacitors in parallel also provide sufficient phase margin. The low ESR and ESL associated with ceramic capacitors also reduces output ripple significantly over that seen with tantalum capacitors. Temperature rise due to ESR ripple current dissipation is also reduced.

Input Capacitor

The input capacitor ripple is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = 1.42Arms$$

In the examples shown C1 is a ceramic capacitor located as close to the IC as possible. C1 provides the low impedance path for the sharp edges associated with the input current. C4 may or may not be required depending upon the impedance characteristics looking back into the source. It serves to dampen out any input oscillations that may arise from a source that is highly inductive. For most applications where the source has sufficient bulk capacitance and is fed directly to the AA1154 through large PCB traces or planes it is not required. When operating the AAT1154 evaluation board on the bench C4 is required due to the inductance of the wires running from the laboratory power supply to the evaluation board.



C1 Murata 10µF 6.3V X5R GRM42-6X5R106K6.3
C2 Vishay120µF 6.3V 594D127X96R6R3C2T
C3 0.1µF 0603ZD104M AVX
C4 Vishay Sprague 100µF 16V 595D107X0016C 100µF 16V
D1 B340LA Diodes Inc.
L1 CDRH6D28-1.5µH Sumida

Options
C2 MuRata 100µF 6.3V GRM43-2 X5R 107M 100µF 6.3V (two or three in parallel
C2 TDK 100µF 6.3V C3325X5R0J107M 100µF 6.3V (two or three in parallel)

Figure 3. 3.3 Volt 3 Amp Output

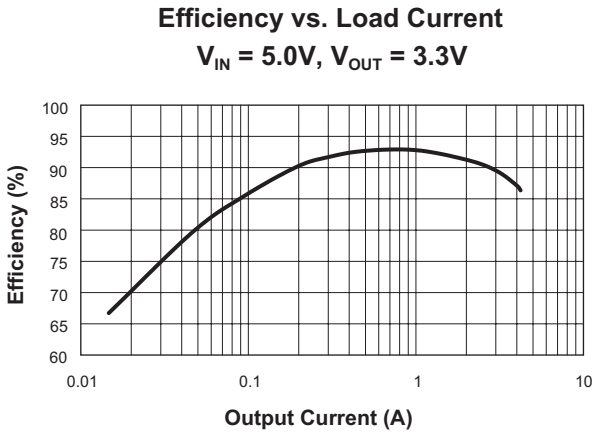
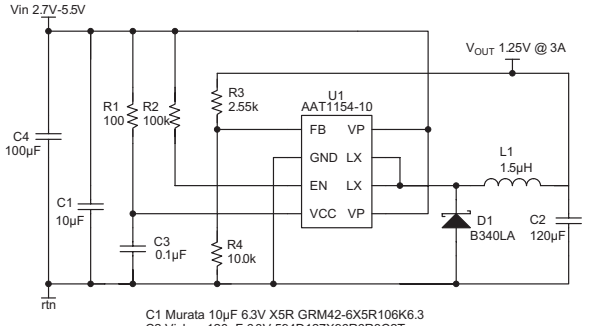


Figure 4. 5 Volt Input 3.3 Volt Output

Adjustable Output

For applications requiring an output other than the fixed outputs available, the 1V version can be programmed externally. Resistors R3 and R4 of figure 5 force the output to regulate higher than 1 Volt. For accurate results (less than 1% error for all outputs) select R4 to be 10kΩ. Once R4 has been selected R3 can be calculated. For a 1.25 Volt output with R4 set to 10k R3 is 2.5kΩ.

$$R3 = (V_O - 1) \cdot R4 = 0.25 \cdot 10k\Omega = 2.5k\Omega$$



C1 Murata 10µF 6.3V X5R GRM42-6X5R106K6.3
C2 Vishay 120µF 6.3V 594D127X96R6R3C2T
C3 0.1µF 0603ZD104M AVX
C4 Vishay Sprague 100µF 16V 595D107X0016C 100µF 16V
D1 B340LA Diodes Inc.
L1 CDRH6D28-1.5µH Sumida

Options
C2 MuRata 100uF 6.3V GRM43-2 X5R 107M 100µF 6.3V (two or three in parallel)
C2 TDK 100µF 6.3V C3325X5R0J107M 100µF 6.3V (two or three in parallel)

Figure 5. AAT1154 Evaluation Board with adjustable output

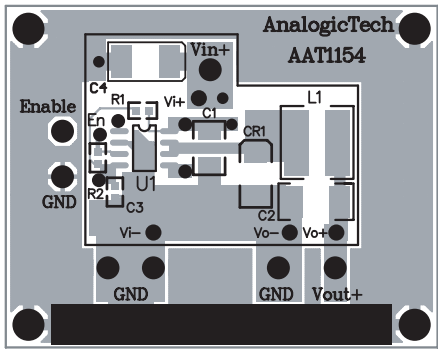


Figure 6. Evaluation Board Top Side

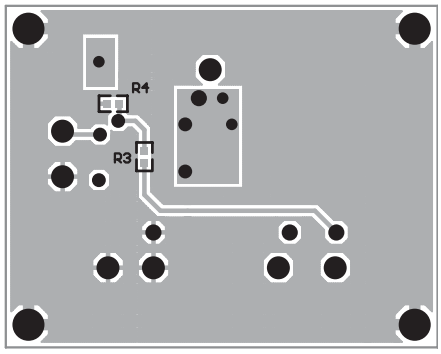


Figure 7. Evaluation Board Bottom Side

Capacitors

Part Number	Manufacturer	Capacitance (µF)	Voltage (V)	Temp Co.	Case
C4532X5ROJ107M	TDK	100	6.3	X5R	1812
GRM43-2 X5R 107M 6.3	MuRata	100	6.3	X5R	1812
GRM43-2 X5R 476K 6.3	MuRata	47	6.3	X5R	1812
GRM42-6 X5R 106K 6.3	MuRata	10	6.3	X5R	1206
594D127X_6R3C2T	Vishay	120	6.3		C case
595D107X0016C	Vishay	100	16		C case

Inductors

Part Number	Manufacturer	Inductance (µH)	I (Amps)	DCR (Ω)	Height (mm)	
CDRH6D38-4763-T055	Sumida	1.5	4.0	.014	4.0	shielded
N05D B1R5M	Taiyo Yuden	1.5	3.2	.025	2.8	Non shielded
NP06DB B1R5M	Taiyo Yuden	1.5	3.0	.022	3.2	shielded
LQH55DN1R5M03	MuRata	1.5	3.7	.022	4.7	Non shielded
LQH66SN1R5M03	MuRata	1.5	3.8	.016	4.7	shielded

Diodes

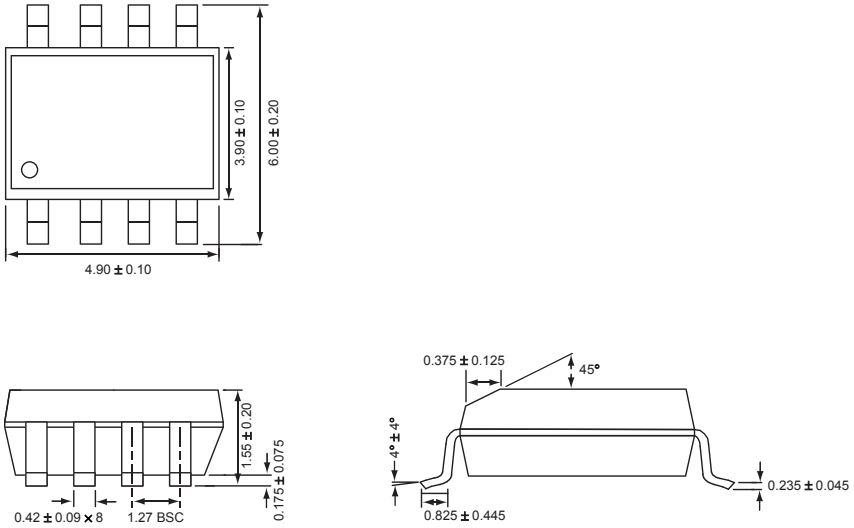
Manufacturer	Part Number	Vfwd
Diodes Inc.	B340LA	0.45V @ 3A
ROHM	RB050L-40	0.45 @ 3A
Micro Semi	5820SM	0.46V @ 3A

Ordering Information

Output Voltage	Package	Marking	Part Number (Tape and Reel)
1.0V (Adj. $V_{OUT} \geq 1.0V$)	SO-8		AAT1154IAS-1.0-T1
1.8V	SO-8		AAT1154IAS-1.8-T1
2.5V	SO-8		AAT1154IAS-2.5-T1
3.3V	SO-8		AAT1154IAS-3.3-T1

Package Information

SO-8



All dimensions in millimeters.

Advanced Analogic Technologies, Inc.
830 E. Arques Avenue, Sunnyvale, CA 94085
Phone (408) 737-4600
Fax (408) 737-4611