SwitchReg™

General Description

The AAT1151 SwitchReg™ is a member of Analogic Tech's Total Power Management IC™ product family. The step-down switching converter is ideal for applications where high efficiency is required over the full range of the output load conditions. The 2.7 to 5.5V input voltage range makes the AAT1151 ideal for single-cell Lithium Ion/Polymer battery applications. Capable of more than 700mA with internal MOSFETs, the current-mode controlled IC provides high efficiency using synchronous rectification. Fully integrated compensation simplifies system design and lowers external part count.

The device operates at a fixed 850kHz switching frequency and enters PFM mode for light load current to maintain high efficiency across all load conditions.

The AAT1151 is available in MSOP-8 and 16 pin 3x3mm QFN package rated over -40 to 85°C.

Features

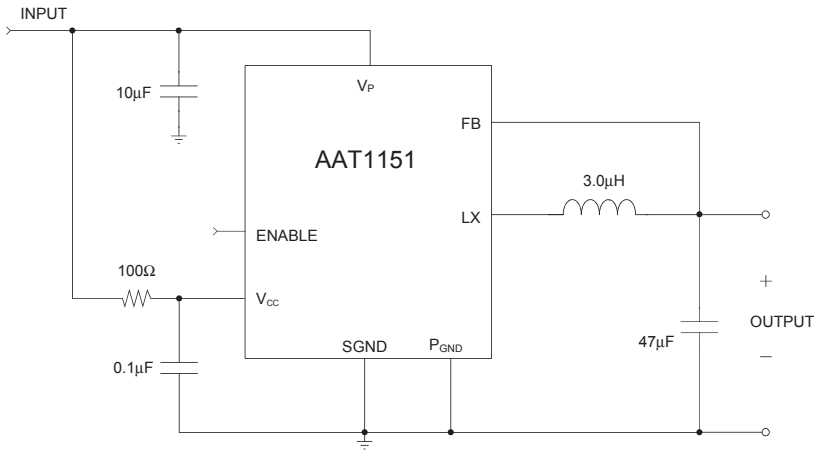
- V_{IN} Range 2.7-5.5 Volts
- Up to 95% Efficiency
- 110 mΩ $R_{DS(ON)}$ Internal Switches
- < 1µA Shutdown Current
- 850kHz Switching Frequency
- Fixed V_{OUT} or Adjustable $V_{OUT} \geq 1.0V$
- Integrated Power Switches
- Synchronous Rectification
- Current Mode Operation
- Internal Compensation
- Stable with Ceramic Capacitors
- PWM and PFM for optimum efficiency for all load conditions
- Internal Soft Start
- Over-Temperature Protection
- Current Limit Protection
- MSOP-8 and 16 pin QFN 3x3mm Package
- -40 to +85°C Temperature Range

Applications

- Wireless Notebook Adapters
- Notebook Computers
- Digital Cameras
- Cellular Phones
- MP3 Players
- PDAs
- USB Powered Equipment

Preliminary Information

Typical Application

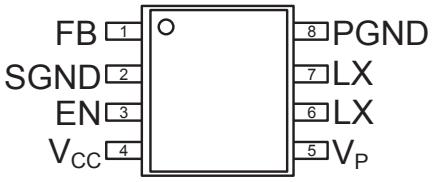


Pin Descriptions

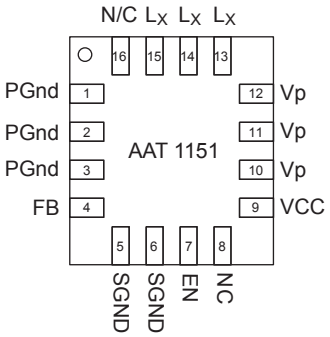
Pin # MSOP-8	Pin # QFN33-16	Symbol	Function
1	4	FB	Feedback input pin. This pin is connected to the converter output. It is used to set the output of the converter to regulate to the desired value via an internal resistive divider. For an adjustable output an external resistive divider is connected to this pin on the 1V model.
2	5, 6	SGND	Signal Ground. Connect the return of all small signal components to this pin. (see board layout rules)
3	7	EN	Enable input pin. A logic high enables the converter, a logic low forces the AAT1151 into shutdown mode reducing the supply current to less than 1µA. The pin should not be left floating.
4	9	VCC	Bias supply. Supplies power for the internal circuitry. Connect to input power via low pass filter with decoupling to SGND.
5	10, 11, 12	VP	Input Supply Voltage for the converter power stage. Must be closely decoupled to PGND.
6, 7	13, 14, 15	LX	Connect inductor to these pins. Switching node internally connected to the drain of both high and low-side MOSFETs.
8	1, 2, 3	PGND	Main power ground return pin. Connect to the output and input capacitor return. (see board layout rules)
	8, 16	n/c	Not internally connected.

Pin Configuration

MSOP-8
(Top view)



QFN33-16
(Top view)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{CC}, V_P	V_{CC}, V_P to GND	6	V
V_{LX}	LX to GND	-0.3 to V_P+0.3	V
V_{FB}	FB to GND	-0.3 to V_{CC}+0.3	V
V_{EN}	EN to GND	-0.3 to 6	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
V_{ESD}	ESD Rating [2] - HBM	3000	V

Notes:
1: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2: Human body model is a 100pF capacitor discharged through a 1.5K resistor into each pin.

Thermal Characteristics

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance (MSOP-8) [2]	150	°C/W
P_D	Maximum Power Dissipation (MSOP-8) (T_A = 25°C) [2, 3]	667	mW
Θ_{JA}	Thermal Resistance (QFN33-16) [2]	50	°C/W
P_D	Maximum Power Dissipation (QFN33-16) (T_A = 25°C) [2, 4]	2.0	W

Note 2: Mounted on a demo board.
Note 3: Derate 6.7mW/°C above 25°C.
Note 4: Derate 20mW/°C above 25°C.

Recommended Operating Conditions

Symbol	Description	Value	Units
T	Ambient Temperature Range	-40 to 85	°C

Electrical Characteristics[1]

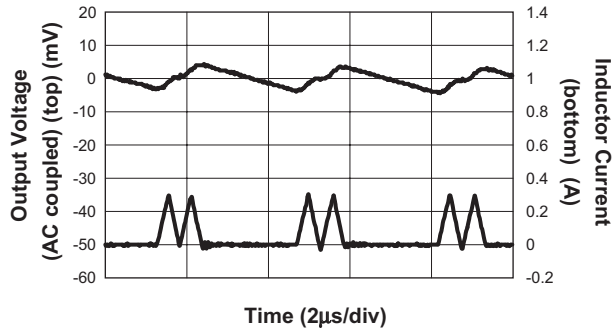
(V_{IN} = V_{CC} = V_P = 5V, T_A = -40 to 85°C unless otherwise noted. Typical values are at T_A = 25°C)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2.7		5.5	V
V_{OUT}	Output Voltage Tolerance	V_{IN} = V_{OUT} + 0.2 to 5.5V, I_{OUT} = 0 to 700 mA	-3.0		+3.0	%
V_{UVLO}	Under Voltage Lockout	V_{IN} Rising			2.5	V
		V_{IN} Falling	1.2			V
$V_{UVLO(HYS)}$	Under Voltage Lockout Hysteresis			250		mV
I_{IL}	Input Low Current	V_{IN} = V_{FB} = 5.5V			1.0	µA
I_{IH}	Input High Current	V_{IN} = V_{FB}= 0 V			1.0	µA
I_Q	Quiescent Supply Current	No Load, V_{FB}= 0 V		160	300	µA
I_{SHDN}	Shutdown Current	V_{EN} = 0 V, V_{IN}= 5.5V			1.0	µA
I_{LIM}	Current Limit	T_A = 25°C	1.2			A
$R_{DS(ON)L}$	High Side Switch On Resistance	T_A = 25°C		110	150	mΩ
$R_{DS(ON)H}$	Low Side Switch On Resistance	T_A = 25°C		100	150	mΩ
η	Efficiency	I_{OUT} = 300mA, V_{IN}= 3.5 V		92		%
ΔV_{OUT} (V_{OUT}*ΔV_{IN})	Load Regulation	V_{IN}= 4.2V, I_{LOAD} = 0 - 700mA		±0.9		%
$\Delta V_{OUT}/V_{OUT}$	Line Regulation	V_{IN}= 2.7 to 5.5V		±0.1		%/V
F_{OSC}	Oscillator Frequency	T_A = 25°C	600	850	1200	KHz
$V_{EN(L)}$	Enable Threshold Low				0.6	V
$V_{EN(H)}$	Enable Threshold High		1.4			V
T_{SD}	Over Temp Shutdown Threshold			140		°C
T_{HYS}	Over Temp Shutdown Hysteresis			15		°C

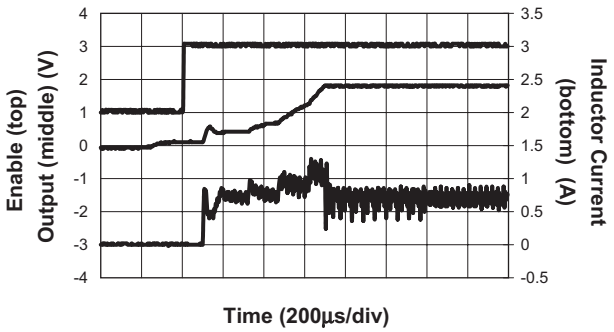
Note 1: The AAT1151 is guaranteed to meet performance specification over the -40 to 85°C operating range and are assured by design, characterization and correlation with statistical process controls.

Typical Characteristics

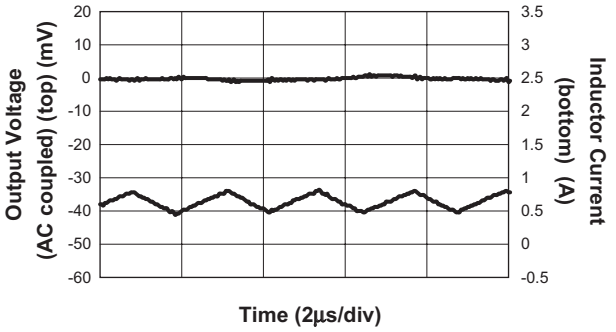
Output Ripple 1.8V 50mA V_{IN} = 3.6V
Circuit of Figure 1



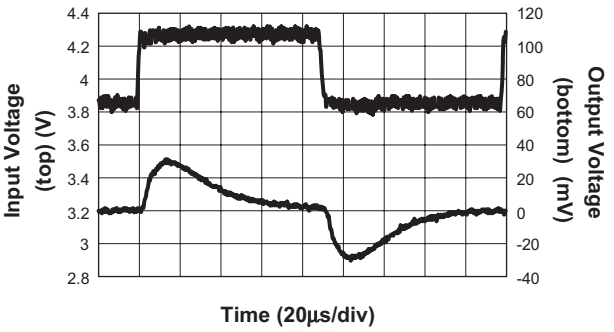
Soft Start 1.8V 0.7A V_{IN} = 3.6V
Circuit of Figure 1



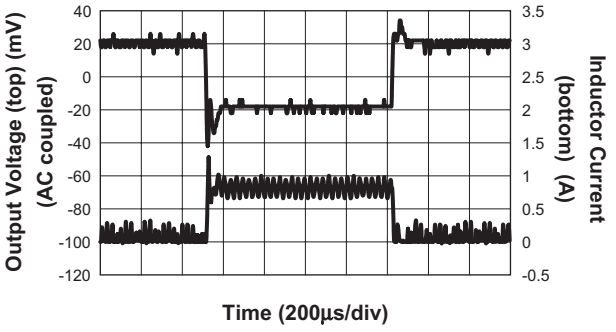
Output Ripple 1.8V 0.7A V_{IN} = 3.6V
Circuit of Figure 1



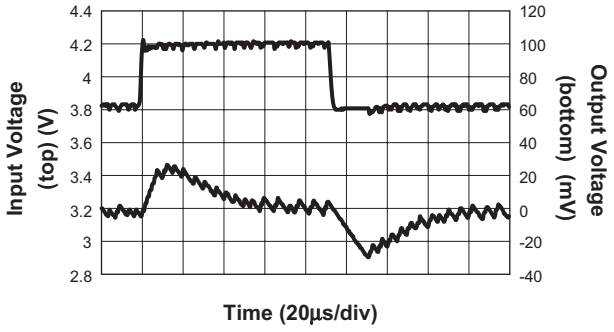
Line Transient Response 1.8V 0.7A
Circuit of Figure 1



Load Transient Response 50mA to 0.7A
V_{IN} = 3.6V – Circuit of Figure 1

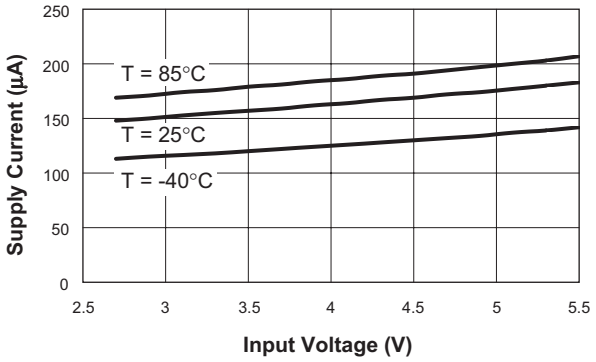


Line Transient Response 1.8V 50mA
Circuit of Figure 1

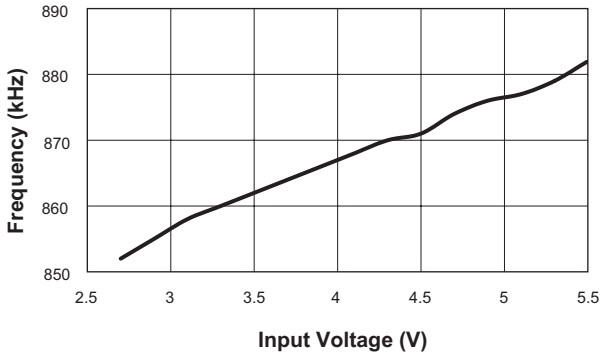


Typical Characteristics

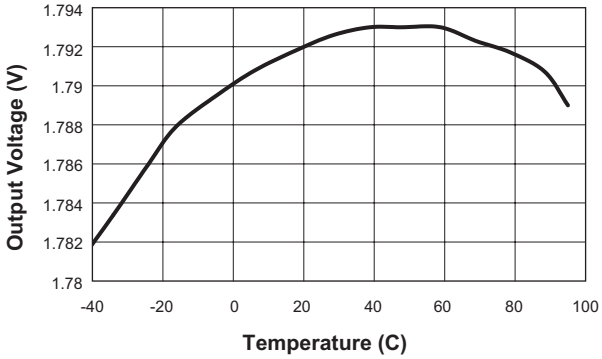
No Load Supply Current vs. Input Voltage



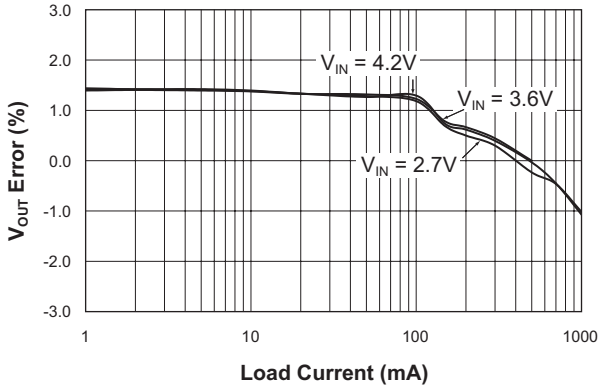
Frequency vs. Input Voltage



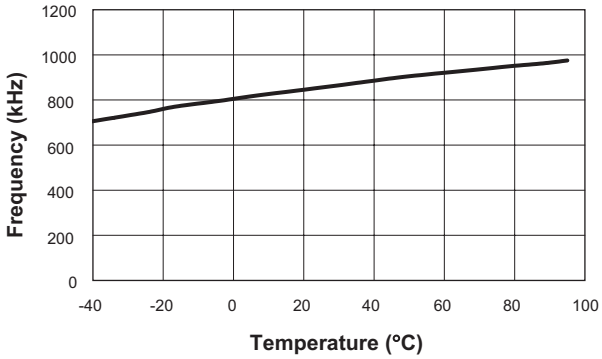
Output Voltage vs. Temperature



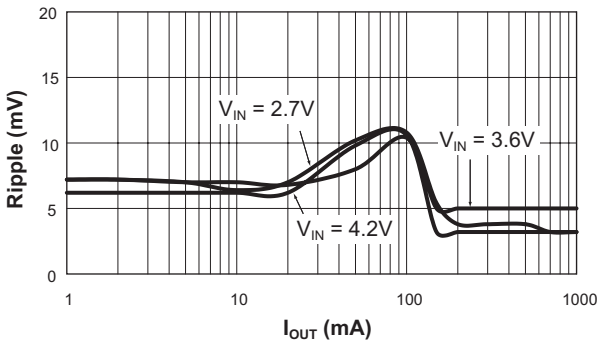
Load and Line Regulation



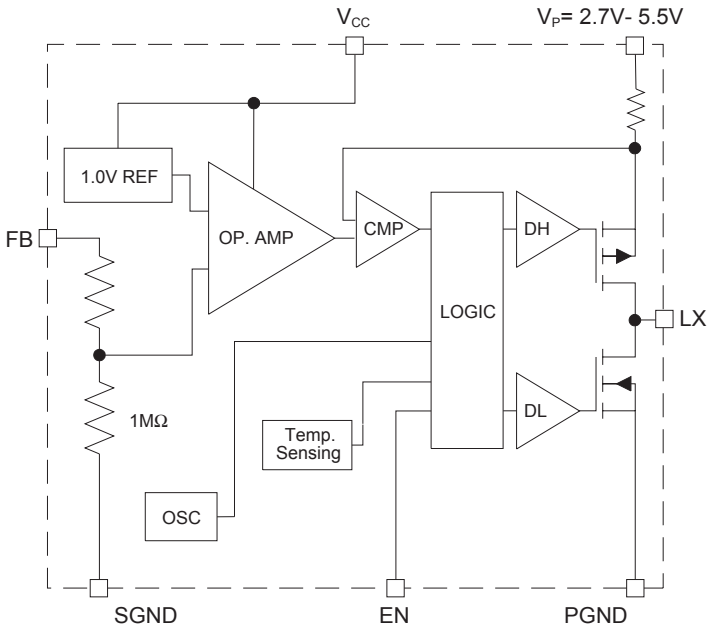
Switching Frequency vs. Temperature



Output Ripple
Circuit of Figure 1



Functional Block Diagram



Operation

Control Loop

The AAT1151 is a peak current mode buck converter. The inner, wide bandwidth loop controls the peak current of the output inductor. The output inductor current is sensed through the P-Channel MOSFET (high side) and is also used for short circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability. The loop appears as a voltage programmed current source in parallel with the output capacitor.

The voltage error amplifier output programs the current loop for the necessary inductor current to force a constant output voltage for all load and line conditions. The voltage feedback resistive divider is internal, dividing the output voltage to the error amplifier reference voltage of 1.0V. The voltage error amplifier does not have a large DC gain typical of most error amplifiers. This eliminates the need for external compensation components while still providing sufficient DC loop gain for load regulation. The voltage loop crossover frequency and phase margin are set by the output capacitor value only.

PFM/PWM Operation

Light load efficiency is maintained by way of Pulse Frequency Modulation (PFM) control. The AAT1151 PFM control forces the peak inductor current to a minimum level regardless of load demand. At medium to high load demand this has no effect on circuit operation and normal PWM controls take over. PFM reduces the switching frequency at light loads thus reducing the associated switching losses.

Soft-Start/Enable

Soft start increases the inductor current limit point in discrete steps when the input voltage or enable input is applied. It limits the current surge seen at the input and eliminates output voltage overshoot. The enable input, when pulled low, forces the AAT1151 into a low power non-switching state. The total input current during shutdown is less that 1µA.

Power and Signal Source

Separate small signal ground and power supply pins isolate the internal control circuitry from the noise associated with the output MOSFET switching. The low pass filter R1 and C3 in schematic figures 3 and 4 filters the noise associated with the power switching.

Current Limit and Over-temperature Protection

For overload conditions the peak input current is limited. Figure 1 displays the VI current limit characteristics. As load impedance decreases and the output voltage falls closer to zero, more power is dissipated internally, raising the device temperature. Thermal protection completely disables switching when internal dissipation becomes excessive, protecting the device from damage. The junction over-temperature threshold is 140°C with 10°C of hysteresis.

Inductor

The output inductor is selected to limit the ripple current to some predetermined value, typically 20-40% of the full load current at the maximum input voltage. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under all normal load conditions. During over load and transient conditions, the average current in the inductor can meet or exceed the current limit point of the AAT1151. These conditions can tolerate greater saturation in the inductor without degradation in converter performance. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

For a 1.0 Amp load and the ripple set to 40% at the maximum input voltage, the maximum peak to peak ripple current is 280mA. The inductance value required is 2.84µH.

$$L = \frac{V_{OUT}}{I_O \cdot k \cdot F} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= \left(\frac{1.5V}{1A \cdot 0.4 \cdot 850kHz}\right) \cdot 1 - \left(\frac{1.5V}{4.2V}\right)$$

$$= 2.84\mu H$$

The factor "k" is the fraction of full load selected for the ripple current at the maximum input voltage. For ripple current at 40% of the full load current the peak current at will be 120% of full load. Selecting a standard value of 3.0µH gives 38% ripple current. A 3.0µH inductor selected from the Sumida CDRH5D28 series has a 24 mΩ DCR and a 2.4 DC current rating. At full load the inductor DC loss is 24mW which amounts to a 1.6% loss in efficiency.

Input Capacitor

The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the AAT1151. A low ESR/ESL ceramic capacitor is ideal for this function. To minimize the stray inductance the capacitor should be placed as close as possible to the IC. This keeps the high frequency content of the input current localized; minimizing radiated and conducted EMI while facilitating optimum performance of the AAT1151. Ceramic X5R or X7R capacitors are ideal for this function. The size required will vary depending on the load, output voltage and input voltage source impedance characteristics. A Typical value is around 10µF. The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current reaches a maximum when V_{IN} is two times the output voltage where it is approximately one half of the load current. Losses associated with the input ceramic capacitor are typically minimal and not an issue. The proper placement of the input capacitor can be seen in the reference design layout in figure 3.

Output Capacitor

Since there are no external compensation components, the output capacitor has a strong effect on loop stability. Lager output capacitance will reduce the crossover frequency with greater phase margin. For the 1.5V 1A design using the 4.1µH inductor, a 47µF capacitor provides a stable loop but with only 35 degrees of phase margin at a crossover frequency of 100 kHz. Doubling the capacitance to 100µF reduces the crossover frequency to half while increasing the phase margin to 60 degrees. In addition to assisting stability, the output capacitor limits the output ripple

and provides holdup during large load transitions. A 100uF X5R or X7R ceramic capacitor provides sufficient bulk capacitance to stabilize the output during large load transitions and has ESR and ESL characteristics necessary for low output ripple. The output capacitor rms ripple current is given by

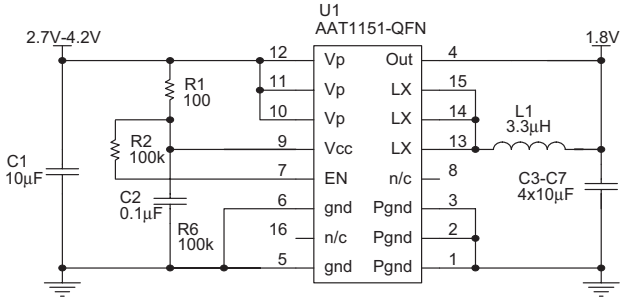
$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}+V_{FWD}) \cdot (V_{IN} - V_{OUT})}{L \cdot F \cdot V_{IN}}$$

For a ceramic capacitor the ESR is so low that dissipation due to the rms current of the capacitor is not a concern. Tantalum capacitors with sufficiently low ESR to meet output voltage ripple requirements also have an RMS current rating well beyond that actually seen in this application.

Layout

Figures 2 and 3 display the suggested PCB layout for the AAT1151. The following guidelines should be used to help insure a proper layout.

- The input capacitor (C1) should connect as closely as possible to V_{POWER} (pin 5) and P_{GND} (pin 8).
- C2, and L1, should be connected as closely as possible. The connection L1 to the LX node should be as short as possible.
- The feedback trace (pin 1) should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high current load trace will degrade DC load regulation.
- The resistance of the trace from the load return to the PGND (pin 8) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power gnd.
- Low pass filter R1 and C3 provide a cleaner bias source for the AAT1151 active circuitry. C3 should be placed as close as possible to SGND (pin 2) and V_{CC} (pin 4).



C1 Murata 10uF 6.3V X5R GRM42-6X5R106K6.3
C2-C5 MuRata 10uF 6.3V GRM21BR60J106KE01L
L1 Sumida CDRH3D16-4R7NC or CDRH3D16-3R3NC

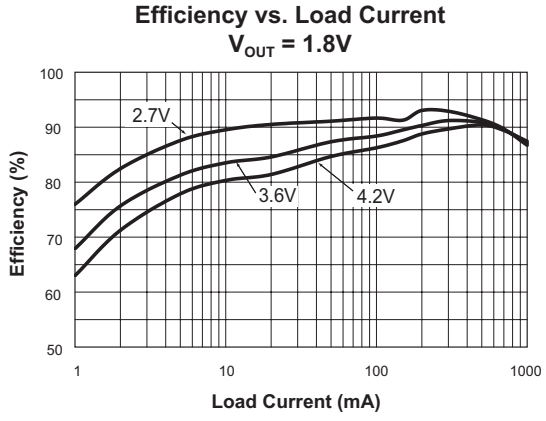


Figure 1.

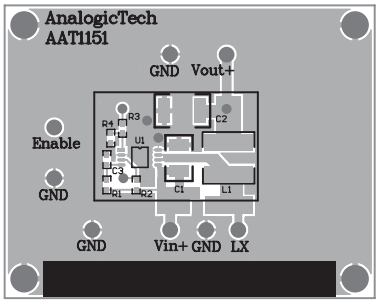


Figure 2: MSOP Evaluation Board Top Layer

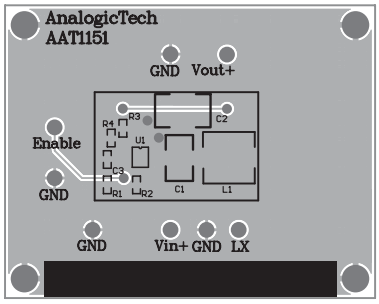


Figure 3: MSOP Evaluation Board Bottom Layer

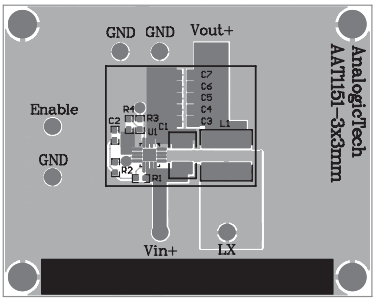


Figure 4: QFN Evaluation Board Top Side

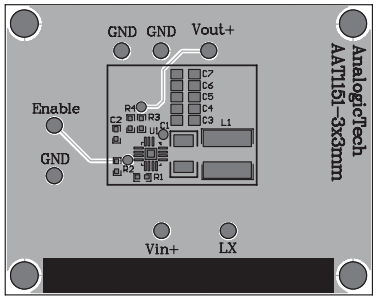


Figure 5: QFN Evaluation Board Bottom Side

Thermal Calculations

There are two types of losses associated with the AAT1151 output switching MOSFET, switching losses and conduction losses. The conduction losses are associated with the $R_{DS(ON)}$ characteristics of the output switching device. At the full load condition, assuming continuous conduction mode (CCM), a simplified form of the total losses is given by

$$P = \frac{I_O2 \cdot (R_{DSON(HS)} \cdot V_O + R_{DSON(LS)} \cdot (V_{IN} \cdot V_O))}{V_{IN}}$$

$$+ (t_{SW} \cdot F \cdot I_O \cdot V_{IN} + I_Q) \cdot V_{IN}$$

where I_q is the AAT1151 quiescent current.

Once the total losses have been determined the junction temperature can be derived from the θ_{JA} for the MSOP-8 package.

$$T_J = P \cdot \theta_{JA} + T_{AMB}$$

Adjustable Output

For applications requiring an output other than the fixed available, the 1V version can be programmed externally. Resistors R3 and R4 of figure 5 force the output to regulate higher than 1 Volt. R4 should be 100 times less than the 1MΩ internal resistance of the FB pin (recommended 10kΩ). Once R4 is selected R3 can be calculated. For a 1.25 Volt output with R4 set to 10.0kΩ, R3 is 2.55kΩ.

$$R3 = (V_O - 1) \cdot R4 = 0.25 \cdot 10k\Omega = 2.55k\Omega$$

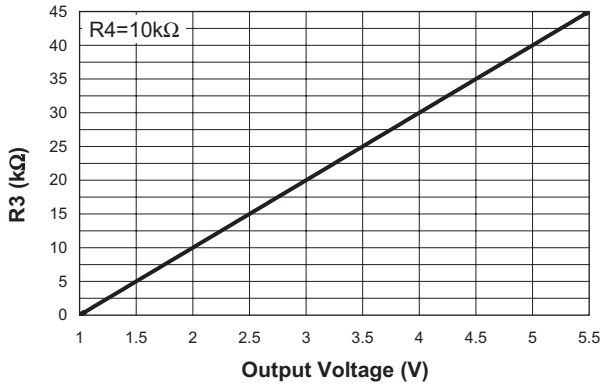
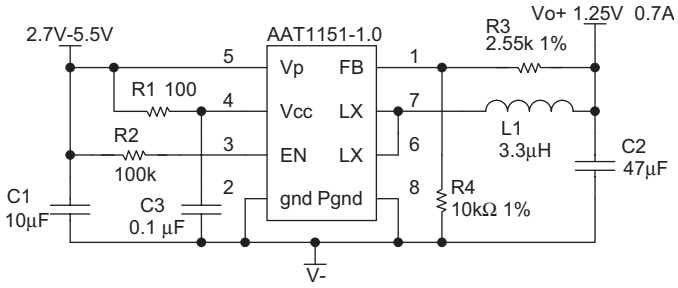


Figure 6: R3 vs. V_{OUT} for Adjustable Output using the AAT1151-1.0V



C1 Murata 10µF 6.3V X5R GRM42-6X5R106K6.3
C2 MuRata 100µF 6.3V GRM43-2 X5R 476M 47µF 6.3V
L1 Sumida CDRH3D16-3R3 NC

Figure 7: Adjustable Output Schematic

Design Example

Specifications

I_{OUT} 0.7A

I_{RIPPLE} 40% of full load at max V_{IN}

V_{OUT} 1.5V

V_{IN} 2.7-4.2 V (3.6V nominal)

F_S 850 kHz

T_{AMB} = 85°C

Maximum input capacitor ripple:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = 0.35\text{Arms}$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot 0.35^2\ A = 0.6mW$$

Inductor Selection:

$$L = \frac{V_{OUT}}{I_O \cdot k \cdot F} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{1.5V}{0.7A \cdot 0.4 \cdot 850kHz} \cdot \left(1 - \frac{1.5V}{4.2V}\right) = 4.05\mu H$$

Select Sumida inductor CDRH3D16 3.3µH 63mΩ 1.8 mm height.

$$\Delta I = \frac{V_O}{L \cdot F} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1.5V}{3.3\mu H \cdot 850kHz} \cdot \left(1 - \frac{1.5V}{4.2V}\right) = 340mA$$

$$I_{PK} = I_{OUT} + \frac{\Delta I}{2} = 0.7A + 0.17A = 0.87A$$

$$P = I_O^2 \cdot DCR = (0.7)^2 \cdot 63mW = 31mW$$

Output Capacitor Ripple Current:

$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{L \cdot F \cdot V_{IN}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.5V \cdot (4.2V - 1.5V)}{3.3\mu H \cdot 850kHz \cdot 4.2V} = 99\text{mArms}$$

$$Pesr = esr \cdot I_{RMS}^2 = 5m\Omega \cdot 99^2\ mA = 50\mu W$$

AAT1151 dissipation:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DSON(H)} \cdot V_O + R_{DSON(L)} \cdot (V_{IN} - V_O))}{V_{IN}} + (t_{sw} \cdot F \cdot I_O + I_Q) \cdot V_{IN}$$

$$= \frac{(0.7^2) \cdot (0.2\Omega \cdot 1.5V + 0.187\Omega \cdot (4.2V - 1.5V))}{4.2V} + (20nsec \cdot 850kHz \cdot 0.7A + 0.3mA) \cdot 4.2V = 0.145W$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + 150°C/W \cdot 0.145W = 107°C \quad (MSOP\text{-}8)$$

$$= 85°C + 50°C/W \cdot 0.145W = 92°C \quad (QFN33\text{-}16)$$

Surface Mount Inductors

Manufacturer	Part Number	Value	Max DC Current	DCR (Ω)	Size (mm) L × W × H	Type
TaiyoYuden	NPO5DB4R7M	4.7µH	1.4A	.038	5.9x6.1x2.8	Shielded
Toko	A914BYW-3R5M-D52LC	3.5µH	1.34A	.073	5.0x5.0x2.0	Shielded
Sumida	CDRH5D28-3R0	3.0µH	2.4A	.024	5.7x5.7x3.0	Shielded
Sumida	CDRH5D28-4R2	4.2µH	2.2A	.031	5.7x5.7x3.0	Shielded
Sumida	CDRH5D18-4R1	4.1µH	1.95A	.057	5.7x5.7x2.0	Shielded
MuRata	LQH55DN4R7M03	4.7µH	2.7A	.041	5.0x5.0x4.7	Non-Shielded
MuRata	LQH66SN4R7M03	4.7µH	2.2A	.025	6.3x6.3x4.7	Shielded
MuRata	CDRH3D16-3R3	3.3µH	1.1A	.063	3.8x3.8x1.8	Shielded

Surface Mount Capacitors

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
TDK	C4532X5ROJ107M	100µF	6.3V	X5R	1812
MuRata	GRM43-2 X5R 107M 6.3	100µF	6.3V	X5R	1812
MuRata	GRM43-2 X5R 476K 6.3	47µF	6.3V	X5R	1812
MuRata	GRM40 X5R 106K 6.3	10µF	6.3V	X5R	0805
MuRata	GRM42-6 X5R 106K 6.3	10µF	6.3V	X5R	1206

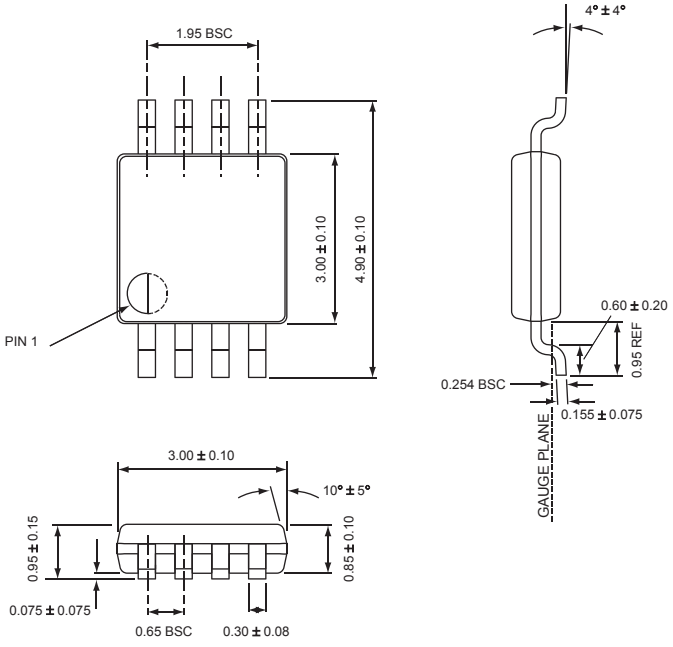
Ordering Information

Output Voltage[1]	Package	Marking[2]	Part Number (Tape and Reel)
1.0V (Adj $V_{OUT} \geq 1.0V$)	MSOP-8	JHXYY	AAT1151IKS-1.0-T1
1.0V (Adj $V_{OUT} \geq 1.0V$)	QFN33-16	JHXYY	AAT1151IVN-1.0-T1
1.8V	MSOP-8	JIXYY	AAT1151IKS-1.8-T1
2.5V	MSOP-8	JJXYY	AAT1151IKS-2.5-T1

Notes
1. Contact local sales office for custom options.
2. XYY = assembly and date code.

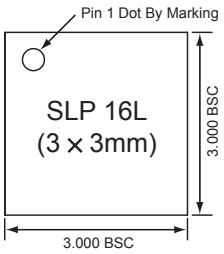
Package Information

MSOP-8

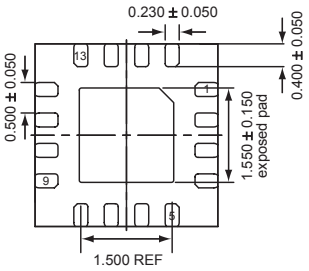


All dimensions in millimeters.

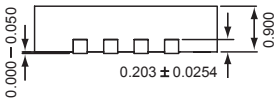
QFN33-16



Top View



Bottom View



Side View

All dimensions in millimeters.

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