

P-Channel 40-V (D-S) 175°C MOSFET

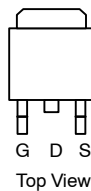
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^d
-40	0.0042 @ $V_{GS} = -10$ V	-110
	0.0062 @ $V_{GS} = -4.5$ V	-110

FEATURES

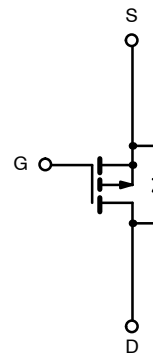
- TrenchFET® Power MOSFET
- New Package with Low Thermal Resistance

APPLICATIONS

- Automotive
 - 12-V Boardnet
 - High-Side Switches
 - Motor Drives

TO-263


Ordering Information: SUM110P04-04L



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^d ($T_J = 175^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	-110
		$T_C = 125^\circ\text{C}$	-110
Pulsed Drain Current	I_{DM}	-240	A
Avalanche Current	I_{AS}	-75	
Single Pulse Avalanche Energy ^a	E_{AS}	281	mJ
Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	375°
		$T_A = 25^\circ\text{C}^b$	3.75
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient PCB Mount ^b	R_{thJA}	40	$^\circ\text{C}/\text{W}$
Junction-to-Case	R_{thJC}	0.4	

Notes:

- Duty cycle $\leq 1\%$.
- When mounted on 1" square PCB (FR-4 material).
- See SOA curve for voltage derating.
- Limited by package.

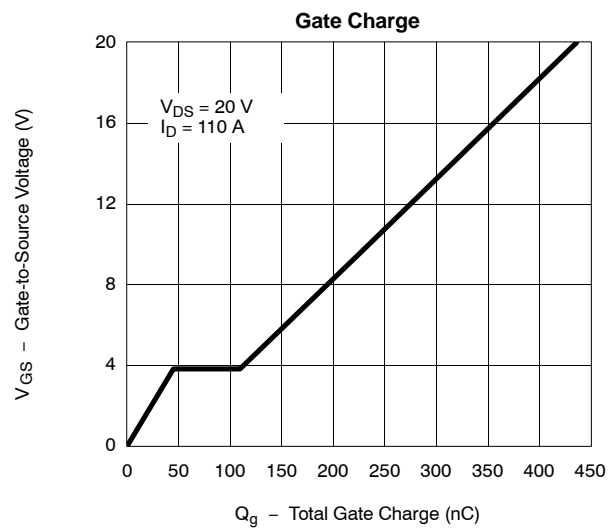
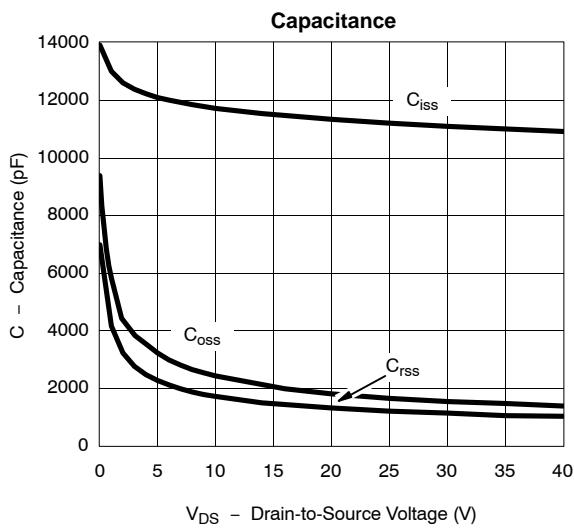
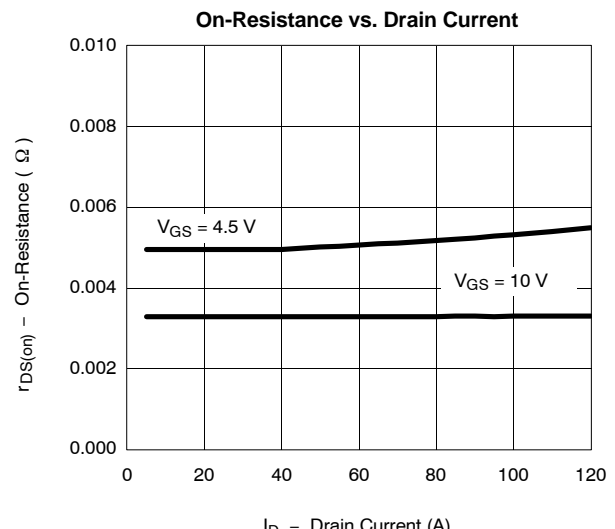
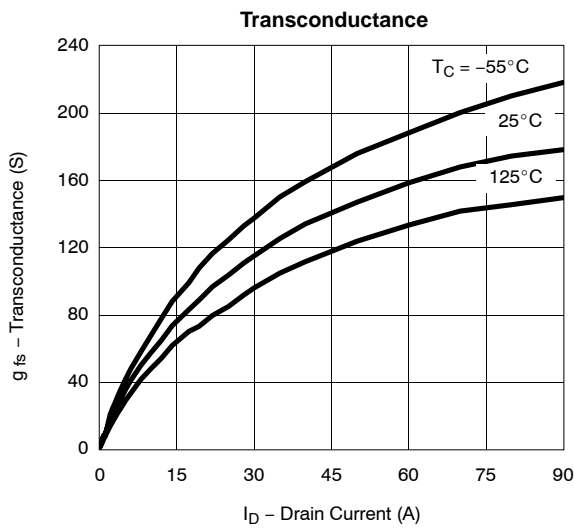
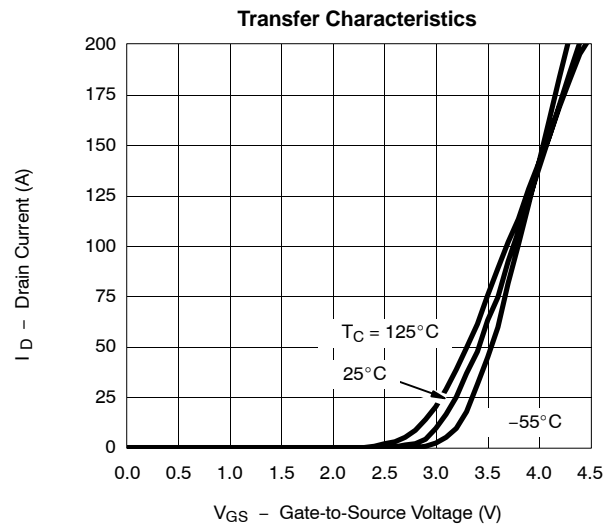
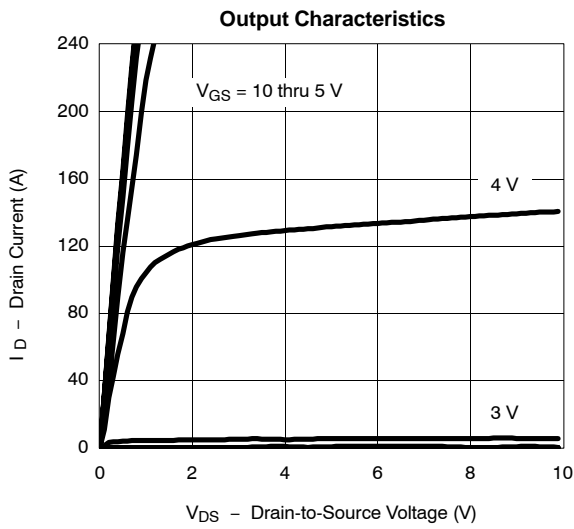
SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1		-3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -40 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -40 V, V _{GS} = 0 V, T _J = 125 °C			-50	
		V _{DS} = -40 V, V _{GS} = 0 V, T _J = 175 °C			-250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	-120			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -10 V, I _D = -30 A		0.0034	0.0042	Ω
		V _{GS} = -10 V, I _D = -30 A, T _J = 125 °C			0.0063	
		V _{GS} = -10 V, I _D = -30 A, T _J = 175 °C			0.0076	
		V _{GS} = -4.5 V, I _D = -20 A		0.005	0.0062	
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -30 A	20			S
Dynamic^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -25 V, f = 1 MHz		11200		pF
Output Capacitance	C _{oss}			1650		
Reverse Transfer Capacitance	C _{rss}			1200		
Total Gate Charge ^c	Q _g	V _{DS} = -20 V, V _{GS} = -10 V, I _D = -110 A		235	350	nC
Gate-Source Charge ^c	Q _{gs}			45		
Gate-Drain Charge ^c	Q _{gd}			65		
Gate Resistance	R _g			3		Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = -20 V, R _L = 0.18 Ω I _D ≈ -110 A, V _{GEN} = -10 V, R _g = 2.5 Ω		25	40	ns
Rise Time ^c	t _r			30	45	
Turn-Off Delay Time ^c	t _{d(off)}			190	300	
Fall Time ^c	t _f			110	165	
Source-Drain Diode Ratings and Characteristics (T_C = 25 °C)^b						
Continuous Current	I _s				-110	A
Pulsed Current	I _{SM}				-240	
Forward Voltage ^a	V _{SD}	I _F = -85 A, V _{GS} = 0 V		-1.0	-1.5	V
Reverse Recovery Time	t _{rr}	I _F = -85 A, di/dt = 100 A/μs		65	100	ns
Peak Reverse Recovery Current	I _{RM(REC)}			-3.7	-5.6	A
Reverse Recovery Charge	Q _{rr}				0.12	0.28

Notes:

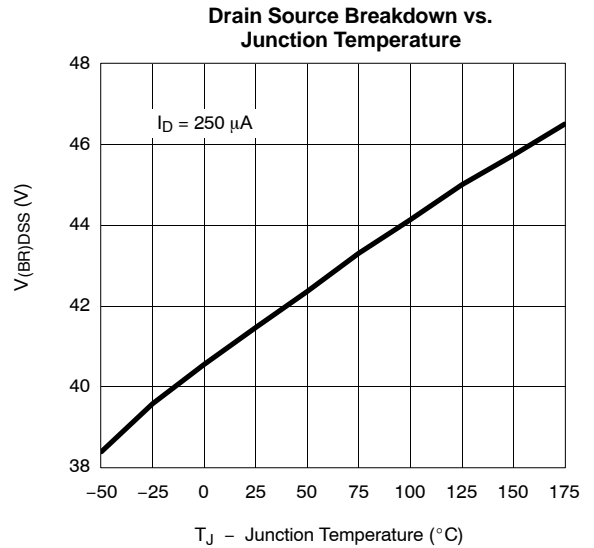
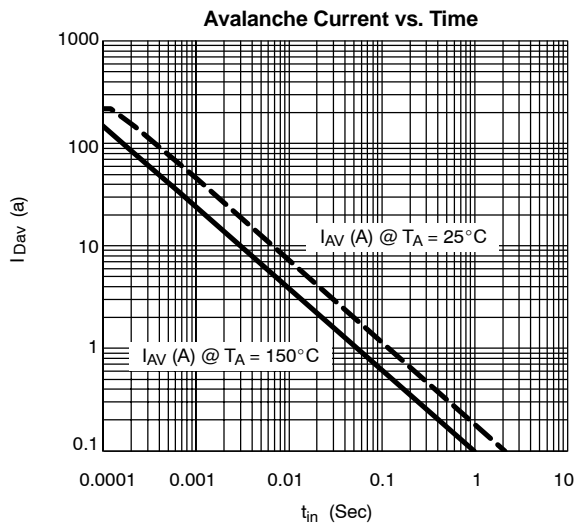
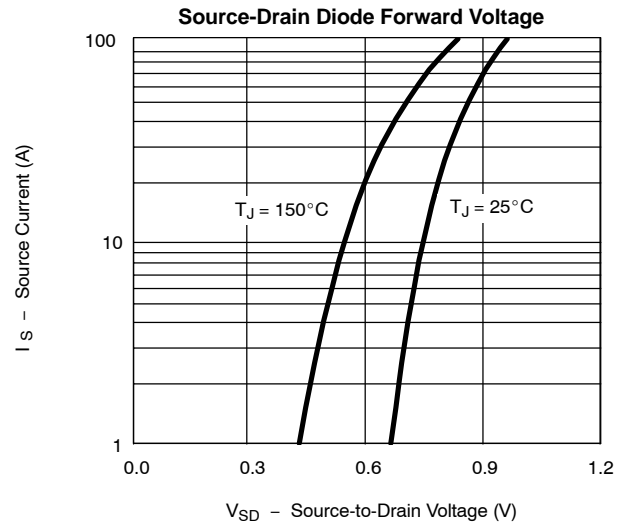
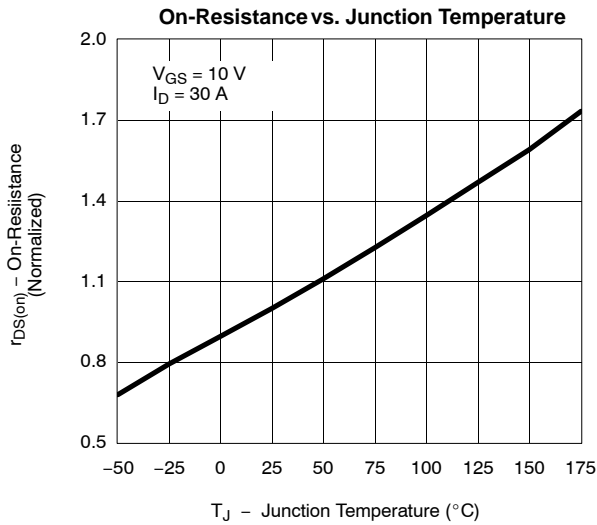
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



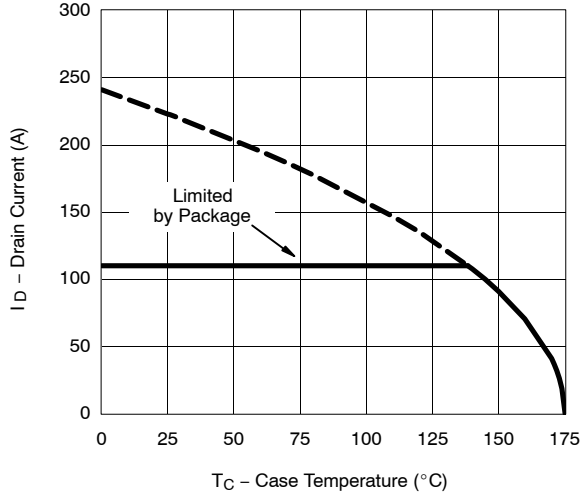
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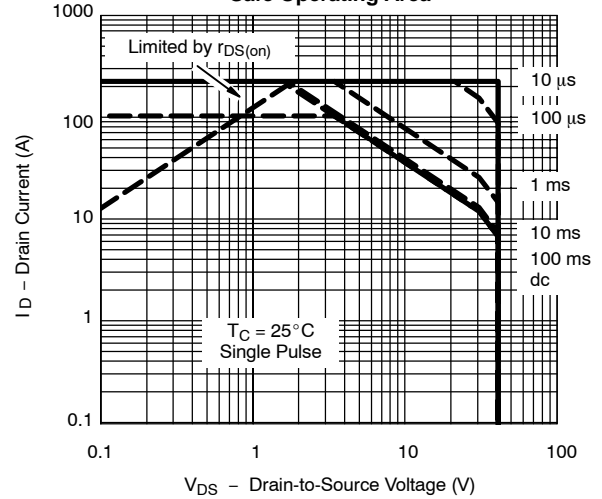


THERMAL RATINGS

Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

