

S3086

Continuous Rate Clock Recovery Unit

Features

- SiGe BiCMOS technology
- Complies with Telcordia and ITU-T specifications for jitter tolerance, jitter transfer and jitter generation
- On-chip high-frequency PLL with loop filter for clock recovery
- Programmable signal detect input active High or active Low (LVTTTL and LVPECL Input)
- Supports clock recovery from 30 Mbps to 2.7 Gbps with no gaps
- Capable of working at OC-48 with Forward or Correction (FEC), OC-48, FireWire, HDTV, GE, FC, OC-12, DTV, ESCON, OC-3, FDDI, FE, OC-1 and DS-3 rates
- Selectable optional reference clock
- (19.44/155.52 MHz for SONET rates or user defined for non-SONET rates)
- Loss-of-Lock Indication
- Low jitter serial interface
- +3.3 V single power supply
- Compact 48-pin TQFP/TEP Green/RoHS compliant package
- Typical power 825 mW (Serial Clock Enabled)
- Typical power 700 mW (Serial Clock Disabled)

Applications

- SONET/SDH/ATM/OC-3/OC-12/OC-48
- Fibre Channel
- Gigabit Ethernet/Fast Ethernet
- High Definition Television/Digital Television (HDTV/DTV)
- FireWire
- Fibre Distributed Data Interface (FDDI)
- Enterprise Systems Connection (ESCON)
- DS-3

Description

The S3086 Continuous Rate Clock Recovery Unit (CRU) is a variable rate clock recovery interface device. This device is suitable for use in applications such as SONET/SDH, Fibre Channel, Fast Ethernet, HDTV, ESCON, Gigabit Ethernet, and DS-3. The chip performs all necessary clock recovery functions in conformance with the Telcordia 253, IEEE 802.3, and SMPTE 292/184 transmission standards.

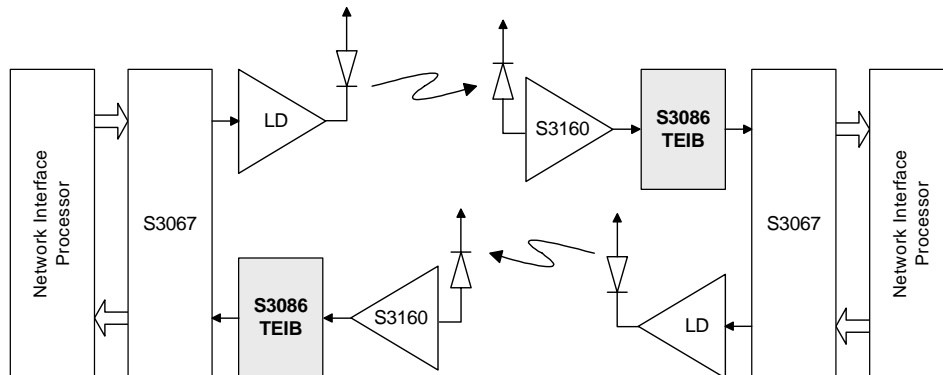
The S3086 CRU is capable of accepting a scrambled 30 Mbps to 2.7 Gbps serial NRZ data stream. It can derive a data clock from the data stream and output the data stream retimed and aligned with a companion serial bit clock. The S3086 achieves its continuous rate capability in a piece-wise continuous manner. This means that the full operating range is provided through the selection of one of twenty six (26) overlapping bands which are uniquely identified/programmed a by 5-bit band select input bus. The S3086 is implemented using AMCC's proven Phase Lock Loop (PLL) technology. Figure 1 shows a typical network application for the S3086.

An external reference oscillator should be used for applications, including SONET/SDH, in which continuous down-stream clocking is a requirement under Loss-of-Signal (LOS) conditions.

The S3086 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a Voltage Controlled Oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage.

AMCC Suggested Interface Devices

S3055	OC-48/12/3 Multi-Rate Transceiver
S3057	OC-48 Transceiver
S3059	OC-48 Transceiver
S3067	OC-48/12/3 Multi-Rate Transceiver



System Block Diagram with the S3086

S3086



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