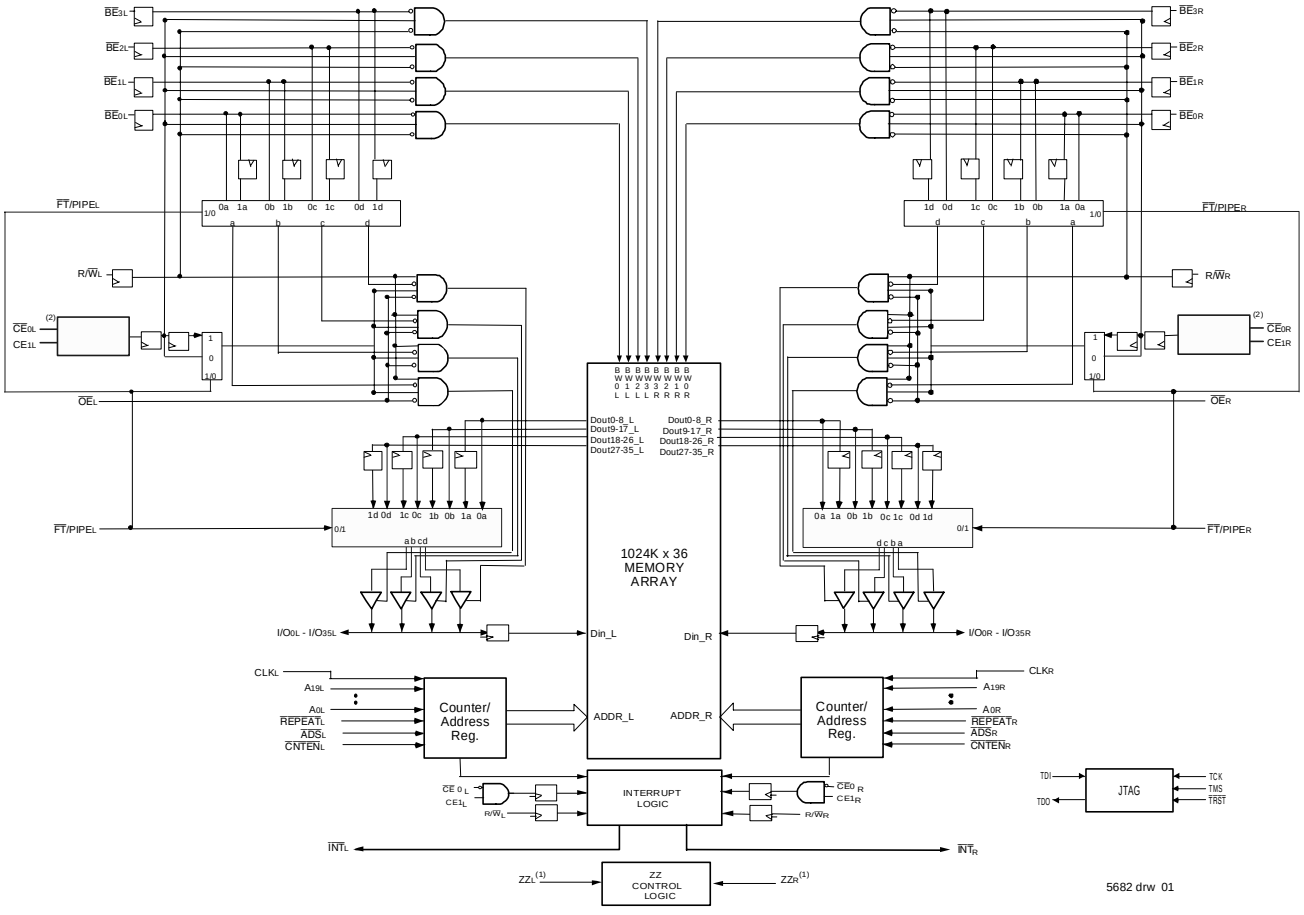
# HIGH-SPEED 2.5V 1024K x 36 SYNCHRONOUS DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

**IDT70T3509M**

## Features:

- **True Dual-Port memory cells which allow simultaneous access of the same memory location**
- **High-speed data access**
  - *Commercial: 4.2ns (133MHz)(max.)*
  - *Industrial: 4.2ns (133MHz)(max.)*
- **Selectable Pipelined or Flow-Through output mode**
- **Counter enable and repeat features**
- **Interrupt Flags**
- **Full synchronous operation on both ports**
  - *7.5ns cycle time, 133MHz operation (9.5Gbps bandwidth)*
  - *1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 133MHz*
  - *Fast 4.2ns clock to data out*
  - *Data input, address, byte enable and control registers*
  - *Self-timed write allows fast cycle time*
- **Separate byte controls for multiplexed bus and bus matching compatibility**
- **Dual Cycle Deselect (DCD) for Pipelined Output Mode**
- **2.5V (±100mV) power supply for core**
- **LVTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port**
- **Includes JTAG functionality**
- **Available in a 256-pin Ball Grid Array (BGA)**
- **Common BGA footprint provides design flexibility over seven density generations (512K to 36M-bit)**
- **Green parts available, see ordering information**

## Functional Block Diagram




**NOTE:**

1. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/$\overline{FT}$x and OPTx and the sleep mode pins themselves (ZZx) are not affected during sleep mode.
2. See Truth Table I for Functionality.

AUGUST 2007

## Description:

The IDT70T3509M is a high-speed 1024K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70T3509M has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and $CE_1$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70T3509M can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device ($V_{DD}$) is at 2.5V.

# Pin Configuration (1,2,3,4)

## 70T3509M BP
## BP-256(5,7)

## 256-Pin BGA
## Top View(6)

08/03/04

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 NC | A2 TDI | A3 $A_{19L}$ | A4 $A_{17L}$ | A5 $A_{14L}$ | A6 $A_{11L}$ | A7 $A_{8L}$ | A8 $\overline{BE}_{2L}$ | A9 $CE_{1L}$ | A10 $\overline{OE}_L$ | A11 $\overline{CNTEN}_L$ | A12 $A_{5L}$ | A13 $A_{2L}$ | A14 $A_{0L}$ | A15 NC | A16 NC |
| B1 $I/O_{18L}$ | B2 NC | B3 TDO | B4 $A_{18L}$ | B5 $A_{15L}$ | B6 $A_{12L}$ | B7 $A_{9L}$ | B8 $\overline{BE}_{3L}$ | B9 $\overline{CE}_{0L}$ | B10 $R/\overline{W}_L$ | B11 $\overline{REPEAT}_L$ | B12 $A_{4L}$ | B13 $A_{1L}$ | B14 $V_{DD}$ | B15 $I/O_{17L}$ | B16 NC |
| C1 $I/O_{18R}$ | C2 $I/O_{19L}$ | C3 $V_{SS}$ | C4 $A_{16L}$ | C5 $A_{13L}$ | C6 $A_{10L}$ | C7 $A_{7L}$ | C8 $\overline{BE}_{1L}$ | C9 $\overline{BE}_{0L}$ | C10 $CLK_L$ | C11 $\overline{ADS}_L$ | C12 $A_{6L}$ | C13 $A_{3L}$ | C14 $OPT_L$ | C15 $I/O_{17R}$ | C16 $I/O_{16L}$ |
| D1 $I/O_{20R}$ | D2 $I/O_{19R}$ | D3 $I/O_{20L}$ | D4 $PIPE/\overline{FT}_L$ | D5 $V_{DDQL}$ | D6 $V_{DDQL}$ | D7 $V_{DDQR}$ | D8 $V_{DDQR}$ | D9 $V_{DDQL}$ | D10 $V_{DDQL}$ | D11 $V_{DDQR}$ | D12 $V_{DDQR}$ | D13 $V_{DD}$ | D14 $I/O_{15R}$ | D15 $I/O_{15L}$ | D16 $I/O_{16R}$ |
| E1 $I/O_{21R}$ | E2 $I/O_{21L}$ | E3 $I/O_{22L}$ | E4 $V_{DDQL}$ | E5 $V_{DD}$ | E6 $V_{DD}$ | E7 $\overline{INT}_L$ | E8 $V_{SS}$ | E9 $V_{SS}$ | E10 $V_{SS}$ | E11 $V_{DD}$ | E12 $V_{DD}$ | E13 $V_{DDQR}$ | E14 $I/O_{13L}$ | E15 $I/O_{14L}$ | E16 $I/O_{14R}$ |
| F1 $I/O_{23L}$ | F2 $I/O_{22R}$ | F3 $I/O_{23R}$ | F4 $V_{DDQL}$ | F5 $V_{DD}$ | F6 NC | F7 NC | F8 $V_{SS}$ | F9 $V_{SS}$ | F10 $V_{SS}$ | F11 $V_{SS}$ | F12 $V_{DD}$ | F13 $V_{DDQR}$ | F14 $I/O_{12R}$ | F15 $I/O_{13R}$ | F16 $I/O_{12L}$ |
| G1 $I/O_{24R}$ | G2 $I/O_{24L}$ | G3 $I/O_{25L}$ | G4 $V_{DDQR}$ | G5 $V_{SS}$ | G6 $V_{SS}$ | G7 $V_{SS}$ | G8 $V_{SS}$ | G9 $V_{SS}$ | G10 $V_{SS}$ | G11 $V_{SS}$ | G12 $V_{SS}$ | G13 $V_{DDQL}$ | G14 $I/O_{10L}$ | G15 $I/O_{11L}$ | G16 $I/O_{11R}$ |
| H1 $I/O_{26L}$ | H2 $I/O_{25R}$ | H3 $I/O_{26R}$ | H4 $V_{DDQR}$ | H5 $V_{SS}$ | H6 $V_{SS}$ | H7 $V_{SS}$ | H8 $V_{SS}$ | H9 $V_{SS}$ | H10 $V_{SS}$ | H11 $V_{SS}$ | H12 $V_{SS}$ | H13 $V_{DDQL}$ | H14 $I/O_{9R}$ | H15 $IO_{9L}$ | H16 $I/O_{10R}$ |
| J1 $I/O_{27L}$ | J2 $I/O_{28R}$ | J3 $I/O_{27R}$ | J4 $V_{DDQL}$ | J5 $ZZ_R$ | J6 $V_{SS}$ | J7 $V_{SS}$ | J8 $V_{SS}$ | J9 $V_{SS}$ | J10 $V_{SS}$ | J11 $V_{SS}$ | J12 $ZZ_L$ | J13 $V_{DDQR}$ | J14 $I/O_{8R}$ | J15 $I/O_{7R}$ | J16 $I/O_{8L}$ |
| K1 $I/O_{29R}$ | K2 $I/O_{29L}$ | K3 $I/O_{28L}$ | K4 $V_{DDQL}$ | K5 $V_{SS}$ | K6 $V_{SS}$ | K7 $V_{SS}$ | K8 $V_{SS}$ | K9 $V_{SS}$ | K10 $V_{SS}$ | K11 $V_{SS}$ | K12 $V_{SS}$ | K13 $V_{DDQR}$ | K14 $I/O_{6R}$ | K15 $I/O_{6L}$ | K16 $I/O_{7L}$ |
| L1 $I/O_{30L}$ | L2 $I/O_{31R}$ | L3 $I/O_{30R}$ | L4 $V_{DDQR}$ | L5 $V_{DD}$ | L6 NC | L7 NC | L8 $V_{SS}$ | L9 $V_{SS}$ | L10 $V_{SS}$ | L11 $V_{SS}$ | L12 $V_{DD}$ | L13 $V_{DDQL}$ | L14 $I/O_{5L}$ | L15 $I/O_{4R}$ | L16 $I/O_{5R}$ |
| M1 $I/O_{32R}$ | M2 $I/O_{32L}$ | M3 $I/O_{31L}$ | M4 $V_{DDQR}$ | M5 $V_{DD}$ | M6 $V_{DD}$ | M7 $\overline{INT}_R$ | M8 $V_{SS}$ | M9 $V_{SS}$ | M10 $V_{SS}$ | M11 $V_{DD}$ | M12 $V_{DD}$ | M13 $V_{DDQL}$ | M14 $I/O_{3R}$ | M15 $I/O_{3L}$ | M16 $I/O_{4L}$ |
| N1 $I/O_{33L}$ | N2 $I/O_{34R}$ | N3 $I/O_{33R}$ | N4 $PIPE/\overline{FT}_R$ | N5 $V_{DDQR}$ | N6 $V_{DDQR}$ | N7 $V_{DDQL}$ | N8 $V_{DDQL}$ | N9 $V_{DDQR}$ | N10 $V_{DDQR}$ | N11 $V_{DDQL}$ | N12 $V_{DDQL}$ | N13 $V_{DD}$ | N14 $I/O_{2L}$ | N15 $I/O_{1R}$ | N16 $I/O_{2R}$ |
| P1 $I/O_{35R}$ | P2 $I/O_{34L}$ | P3 TMS | P4 $A_{16R}$ | P5 $A_{13R}$ | P6 $A_{10R}$ | P7 $A_{7R}$ | P8 $\overline{BE}_{1R}$ | P9 $\overline{BE}_{0R}$ | P10 $CLK_R$ | P11 $\overline{ADS}_R$ | P12 $A_{6R}$ | P13 $A_{3R}$ | P14 $I/O_{0L}$ | P15 $I/O_{0R}$ | P16 $I/O_{1L}$ |
| R1 $I/O_{35L}$ | R2 NC | R3 $\overline{TRST}$ | R4 $A_{18R}$ | R5 $A_{15R}$ | R6 $A_{12R}$ | R7 $A_{9R}$ | R8 $\overline{BE}_{3R}$ | R9 $\overline{CE}_{0R}$ | R10 $R/\overline{W}_R$ | R11 $\overline{REPEAT}_R$ | R12 $A_{4R}$ | R13 $A_{1R}$ | R14 $OPT_R$ | R15 NC | R16 NC |
| T1 NC | T2 TCK | T3 $A_{19R}$ | T4 $A_{17R}$ | T5 $A_{14R}$ | T6 $A_{11R}$ | T7 $A_{8R}$ | T8 $\overline{BE}_{2R}$ | T9 $CE_{1R}$ | T10 $\overline{OE}_R$ | T11 $\overline{CNTEN}_R$ | T12 $A_{5R}$ | T13 $A_{2R}$ | T14 $A_{0R}$ | T15 NC | T16 NC |

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**NOTES:**
1. All $V_{DD}$ pins must be connected to 2.5V power supply.
2. All $V_{DDQ}$ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to $V_{DD}$ (2.5V), and 2.5V if OPT pin for that port is set to $V_{SS}$ (0V).
3. All $V_{SS}$ pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.76mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.
7. BP-256 package thickness is 1.76mm nominal. This is thicker than the BC-256 package (1.40mm nominal) used for the lower density IDT dual-port products.

## Pin Names

| Left Port | Right Port | Names |
|---|---|---|
| $\overline{CE}_{0L}$, $CE_{1L}$ | $\overline{CE}_{0R}$, $CE_{1R}$ | Chip Enables (Input)[5] |
| R/$\overline{W}_L$ | R/$\overline{W}_R$ | Read/Write Enable (Input) |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable (Input) |
| $A_{0L}$ - $A_{19L}$ | $A_{0R}$ - $A_{19R}$ | Address (Input) |
| $I/O_{0L}$ - $I/O_{35L}$ | $I/O_{0R}$ - $I/O_{35R}$ | Data Input/Output |
| $CLK_L$ | $CLK_R$ | Clock (Input) |
| PL/$\overline{FT}_L$ | PL/$\overline{FT}_R$ | Pipeline/Flow-Through (Input) |
| $\overline{ADS}_L$ | $\overline{ADS}_R$ | Address Strobe Enable (Input) |
| $\overline{CNTEN}_L$ | $\overline{CNTEN}_R$ | Counter Enable (Input) |
| $\overline{REPEAT}_L$ | $\overline{REPEAT}_R$ | Counter Repeat[3] (Input) |
| $\overline{BE}_{0L}$ - $\overline{BE}_{3L}$ | $\overline{BE}_{0R}$ - $\overline{BE}_{3R}$ | Byte Enables (9-bit bytes) (Input)[5] |
| $V_{DDQL}$ | $V_{DDQR}$ | Power (I/O Bus) (3.3V or 2.5V)[1] (Input) |
| $OPT_L$ | $OPT_R$ | Option for selecting $V_{DDQX}$[1,2] (Input) |
| $ZZ_L$ | $ZZ_R$ | Sleep Mode pin[4] (Input) |
| $V_{DD}$ | | Power (2.5V)[1] (Input) |
| $V_{SS}$ | | Ground (0V) (Input) |
| TDI | | Test Data Input |
| TDO | | Test Data Output |
| TCK | | Test Logic Clock (10MHz) (Input) |
| TMS | | Test Mode Select (Input) |
| $\overline{TRST}$ | | Reset (Initialize TAP Controller) (Input) |
| $\overline{INT}_L$ | $\overline{INT}_R$ | Interrupt Flag (Output) |

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**NOTES:**
1. $V_{DD}$, $OPT_X$, and $V_{DDQX}$ must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
2. $OPT_X$ selects the operating voltage levels for the I/Os and controls on that port. If $OPT_X$ is set to $V_{DD}$ (2.5V), then that port's I/Os and controls will operate at 3.3V levels and $V_{DDQX}$ must be supplied at 3.3V. If $OPT_X$ is set to $V_{SS}$ (0V), then that port's I/Os and address controls will operate at 2.5V levels and $V_{DDQX}$ must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
3. When $\overline{REPEAT}_X$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}_X$.
4. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/$\overline{FT}_X$ and $OPT_X$ and the sleep mode pins themselves ($ZZ_X$) are not affected during sleep mode. It is recommended that boundary scan not be operated during sleep mode.
5. Chip Enables and Byte Enables are double buffered when PL/$\overline{FT}$ = $V_{IH}$, i.e., the signals take two cycles to deselect.

## Truth Table I—Read/Write and Enable Control (1,2,3,4)

| $\overline{OE}$ | CLK | $\overline{CE}_0$ | $CE_1$ | $\overline{BE}_3$ | $\overline{BE}_2$ | $\overline{BE}_1$ | $\overline{BE}_0$ | R/$\overline{W}$ | ZZ | Byte 3 $I/O_{27-35}$ | Byte 2 $I/O_{18-26}$ | Byte 1 $I/O_{9-17}$ | Byte 0 $I/O_{0-8}$ | MODE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | ↑ | H | L | X | X | X | X | X | L | High-Z | High-Z | High-Z | High-Z | Deselected–Power Down |
| X | ↑ | L | L | X | X | X | X | X | X | Active | Active | Active | Active | Not Allowed |
| X | ↑ | H | H | X | X | X | X | X | X | Active | Active | Active | Active | Not Allowed |
| X | ↑ | L | H | H | H | H | H | X | L | High-Z | High-Z | High-Z | High-Z | All Bytes Deselected |
| X | ↑ | L | H | H | H | H | L | L | L | High-Z | High-Z | High-Z | $D_{IN}$ | Write to Byte 0 Only |
| X | ↑ | L | H | H | H | L | H | L | L | High-Z | High-Z | $D_{IN}$ | High-Z | Write to Byte 1 Only |
| X | ↑ | L | H | H | L | H | H | L | L | High-Z | $D_{IN}$ | High-Z | High-Z | Write to Byte 2 Only |
| X | ↑ | L | H | L | H | H | H | L | L | $D_{IN}$ | High-Z | High-Z | High-Z | Write to Byte 3 Only |
| X | ↑ | L | H | H | H | L | L | L | L | High-Z | High-Z | $D_{IN}$ | $D_{IN}$ | Write to Lower 2 Bytes Only |
| X | ↑ | L | H | L | L | H | H | L | L | $D_{IN}$ | $D_{IN}$ | High-Z | High-Z | Write to Upper 2 bytes Only |
| X | ↑ | L | H | L | L | L | L | L | L | $D_{IN}$ | $D_{IN}$ | $D_{IN}$ | $D_{IN}$ | Write to All Bytes |
| L | ↑ | L | H | H | H | H | L | H | L | High-Z | High-Z | High-Z | $D_{OUT}$ | Read Byte 0 Only |
| L | ↑ | L | H | H | H | L | H | H | L | High-Z | High-Z | $D_{OUT}$ | High-Z | Read Byte 1 Only |
| L | ↑ | L | H | H | L | H | H | H | L | High-Z | $D_{OUT}$ | High-Z | High-Z | Read Byte 2 Only |
| L | ↑ | L | H | L | H | H | H | H | L | $D_{OUT}$ | High-Z | High-Z | High-Z | Read Byte 3 Only |
| L | ↑ | L | H | H | H | L | L | H | L | High-Z | High-Z | $D_{OUT}$ | $D_{OUT}$ | Read Lower 2 Bytes Only |
| L | ↑ | L | H | L | L | H | H | H | L | $D_{OUT}$ | $D_{OUT}$ | High-Z | High-Z | Read Upper 2 Bytes Only |
| L | ↑ | L | H | L | L | L | L | H | L | $D_{OUT}$ | $D_{OUT}$ | $D_{OUT}$ | $D_{OUT}$ | Read All Bytes |
| H | ↑ | X | X | X | X | X | X | X | L | High-Z | High-Z | High-Z | High-Z | Outputs Disabled |
| X | X | X | X | X | X | X | X | X | H | High-Z | High-Z | High-Z | High-Z | Sleep Mode |

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**NOTES:**
1. "H" = $V_{IH}$, "L" = $V_{IL}$, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = $V_{IH}$.
3. $\overline{OE}$ and ZZ are asynchronous input signals.
4. It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

## Truth Table II—Address Counter Control (1,2)

| Address | Previous Internal Address | Internal Address Used | CLK | $\overline{ADS}$ | $\overline{CNTEN}$ | $\overline{REPEAT}$(6) | I/O(3) | MODE |
|---|---|---|---|---|---|---|---|---|
| An | X | An | ↑ | L(4) | X | H | $D_{I/O}$ (n) | External Address Used |
| X | An | An + 1 | ↑ | H | L(5) | H | $D_{I/O}$(n+1) | Counter Enabled—Internal Address generation(7) |
| X | An + 1 | An + 1 | ↑ | H | H | H | $D_{I/O}$(n+1) | External Address Blocked—Counter disabled (An + 1 reused) |
| X | X | An | ↑ | X | X | L(4) | $D_{I/O}$(n) | Counter Set to last valid $\overline{ADS}$ load |

5682 tbl 03

**NOTES:**
1. "H" = $V_{IH}$, "L" = $V_{IL}$, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of R/$\overline{W}$, $\overline{CE}_0$, $CE_1$, $\overline{BE}$n and $\overline{OE}$.
3. Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{REPEAT}$ are independent of all other memory control signals including $\overline{CE}_0$, $CE_1$ and $\overline{BE}$n
5. The address counter advances if $\overline{CNTEN}$ = $V_{IL}$ on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, $CE_1$, $\overline{BE}$n.
6. When $\overline{REPEAT}$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}$. This value is not set at power-up: a known location should be loaded via $\overline{ADS}$ during initialization if desired. Any subsequent $\overline{ADS}$ access during operations will update the $\overline{REPEAT}$ address location.
7. Address $A_{19}$ must be managed as part of a full depth counter implementation using the IDT70T3509M. For physical addresses $00000_H$ through $7FFFF_H$ the value of a $A_{19}$ is 0, while for physical addresses $80000_H$ through $FFFFF_H$ the value of $A_{19}$ is 1. The user needs to keep track of the device counter and make sure that $A_{19}$ is actively driven from 0-to-1 or 1-to-0 and held as needed at the appropriate address boundaries for full depth counter operation and that $A_{19}$ is in the appropriate state when using the $\overline{REPEAT}$ function.

## Recommended Operating Temperature and Supply Voltage (1)

| Grade | Ambient Temperature | GND | $V_{DD}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 2.5V ± 100mV |
| Industrial | -40°C to +85°C | 0V | 2.5V ± 100mV |

5682 tbl 04

**NOTES:**
1. This is the parameter TA. This is the "instant on" case temperature.

## Recommended DC Operating Conditions with $V_{DDQ}$ at 2.5V

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | 2.4 | 2.5 | 2.6 | V |
| $V_{DDQ}$ | I/O Supply Voltage(3) | 2.4 | 2.5 | 2.6 | V |
| $V_{SS}$ | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Volltage (Address, Control & Data I/O Inputs)(3) | 1.7 | — | $V_{DDQ}$ + 100mV(2) | V |
| $V_{IH}$ | Input High Voltage – JTAG | 1.7 | — | $V_{DD}$ + 100mV(2) | V |
| $V_{IH}$ | Input High Voltage - ZZ, OPT, PIPE/$\overline{FT}$ | $V_{DD}$ - 0.2V | — | $V_{DD}$ + 100mV(2) | V |
| $V_{IL}$ | Input Low Voltage | -0.3(1) | — | 0.7 | V |
| $V_{IL}$ | Input Low Voltage - ZZ, OPT, PIPE/$\overline{FT}$ | -0.3(1) | — | 0.2 | V |

5682 tbl 05a

**NOTES:**
1. $V_{IL}$ (min.) = -1.0V for pulse width less than $t_{CYC}$/2 or 5ns, whichever is less.
2. $V_{IH}$ (max.) = $V_{DDQ}$ + 1.0V for pulse width less than $t_{CYC}$/2 or 5ns, whichever is less.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to $V_{ss}$(0V), and $V_{DDQX}$ for that port must be supplied as indicated above.

## Recommended DC Operating Conditions with $V_{DDQ}$ at 3.3V

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | 2.4 | 2.5 | 2.6 | V |
| $V_{DDQ}$ | I/O Supply Voltage(3) | 3.15 | 3.3 | 3.45 | V |
| $V_{SS}$ | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage (Address, Control &Data I/O Inputs)(3) | 2.0 | — | $V_{DDQ}$ + 150mV(2) | V |
| $V_{IH}$ | Input High Voltage – JTAG | 1.7 | — | $V_{DD}$ + 100mV(2) | V |
| $V_{IH}$ | Input High Voltage - ZZ, OPT, PIPE/$\overline{FT}$ | $V_{DD}$ - 0.2V | — | $V_{DD}$ + 100mV(2) | V |
| $V_{IL}$ | Input Low Voltage | -0.3(1) | — | 0.8 | V |
| $V_{IL}$ | Input Low Voltage - ZZ, OPT, PIPE/$\overline{FT}$ | -0.3(1) | — | 0.2 | V |

5682 tbl 05b

**NOTES:**
1. $V_{IL}$ (min.) = -1.0V for pulse width less than $t_{CYC}$/2, or 5ns, whichever is less.
2. $V_{IH}$ (max.) = $V_{DDQ}$ + 1.0V for pulse width less than $t_{CYC}$/2 or 5ns, whichever is less.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to $V_{DD}$ (2.5V), and $V_{DDQX}$ for that port must be supplied as indicated above.

## Absolute Maximum Ratings (1)

| Symbol | Rating | Com'l & Ind | Unit |
|---|---|---|---|
| $V_{TERM}$ ($V_{DD}$) | $V_{DD}$ Terminal Voltage with Respect to GND | -0.5 to 3.6 | V |
| $V_{TERM}$(2) ($V_{DDQ}$) | $V_{DDQ}$ Terminal Voltage with Respect to GND | -0.3 to $V_{DDQ}$ + 0.3 | V |
| $V_{TERM}$(2) (INPUTS and I/O's) | Input and I/O Terminal Voltage with Respect to GND | -0.3 to $V_{DDQ}$ + 0.3 | V |
| $T_{BIAS}$(3) | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $T_{JN}$ | Junction Temperature | +150 | °C |
| $I_{OUT}$(For $V_{DDQ}$ = 3.3V) | DC Output Current | 50 | mA |
| $I_{OUT}$(For $V_{DDQ}$ = 2.5V) | DC Output Current | 40 | mA |

5682 tbl 06

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed $V_{DDQ}$ during power supply ramp up.
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.

## Capacitance(1)

($T_A$ = +25°C, F = 1.0MHz) BGA ONLY

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 35 | pF |
| $C_{OUT}$(2) | Output Capacitance | $V_{OUT}$ = 0V | 35 | pF |

5682 tbl 07

**NOTES:**
1. These parameters are determined by device characterization, but are not production tested.
2. $C_{OUT}$ also references $C_{I/O}$.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD}$ = 2.5V ± 100mV)

| Symbol | Parameter | Test Conditions | 70T3509MS | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $\|I_{LI}\|$ | Input Leakage Current(1) | $V_{DDQ}$ = Max., $V_{IN}$ = 0V to $V_{DDQ}$ | — | 20 | µA |
| $\|I_{LI}\|$ | JTAG & ZZ Input Leakage Current(1,2) | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | 60 | µA |
| $\|I_{LO}\|$ | Output Leakage Current(1,3) | $\overline{CE}_0$ = $V_{IH}$ and $CE_1$ = $V_{IL}$, $V_{OUT}$ = 0V to $V_{DDQ}$ | — | 20 | µA |
| $V_{OL}$ (3.3V) | Output Low Voltage(1) | $I_{OL}$ = +4mA, $V_{DDQ}$ = Min. | — | 0.4 | V |
| $V_{OH}$ (3.3V) | Output High Voltage(1) | $I_{OH}$ = -4mA, $V_{DDQ}$ = Min. | 2.4 | — | V |
| $V_{OL}$ (2.5V) | Output Low Voltage(1) | $I_{OL}$ = +2mA, $V_{DDQ}$ = Min. | — | 0.4 | V |
| $V_{OH}$ (2.5V) | Output High Voltage(1) | $I_{OH}$ = -2mA, $V_{DDQ}$ = Min. | 2.0 | — | V |

5682 tbl 08

**NOTES:**
1. $V_{DDQ}$ is selectable (3.3V/2.5V) via OPT pins. Refer to p.5 for details.
2. Applicable only for TMS, TDI and $\overline{TRST}$ inputs.
3. Outputs tested in tri-state mode.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (3) ($V_{DD}$ = 2.5V ± 100mV)

| Symbol | Parameter | Test Condition | Version | | 70T3509MS133 Com'l & Ind Typ.(4) | 70T3509MS133 Com'l & Ind Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Dynamic Operating Current (Both Ports Active) | $\overline{CE}_L$ and $\overline{CE}_R$= $V_{IL}$, Outputs Disabled, f = $f_{MAX}$(1) | COM'L | S | 800 | 1120 | mA |
| | | | IND | S | 800 | 1370 | |
| $I_{SB1}$(6) | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L$ = $\overline{CE}_R$ = $V_{IH}$ f = $f_{MAX}$(1) | COM'L | S | 560 | 760 | mA |
| | | | IND | S | 560 | 940 | |
| $I_{SB2}$(6) | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}_{"A"}$ = $V_{IL}$ and $\overline{CE}_{"B"}$ = $V_{IH}$(5) Active Port Outputs Disabled, f=$f_{MAX}$(1) | COM'L | S | 680 | 880 | mA |
| | | | IND | S | 680 | 1090 | |
| $I_{SB3}$ | Full Standby Current (Both Ports - CMOS Level Inputs) | Both Ports $\overline{CE}_{0L}$ = $\overline{CE}_{0R}$ ≥ $V_{DD}$ - 0.2V and $CE_{1L}$ = $CE_{1R}$ ≤ 0.2V, $V_{IN}$ ≥ $V_{DDQ}$ - 0.2V or $V_{IN}$ ≤ 0.2V, f = 0(2) | COM'L | S | 20 | 60 | mA |
| | | | IND | S | 20 | 80 | |
| $I_{SB4}$(6) | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ $V_{DDQ}$ - 0.2V(5) $V_{IN}$ ≥ $V_{DDQ}$ - 0.2V or $V_{IN}$ ≤ 0.2V Active Port, Outputs Disabled, f = $f_{MAX}$(1) | COM'L | S | 680 | 880 | mA |
| | | | IND | S | 680 | 1090 | |
| $I_{ZZ}$ | Sleep Mode Current (Both Ports - TTL Level Inputs) | $ZZ_L$ = $ZZ_R$ = $V_{IH}$ f=$f_{MAX}$(1) | COM'L | S | 20 | 60 | mA |
| | | | IND | S | 20 | 80 | |

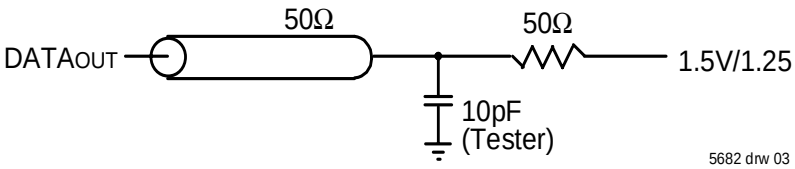
5682 tbl 09

**NOTES:**
1. At f = $f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/$t_{CYC}$, using "AC TEST CONDITIONS".
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. $V_{DD}$ = 2.5V, $T_A$ = 25°C for Typ, and are not production tested. $I_{DD\,DC}$(f=0) = 30mA (Typ).
5. $\overline{CE}_X$ = $V_{IL}$ means $\overline{CE}_{0X}$ = $V_{IL}$ and $CE_{1X}$ = $V_{IH}$ (enabled)
   $\overline{CE}_X$ = $V_{IH}$ means $\overline{CE}_{0X}$ = $V_{IH}$ and $CE_{1X}$ = $V_{IL}$ (disabled)
   $\overline{CE}_X$ ≤ 0.2V means $\overline{CE}_{0X}$ ≤ 0.2V and $CE_{1X}$ ≥ $V_{DD}$ - 0.2V (enabled - CMOS levels)
   $\overline{CE}_X$ ≥ $V_{DD}$ - 0.2V means $\overline{CE}_{0X}$ ≥ $V_{DD}$ - 0.2V and $CE_{1X}$ ≤ 0.2V (disabled - CMOS levels)
   "X" represents "L" for left port or "R" for right port.
6. $I_{SB1}$, $I_{SB2}$ and $I_{SB4}$ will all reach full standby levels ($I_{SB3}$) on the appropriate port(s) if $ZZ_L$ and/or $ZZ_R$ = $V_{IH}$.

## AC Test Conditions ($V_{DDQ}$ - 3.3V/2.5V)

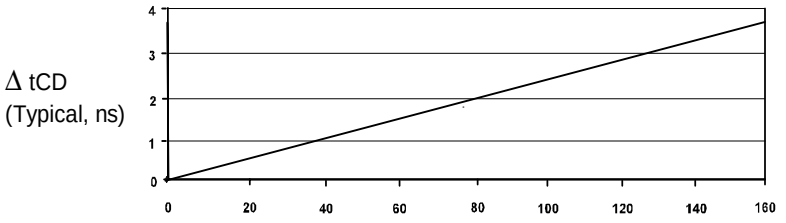
| | |
|---|---|
| Input Pulse Levels (Address & Controls) | GND to 3.0V/GND to 2.4V |
| Input Pulse Levels (I/Os) | GND to 3.0V/GND to 2.4V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | 1.5V/1.25V |
| Output Reference Levels | 1.5V/1.25V |
| Output Load | Figure 1 |

5682 tbl 10




5682 drw 03

**Figure 1. AC Output Test load.**




5682 drw 04

# AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) [2,3] ($V_{DD}$ = 2.5V ± 100mV, $T_A$ = 0°C to +70°C)

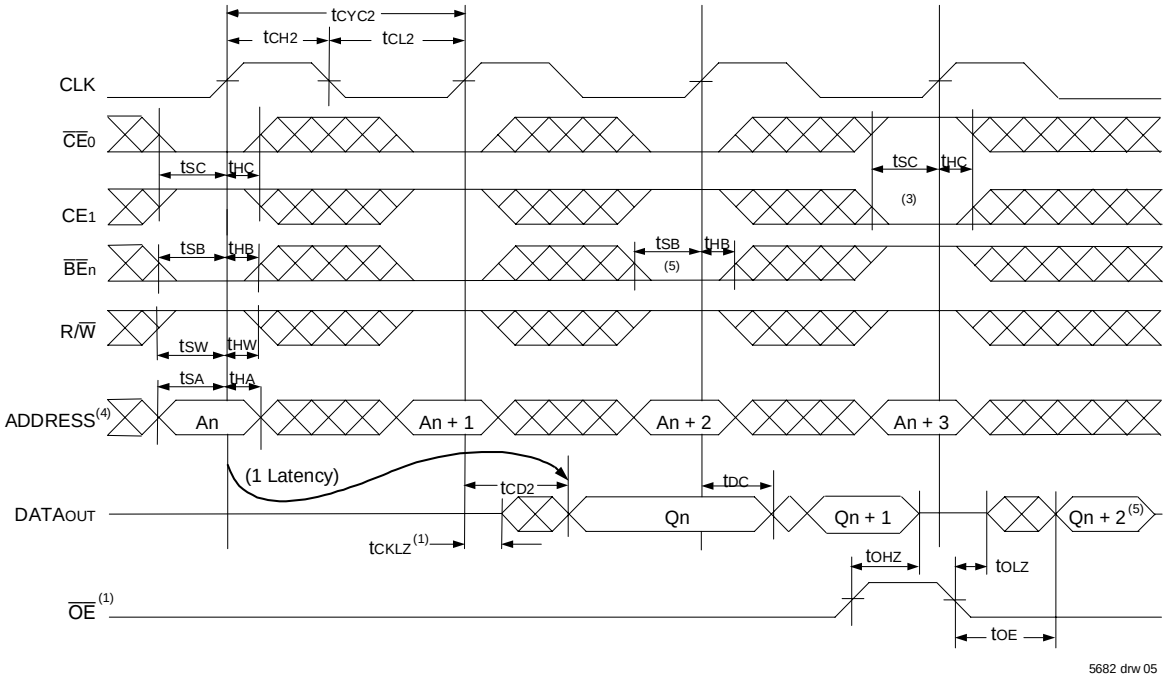
| | | 70T3509MS133 Com'l & Ind | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Unit** |
| $t_{CYC1}$ | Clock Cycle Time (Flow-Through)[1] | 25 | — | ns |
| $t_{CYC2}$ | Clock Cycle Time (Pipelined)[1] | 7.5 | — | ns |
| $t_{CH1}$ | Clock High Time (Flow-Through)[1] | 10 | — | ns |
| $t_{CL1}$ | Clock Low Time (Flow-Through)[1] | 10 | — | ns |
| $t_{CH2}$ | Clock High Time (Pipelined)[2] | 3 | — | ns |
| $t_{CL2}$ | Clock Low Time (Pipelined)[1] | 3 | — | ns |
| $t_{SA}$ | Address Setup Time | 1.8 | — | ns |
| $t_{HA}$ | Address Hold Time | 0.5 | — | ns |
| $t_{SC}$ | Chip Enable Setup Time | 1.8 | — | ns |
| $t_{HC}$ | Chip Enable Hold Time | 0.5 | — | ns |
| $t_{SB}$ | Byte Enable Setup Time | 1.8 | — | ns |
| $t_{HB}$ | Byte Enable Hold Time | 0.5 | — | ns |
| $t_{SW}$ | R/W Setup Time | 1.8 | — | ns |
| $t_{HW}$ | R/W Hold Time | 0.5 | — | ns |
| $t_{SD}$ | Input Data Setup Time | 1.8 | — | ns |
| $t_{HD}$ | Input Data Hold Time | 0.5 | — | ns |
| $t_{SAD}$ | $\overline{ADS}$ Setup Time | 1.8 | — | ns |
| $t_{HAD}$ | $\overline{ADS}$ Hold Time | 0.5 | — | ns |
| $t_{SCN}$ | $\overline{CNTEN}$ Setup Time | 1.8 | — | ns |
| $t_{HCN}$ | $\overline{CNTEN}$ Hold Time | 0.5 | — | ns |
| $t_{SRPT}$ | $\overline{REPEAT}$ Setup Time | 1.8 | — | ns |
| $t_{HRPT}$ | $\overline{REPEAT}$ Hold Time | 0.5 | — | ns |
| $t_{OE}$ | Output Enable to Data Valid | — | 4.6 | ns |
| $t_{OLZ}$[4] | Output Enable to Output Low-Z | 1 | — | ns |
| $t_{OHZ}$[4] | Output Enable to Output High-Z | 1 | 4.2 | ns |
| $t_{CD1}$ | Clock to Data Valid (Flow-Through)[1] | — | 15 | ns |
| $t_{CD2}$ | Clock to Data Valid (Pipelined)[1] | — | 4.2 | ns |
| $t_{DC}$ | Data Output Hold After Clock High | 1 | — | ns |
| $t_{CKHZ}$[4] | Clock High to Output High-Z | 1 | 4.2 | ns |
| $t_{CKLZ}$[4] | Clock High to Output Low-Z | 1 | — | ns |
| $t_{INS}$ | Interrupt Flag Set Time | — | 7 | ns |
| $t_{INR}$ | Interrupt Flag Reset Time | — | 7 | ns |
| $t_{COLS}$ | Collision Flag Set Time | — | 4.2 | ns |
| $t_{COLR}$ | Collision Flag Reset Time | — | 4.2 | ns |
| $t_{ZZSC}$ | Sleep Mode Set Cycles | 2 | — | cycles |
| $t_{ZZRC}$ | Sleep Mode Recovery Cycles | 3 | — | cycles |
| **Port-to-Port Delay** | | | | |
| $t_{CO}$ | Clock-to-Clock Offset | 6 | — | ns |

5682 tbl 11

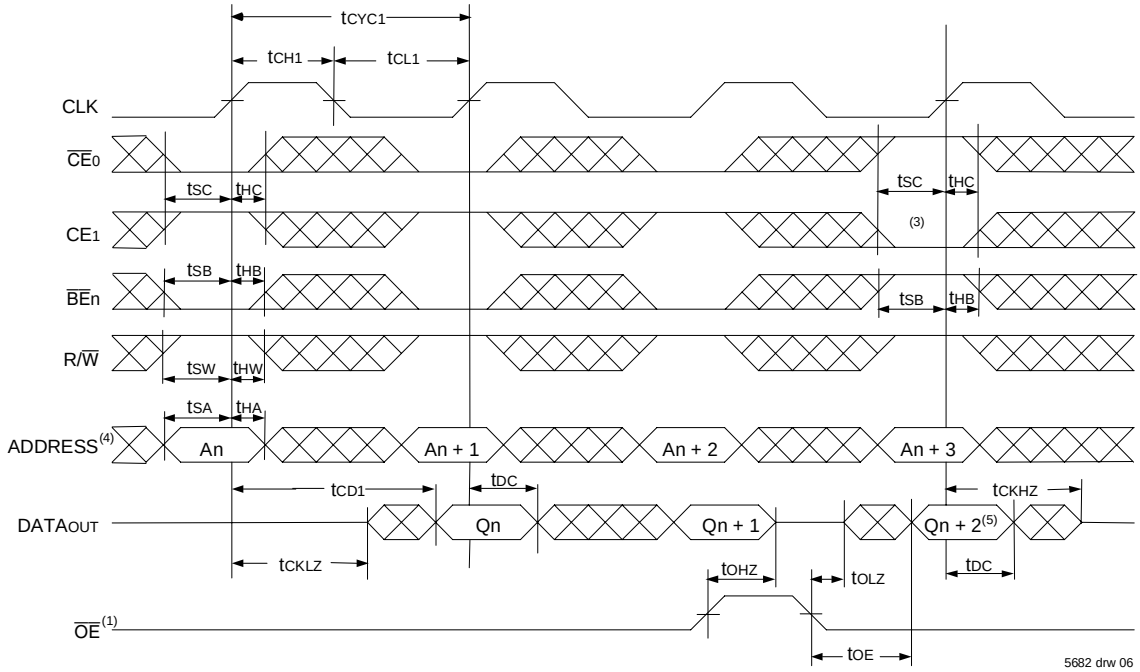
**NOTES:**

1. The Pipelined output parameters ($t_{CYC2}$, $t_{CD2}$) apply to either or both left and right ports when $\overline{FT}$/PIPE$_X$ = $V_{DD}$ (2.5V). Flow-through parameters ($t_{CYC1}$, $t_{CD1}$) apply when $\overline{FT}$/PIPE = $V_{SS}$ (0V) for that port.
2. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$), $\overline{FT}$/PIPE and OPT. $\overline{FT}$/PIPE and OPT should be treated as DC signals, i.e. steady state during operation.
3. These values are valid for either level of $V_{DDQ}$ (3.3V/2.5V). See page 6 for details on selecting the desired operating voltage levels for each port.
4. Guaranteed by design (not production tested).

## Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE'X' = $V_{IH}$)(1,2)



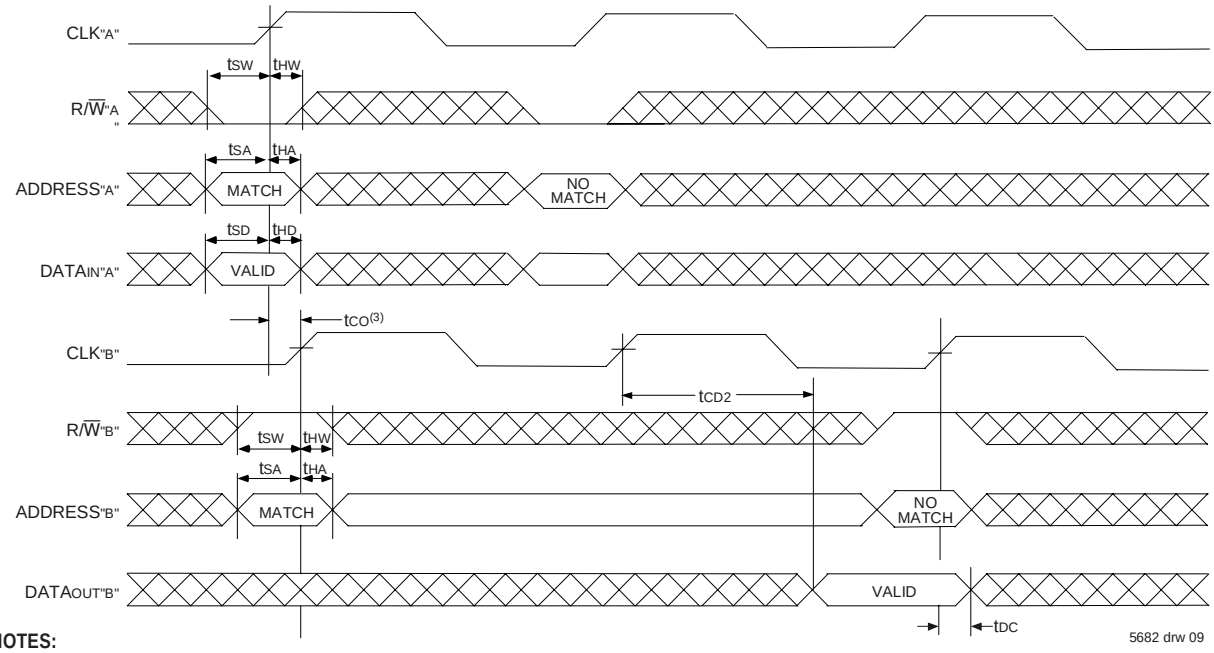

## Timing Waveform of Read Cycle for Flow-Through Output ($\overline{FT}$/PIPE"X" = $V_{IL}$)(1,2,6)




**NOTES:**

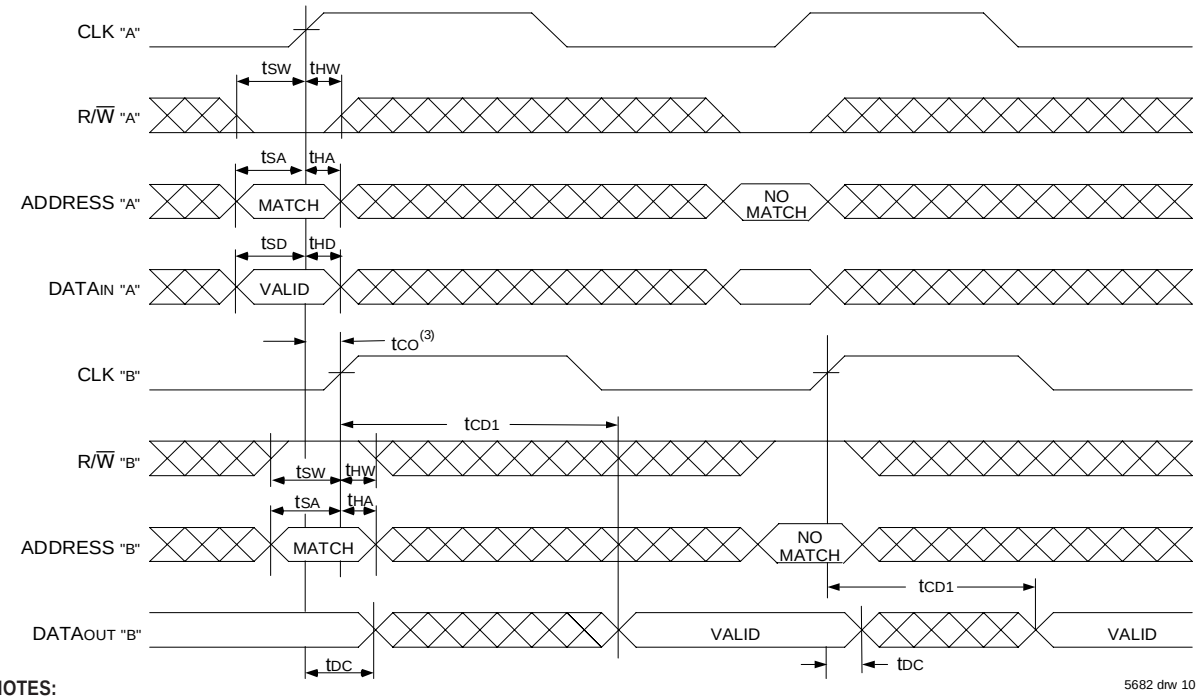
1. $\overline{OE}$ is asynchronously controlled; all other inputs depicted in the above waveforms are synchronous to the rising clock edge.
2. $\overline{ADS}$ = $V_{IL}$, $\overline{CNTEN}$ and $\overline{REPEAT}$ = $V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = $V_{IH}$, $CE_1$ = $V_{IL}$, $\overline{BE}_n$ = $V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{BE}_n$ was HIGH, then the appropriate Byte of $DATA_{OUT}$ for Qn + 2 would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

## Timing Waveform of Left Port Write to Pipelined Right Port Read(1,2,4)



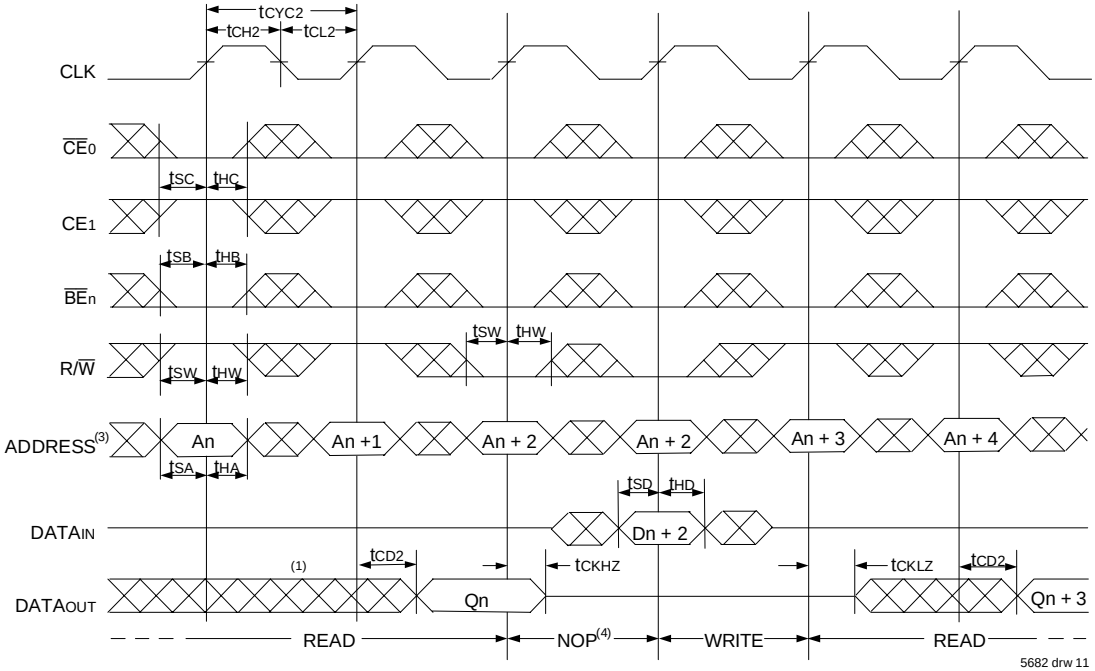

**NOTES:**
1. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS}$ = $V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{REPEAT}$ = $V_{IH}$.
2. $\overline{OE}$ = $V_{IL}$ for Port "B", which is being read from. $\overline{OE}$ = $V_{IH}$ for Port "A", which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2\ t_{CYC2} + t_{CD2}$). If $t_{CO}$ > minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

## Timing Waveform with Port-to-Port Flow-Through Read(1,2,4)




**NOTES:**
1. $\overline{CE}_0$, $\overline{BE}$n, and $\overline{ADS}$ = $V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{REPEAT}$ = $V_{IH}$.
2. $\overline{OE}$ = $V_{IL}$ for the Right Port, which is being read from. $\overline{OE}$ = $V_{IH}$ for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CYC} + t_{CD1}$). If $t_{CO}$ > minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CD1}$).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

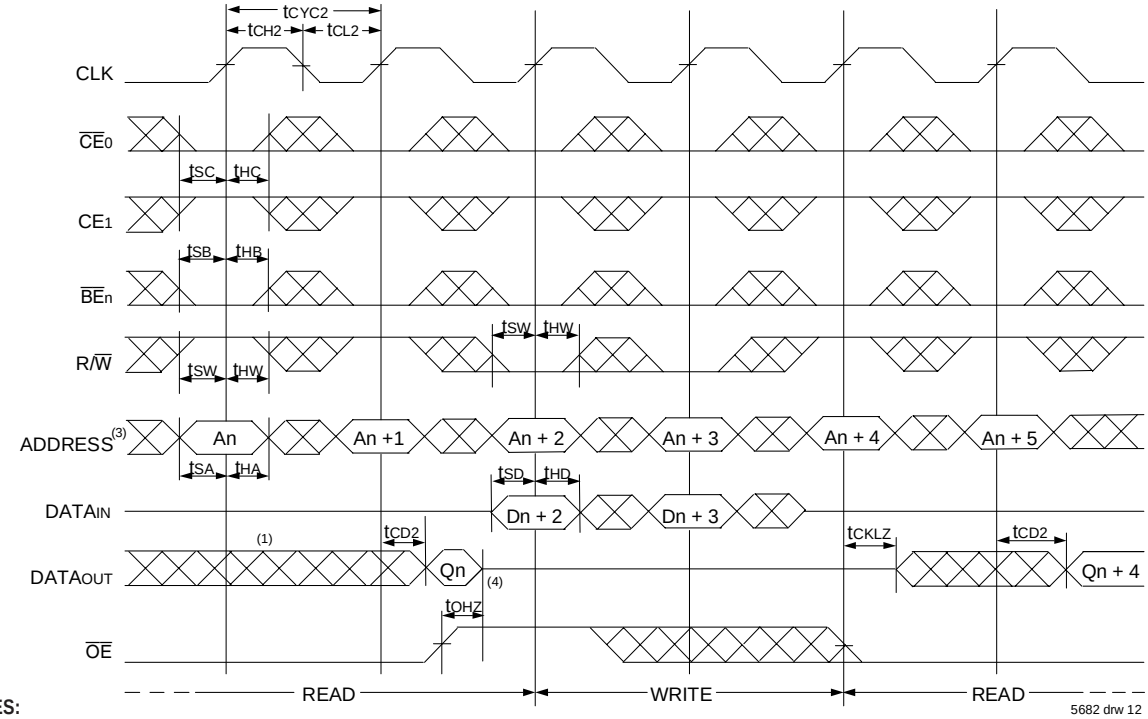
## Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)(2)




**NOTES:**

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

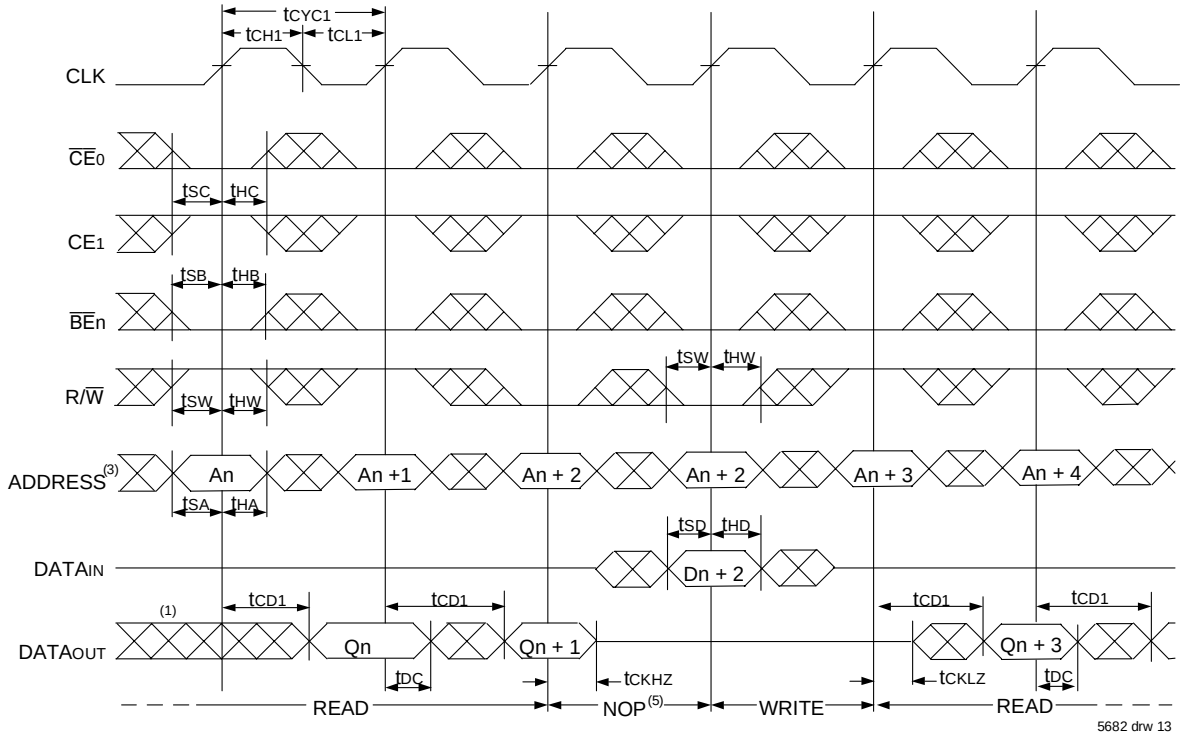
## Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(2)



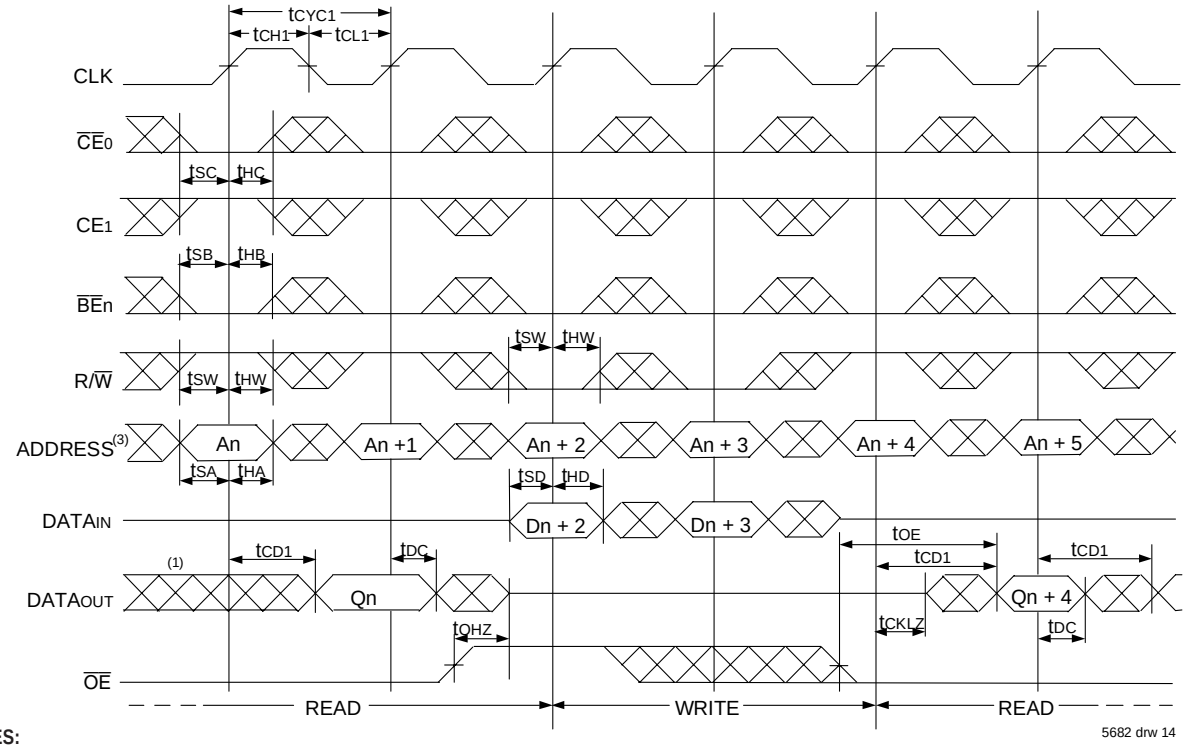

**NOTES:**

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

## Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = VIL)(2)



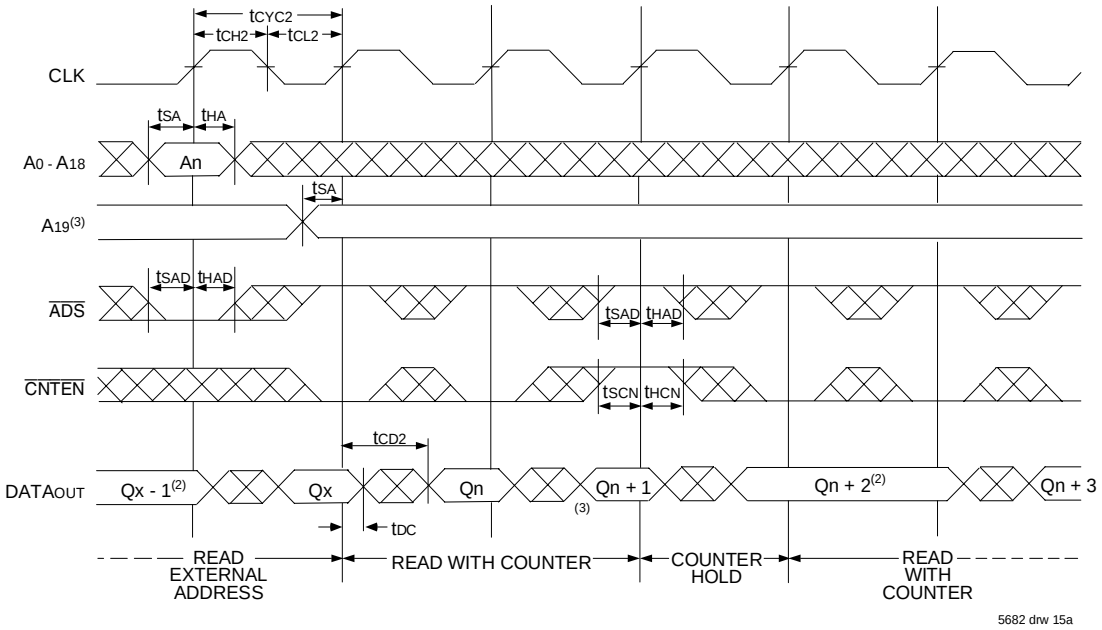

## Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)(2)



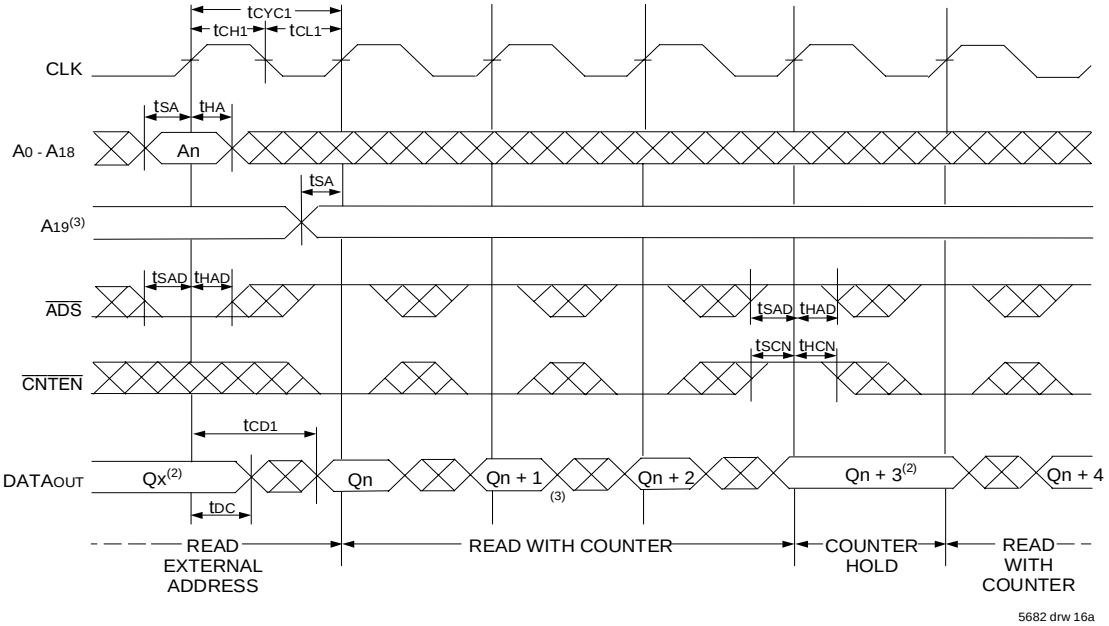

**NOTES:**

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE}n$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

## Timing Waveform of Pipelined Read with Address Counter Advance(1)



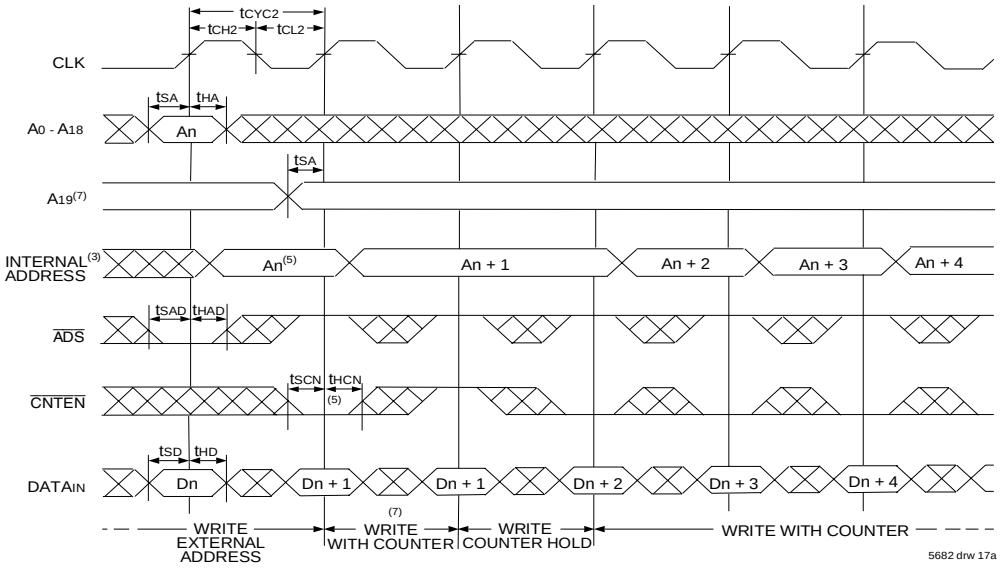

## Timing Waveform of Flow-Through Read with Address Counter Advance(1)



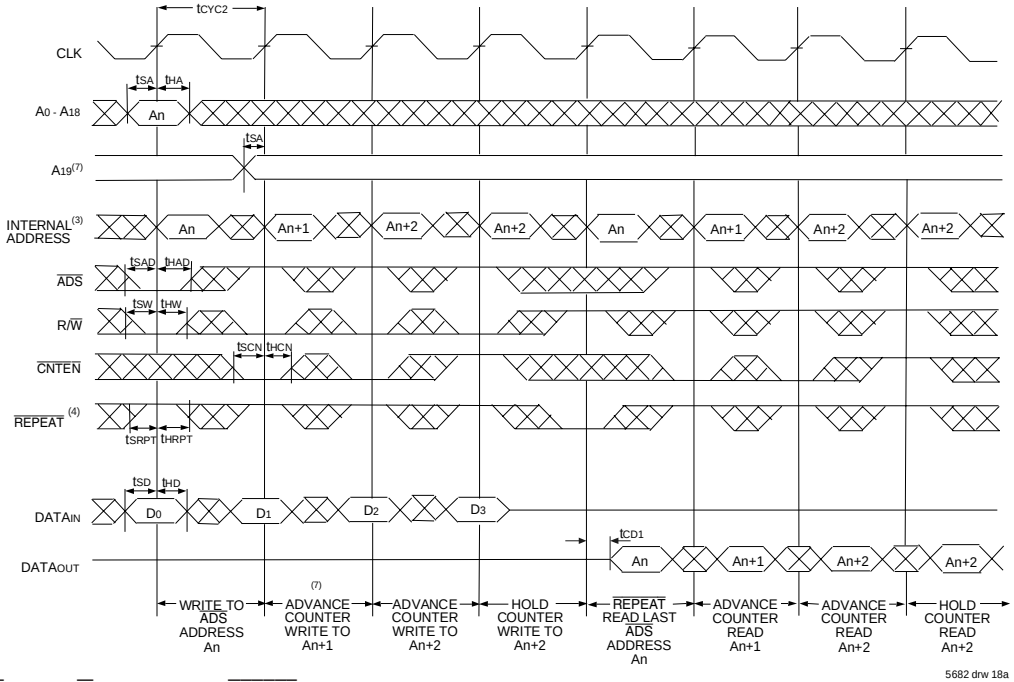

**NOTES:**

1. $\overline{CE_0}$, $\overline{OE}$, $\overline{BE}n$ = $V_{IL}$; $CE_1$, R/$\overline{W}$, and $\overline{REPEAT}$ = $V_{IH}$.
2. If there is no address change via $\overline{ADS}$ = $V_{IL}$ (loading a new address) or $\overline{CNTEN}$ = $V_{IL}$ (advancing the address), i.e. $\overline{ADS}$ = $V_{IH}$ and $\overline{CNTEN}$ = $V_{IH}$, then the data remains constant for subsequent clocks.
3. Address $A_{19}$ must be managed as part of a full depth counter implementation using the IDT70T3509M. For physical addresses 00000H through 7FFFFH the value of a $A_{19}$ is 0, while for physical addresses 80000H through FFFFFH the value of $A_{19}$ is 1. The user needs to keep track of the device counter and make sure that $A_{19}$ is actively driven from 0-to-1 or 1-to-0 and held as needed at the appropriate address boundaries for full depth counter operation. As shown this transition reflects An = 7FFFFH or FFFFFH.

## Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)(1)



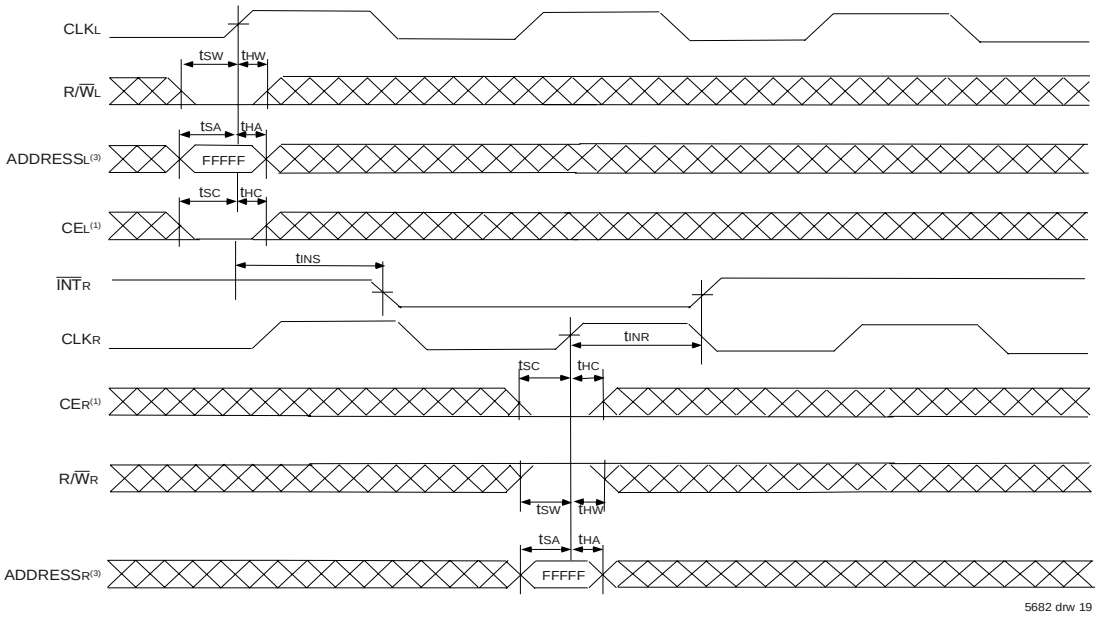

## Timing Waveform of Counter Repeat(2,6)




**NOTES:**

1. $\overline{CE_0}$, $\overline{BE_n}$, and R/$\overline{W}$ = $V_{IL}$; $CE_1$ and $\overline{REPEAT}$ = $V_{IH}$.
2. $\overline{CE_0}$, $\overline{BE_n}$ = $V_{IL}$; $CE_1$ = $V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = $V_{IL}$ and equals the counter output when $\overline{ADS}$ = $V_{IH}$.
4. No dead cycle exists during $\overline{REPEAT}$ operation. A READ or WRITE cycle may be coincidental with the counter $\overline{REPEAT}$ cycle: Address loaded by last valid $\overline{ADS}$ load will be accessed. For more information on $\overline{REPEAT}$ function refer to Truth Table II. $A_{19}$ must be in the appropriate state when using the REPEAT function to guarantee the correct address location is loaded.
5. $\overline{CNTEN}$ = $V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.
6. For Pipelined Mode user should add 1 cycle latency for outputs as per timing waveform of read cycle for pipelined operations.
7. Address $A_{19}$ must be managed as part of a full depth counter implementation using the IDT70T3509M. For physical addresses 00000H through 7FFFFH the value of a $A_{19}$ is 0, while for physical addresses 80000H through FFFFFH the value of $A_{19}$ is 1. The user needs to keep track of the device counter and make sure that $A_{19}$ is actively driven from 0-to-1 or 1-to-0 and held as needed at the appropriate address boundaries for full depth counter operation. As shown this transition reflects An = 7FFFFH or FFFFFH.

## Waveform of Interrupt Timing(2)

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**NOTES:**
1. $\overline{CE}_0$ = $V_{IL}$ and $CE_1$ = $V_{IH}$.
2. All timing is the same for Left and Right ports.
3. Address is for internal register, not the external bus, i.e. address needs to be qualified by one of the Address counter control signals.

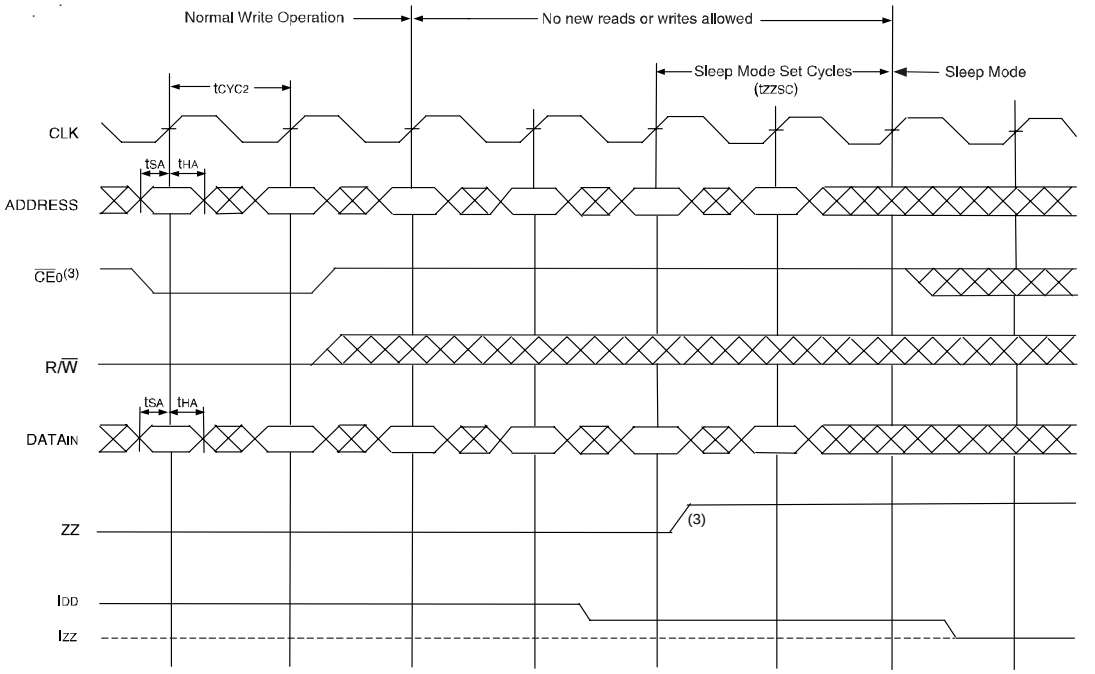
## Truth Table III - Interrupt Flag(1)

| Left Port | | | | | Right Port | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| CLKL | R/$\overline{W}$L(2) | CEL(2) | A19L-A0L | $\overline{INT}$L | CLKR | R/$\overline{W}$R(2) | CER(2) | A19R-A0R | $\overline{INT}$R | Function |
| ↑ | L | L | FFFFF | X | ↑ | X | X | X | L | Set Right $\overline{INT}$R Flag |
| ↑ | X | X | X | X | ↑ | H | L | FFFFF | H | Reset Right $\overline{INT}$R Flag |
| ↑ | X | X | X | L | ↑ | L | L | FFFFE | X | Set Left $\overline{INT}$L Flag |
| ↑ | H | L | FFFFE | H | ↑ | X | X | X | X | Reset Left $\overline{INT}$L Flag |

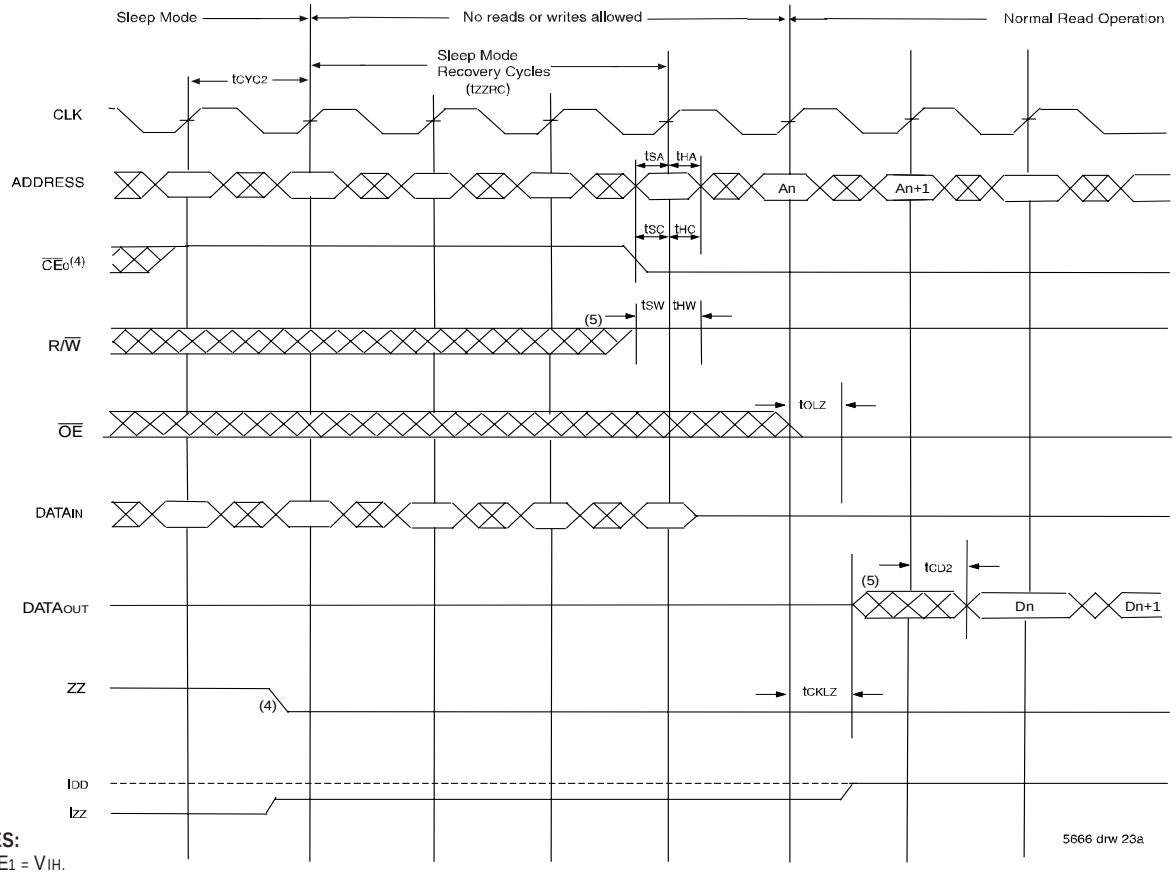
5682 tbl 12

**NOTES:**
1. $\overline{INT}_L$ and $\overline{INT}_R$ must be initialized at power-up by Resetting the flags.
2. $\overline{CE}_0$ = $V_{IL}$ and $CE_1$ = $V_{IH}$, R/$\overline{W}$ and CE are synchronous with respect to the clock and need valid set-up and hold times.
3. Address is for internal register, not the external bus, i.e. address needs to be qualified by one of the Address counter control signals.

## Timing Waveform - Entering Sleep Mode (1,2)




## Timing Waveform - Exiting Sleep Mode (1,2)




**NOTES:**
1. CE1 = VIH.
2. All timing is same for Left and Right ports.
3. $\overline{CE}_0$ has to be deactivated ($\overline{CE}_0$ = VIH) three cycles prior to asserting ZZ (ZZx = VIH) and held for two cycles after asserting ZZ (ZZx = VIH).
4. $\overline{CE}_0$ has to be deactivated ($\overline{CE}_0$ = VIH) one cycle prior to de-asserting ZZ (ZZx = VIL) and held for three cycles after de-asserting ZZ (ZZx = VIL).
5. The device must be in Read Mode (R/$\overline{W}$ High) when exiting sleep mode. Outputs are active but data is not valid until the following cycle.

## Functional Description

The IDT70T3509M provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse width is independent of the cycle time.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

The combination of a HIGH on $\overline{CE}_0$ and a LOW on $CE_1$ for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70T3509Ms for depth expansion configurations. Two cycles are required with $\overline{CE}_0$ LOW and $CE_1$ HIGH to re-activate the outputs.

## Width Expansion

The IDT70T3509M can be used in applications requiring expanded width. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

## Sleep Mode

The IDT70T3509M is equipped with an optional sleep or low power mode on both ports. The sleep mode pin on both ports is asynchronous and active high. During normal operation, the ZZ pin is pulled low. When ZZ is pulled high, the port will enter sleep mode where it will meet lowest possible power conditions. The sleep mode timing diagram shows the modes of operation: Normal Operation, No Read/Write Allowed and Sleep Mode.

For normal operation all inputs must meet setup and hold times prior to sleep and after recovering from sleep. Clocks must also meet cycle high and low times during these periods. Three cycles prior to asserting ZZ ($ZZx = V_{IH}$) and three cycles after de-asserting ZZ ($ZZx = V_{IL}$), the device must be disabled via the chip enable pins. If a write or read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM cannot be guaranteed immediately after ZZ is asserted (prior to being in sleep). When exiting sleep mode, the device must be in Read mode ($R/\overline{W}x = V_{IH}$)when chip enable is asserted, and the chip enable must be valid for one full cycle before a read will result in the output of valid data.

During sleep mode the RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current ($I_{ZZ}$). All outputs will remain in high-Z state while in sleep mode. All inputs are allowed to toggle. The RAM will not be selected and will not perform any reads or writes.

## JTAG Functionality and Configuration

The IDT70T3509M is composed of four independent memory arrays, and thus cannot be treated as a single JTAG device in the scan chain. The four arrays (A, B, C and D) each have identical characteristics and commands but must be treated as separate entities in JTAG operations. Please refer to Figure 2.

JTAG signaling must be provided serially to each array and utilize the information provided in the Identification Register Definitions, Scan Register Sizes, and System Interface Parameter tables. Specifically, all serial commands must be issued to the IDT70T3509M in the following sequence: Array D, Array C, Array B, Array A. Please reference Application Note AN-411, "JTAG Testing of Multichip Modules" for specific instructions on performing JTAG testing on the IDT70T3509M. AN-411 is available at www.idt.com.

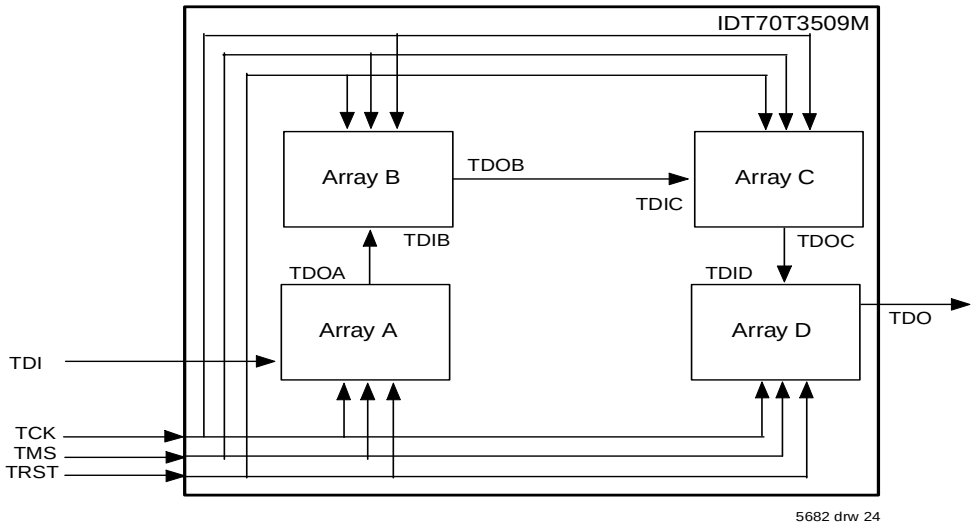



**Figure 2. JTAG Configuration for IDT70T3509M**

## JTAG Timing Specifications

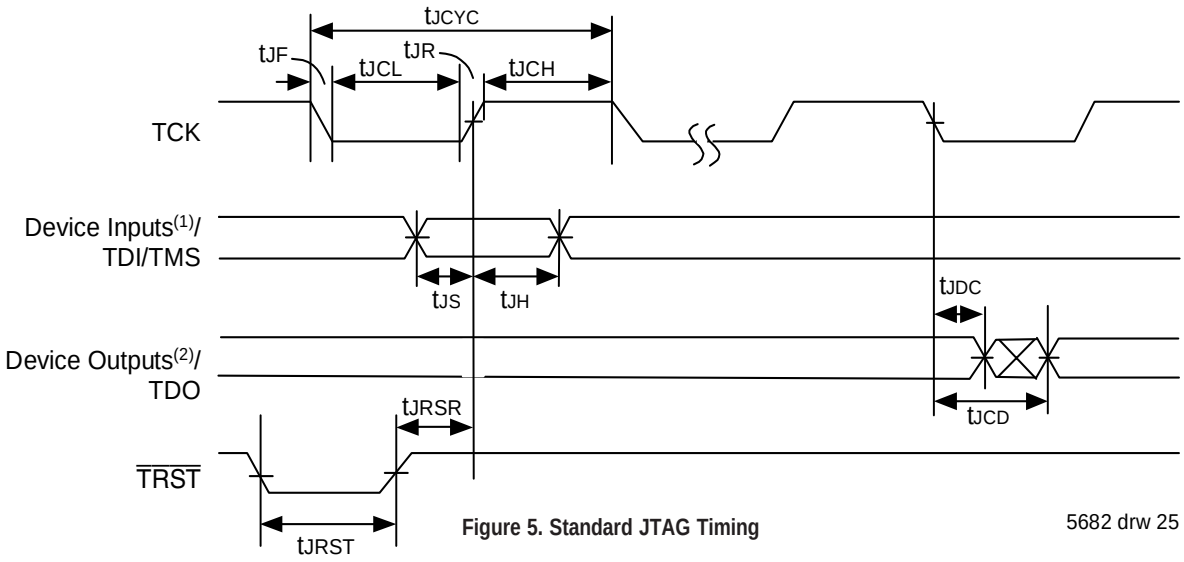



**Figure 5. Standard JTAG Timing**

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**NOTES:**
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

## JTAG AC Electrical Characteristics (1,2,3,4)

| Symbol | Parameter | 70T3509M | | |
|---|---|---|---|---|
| | | Min. | Max. | Units |
| tJCYC | JTAG Clock Input Period | 100 | — | ns |
| tJCH | JTAG Clock HIGH | 40 | — | ns |
| tJCL | JTAG Clock Low | 40 | — | ns |
| tJR | JTAG Clock Rise Time | — | 3(1) | ns |
| tJF | JTAG Clock Fall Time | — | 3(1) | ns |
| tJRST | JTAG Reset | 50 | — | ns |
| tJRSR | JTAG Reset Recovery | 50 | — | ns |
| tJCD | JTAG Data Output | — | 25 | ns |
| tJDC | JTAG Data Output Hold | 0 | — | ns |
| tJS | JTAG Setup | 15 | — | ns |
| tJH | JTAG Hold | 15 | — | ns |

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**NOTES:**
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

## Identification Register Definitions

| Instruction Field Array D | Value Array D | Instruction Field Array C | Value Array C | Instruction Field Array B | Value Array B | Instruction Field Array A | Value Array A | Description |
|---|---|---|---|---|---|---|---|---|
| Revision Number (31:28) | 0x0 | Revision Number (63:60) | 0x0 | Revision Number (95:92) | 0x0 | Revision Number (127:124) | 0x0 | Reserved for Version number |
| IDT Device ID (27:12) | 0x333 | IDT Device ID (59:44) | 0x333 | IDT Device ID (91:76) | 0x333 | IDT Device ID (123:108) | 0x333 | Defines IDT Part number |
| IDT JEDEC ID (11:1) | 0x33 | IDT JEDEC ID (43:33) | 0x33 | IDT JEDEC ID (75:65) | 0x33 | IDT JEDEC ID (107:97) | 0x33 | Allows unique identification of device vendor as IDT |
| ID Register Indicator Bit (Bit 0) | 1 | ID Register Indicator Bit (Bit 32) | 1 | ID Register Indicator Bit (Bit 64) | 1 | ID Register Indicator Bit (Bit 96) | 1 | Indicates the presence of an ID Register |

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## Scan Register Sizes

| Register Name | Bit Size Array A | Bit Size Array B | Bit Size Array C | Bit Size Array D | Bit Size 70T3509M |
|---|---|---|---|---|---|
| Instruction (IR) | 4 | 4 | 4 | 4 | 16 |
| Bypass (BYR) | 1 | 1 | 1 | 1 | 4 |
| Identification (IDR) | 32 | 32 | 32 | 32 | 128 |
| Boundary Scan (BSR) | Note (3) | Note (3) | Note (3) | Note (3) | Note (3) |

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## System Interface Parameters

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 0000000000000000 | Forces contents of the boundary scan cells onto the device outputs[1]. Places the boundary scan register (BSR) between TDI and TDO. |
| BYPASS | 1111111111111111 | Places the bypass register (BYR) between TDI and TDO. |
| IDCODE | 0010001000100010 | Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO. |
| HIGHZ | 0100010001000100 | Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers except $\overline{INT}$x to a High-Z state. |
| CLAMP | 0011001100110011 | Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO. |
| SAMPLE/PRELOAD | 0001000100010001 | Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs[2] to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI. |
| RESERVED | 0101010101010101, 0111011101110111, 1000100010001000, 1001100110011001, 1010101010101010, 1011101110111011, 1100110011001100 | Several combinations are reserved. Do not use codes other than those identified above. |
| PRIVATE | 0110011001100110,1110111011101110, 1101110111011101 | For internal use only. |

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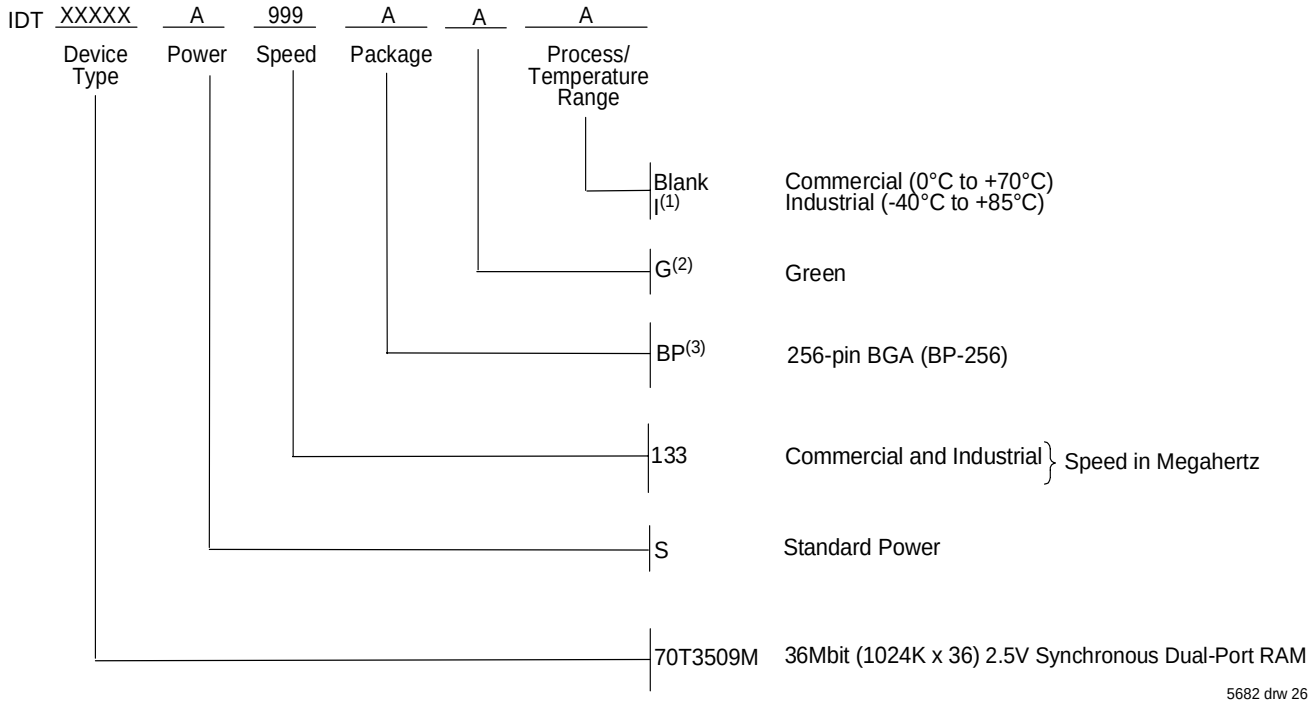
**NOTES:**
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{TRST}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

## Ordering Information




**NOTES:**

1. Contact your local sales office for Industrial temp range in other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.
3. BP-256 package thickness is 1.76mm nominal. This is thicker than the BC-256 package (1.40mm nominal) used for the lower density IDT dual-port products.

## Datasheet Document History:

| | |
|---|---|
| 11/09/04: | Initial Public Release of Preliminary Datasheet |
| 03/24/05: | Page 1 Added I-temp offering to features |
| | Page 6 Added I-temp information to the Recommended Operating Temperature and Supply Voltage table |
| | Page 8 Added I-temp values to the DC Electrical Characteristics table |
| | Page 10 Added I-temp to the heading of the AC Electrical Characteristics table |
| | Page 23 Added I-temp to ordering information |
| | Page 1 Added green availability to features |
| | Page 1 - 23 Removed Preliminary status |
| 06/14/05: | Page 1 Added feature to highlight footprint compatibility |
| | Page 3 & 23 Added a footnote to highlight package thickness of BP-256 vs. BC-256 |
| 08/27/07: | Page 1 Functional Block Diagram changed to correct chip enable logic and added footnote 2 referencing Truth Table I |

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