SPI EXCHANGE
2 x SPI-3 TO SPI-4

PRODUCT BRIEF
IDT88P8342

FEATURES

- **Functionality**
  - *Low speed to high speed SPI exchange device*
  - *Logical port (LP) mapping (SPI-3 <-> SPI-4) tables per direction*
  - *Per LP configurable memory allocation*
  - *Maskable interrupts for fatal errors*
  - *Fragment and burst length configurable per interface: min 16 bytes, max 256 bytes*
- **Standard Interfaces**
  - *Two OIF SPI-3: 8 or 32 bit, 19.44-133 MHz, 256 address range, 64 concurrently active LPs per interface*
  - *One OIF SPI-4 phase 2: 80 - 400 MHz, 256 address range, 128 concurrently active LPs*
  - *SPI-4 FIFO status channel options:*
    - *LVDS full-rate*
    - *LVTTL quarter-rate*
  - *Compatible with Network Processor Streaming Interface (NPSI) NPE-Framer mode of operation*
  - *SPI-4 ingress LVDS automatic bit alignment and lane de-skew over the entire frequency range*
  - *SPI-4 egress LVDS programmable lane pre-skew 0.1UI to 0.3UI*
  - *IEEE 1149.1 JTAG*
  - *Serial or parallel microprocessor interface for control and monitoring*
- **Full Suite of Performance Monitoring Counters**
  - *Number of packets*
  - *Number of fragments*
  - *Number of errors*
  - *Number of bytes*

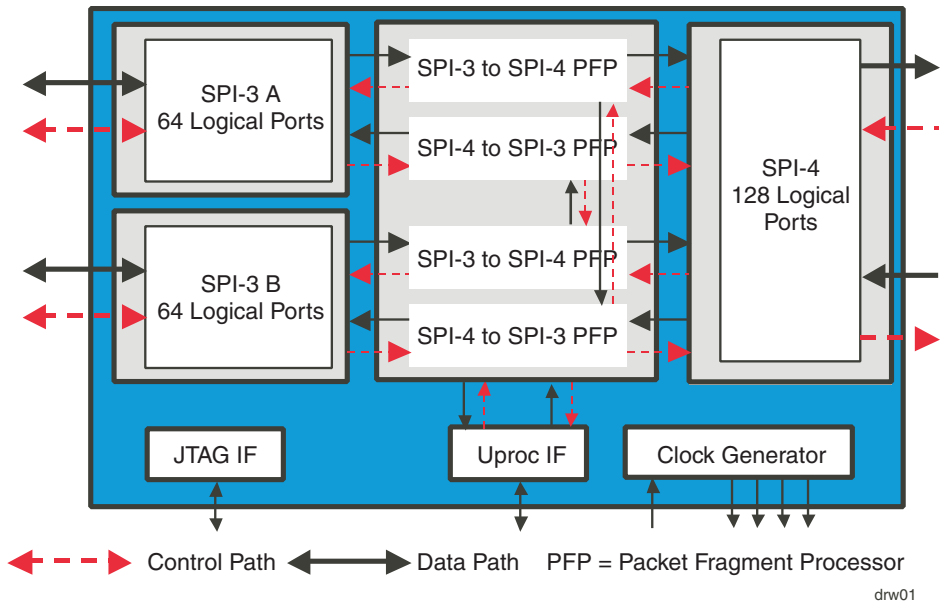
APPLICATIONS

- **Ethernet transport**
- **SONET / SDH packet transport line cards**
- **Broadband aggregation**
- **Multi-service switches**
- **IP services equipment**

DESCRIPTION

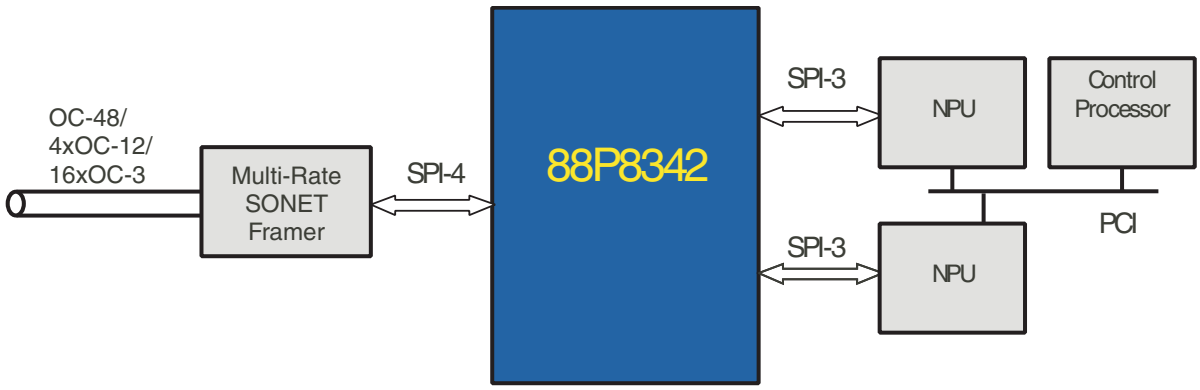
The IDT88P8342 is a SPI (System Packet Interface) Exchange with two SPI-3 interfaces and one SPI-4 interface. The data that enter on the low speed interface (SPI-3) are mapped to logical identifiers (LIDs) and enqueued for transmission over the high speed interface (SPI-4). The data that enter on the high speed interface (SPI-4) are mapped to logical identifiers (LIDs) and enqueued for transmission over a low speed interface (SPI-3). A data flow between SPI-3 and SPI-4 interfaces is accomplished with LID maps. The logical port addresses and number of entries in the LID maps may be dynamically configured. Various parameters of a data flow may be configured by the user such as buffer memory size and watermarks. In a typical application, the IDT88P8342 enables connection of two SPI-3 devices to a SPI-4 network processor. In other applications a SPI-3 or SPI-4 device may be connected to a SPI-3 network processor or traffic manager.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION

Exchange between optical ports and two NPU/Traffic Managers



INTRODUCTION

The IDT88P8342 device is a dual SPI-3 to single SPI-4 exchange intended for use in optical line cards, Ethernet transport, and multi-service switches. The SPI-3 and SPI-4 interfaces are defined by the Optical Interworking Forum.

The device can be used as a rate adapter, a switch, or an aggregation device between network processor units, multi-gigabit framers and PHYs, and switch fabric interface devices.

DATA PATH OVERVIEW

Figure 1. *Data Path Diagram* shows an overview of the data path through the device.

In normal operation, there are two paths through the IDT88P8342 device: the dual SPI-3 ingress to SPI-4 egress path, and the SPI-4 ingress to dual SPI-3 egress path. SPI-3 and SPI-4 burst sizes are separately configurable.

In the SPI-3 ingress to SPI-4 egress path, data enter in fragments on the SPI-3 interface and are received by the SPI-3 interface block. The fragments are mapped to a SPI-4 address and stored in memory allocated at the SPI-3 level until such a time that the Packet Fragment Processor determines that they are to be transmitted on the SPI-4 interface. The data is transferred in bursts, in line with the OIF SPI-4 implementation agreement, to the SPI-4 interface block, and are transmitted on the SPI-4 interface.

In the SPI-4 ingress to SPI-3 egress path, data enter in bursts on the SPI-4 interface and are received by the SPI-4 interface block. The SPI-4 address is translated to a SPI-3 address, and the data contained in the bursts are stored in memory allocated at the SPI-3 level until such a time that the Packet Fragment Processor determines that they are to be transmitted on the SPI-3 interface. The data is transferred in packet fragments, in line with the OIF SPI-3 implementation agreement, to the SPI-3 interface block, and are transmitted on the SPI-3 interface.

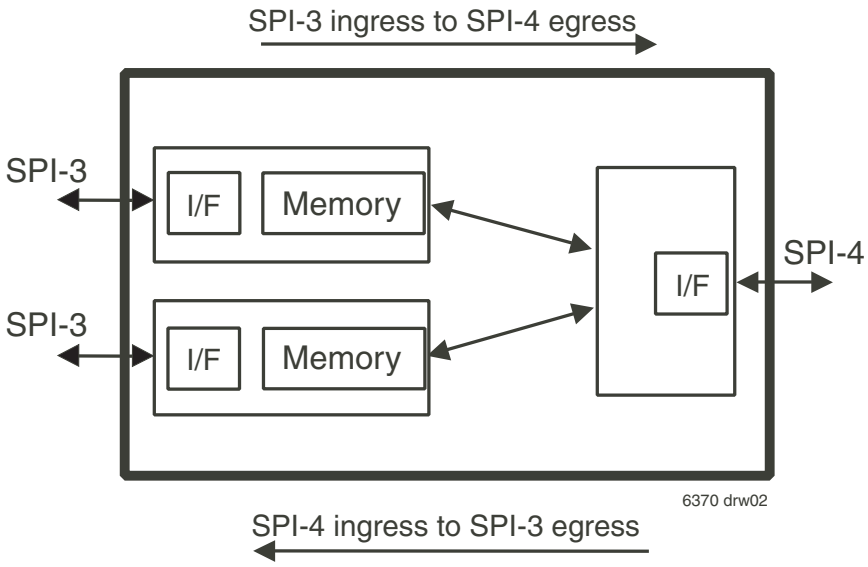


Figure 1. Data Path Diagram

EXTERNAL INTERFACES

The external interfaces provided on the IDT88P8342 device are two SPI-3 interfaces, one SPI-4 interface, a serial or parallel microprocessor interface, a JTAG interface, and a set of GPIO pins. Each of the interfaces is defined in the relevant standard.

The following information contains a set of the highlights of the features supported from the relevant standards, and a description of additional features implemented to enhance the usability of these interfaces for the system architect.

SPI-3

Refer to OIF SPI-3 document for full details of the implementation agreement.

- Two instantiations of SPI-3 interface; each interface independently configurable
- Device supports a 8-bit and 32-bit data bus structure.
- Clock rate is minimum 19.44 - to maximum 133 MHz
- Link, single port PHY and multi port PHY modes supported
- Master and slave modes supported
- Byte level and packet level transfer control mechanisms supported
  - 4 DTPA signals supported, mapped to LP addresses 0 – 3
  - 8 ADR signals supported
- Address range 0 – 255 with support for 64 simultaneously active logical ports
- Fragment length (section) configurable from 16 – 256 bytes in 16 byte multiples
- Configurable standard and non-standard bit and byte ordering

SPI-4

Refer to OIF SPI-4 phase 2 (OIF-SPI4-02.0) implementation agreement for full details of the implementation agreement.

- One instantiation of SPI-4 interface
- Clock rate is 80 - 400 MHz (160 — 800MHz DDR)
- Link and PHY modes supported
- Address range 0 – 255 with support for 128 simultaneously active logical ports
- MAXBURST parameters configurable 16-256 bytes in 16 byte multiples
- 256 entry calendar
- LVTTL and LVDS status signals supported

MICROPROCESSOR INTERFACE

- Parallel microprocessor interface
  - 8 bit data bus for parallel operation
  - Byte access
  - Direct accessed space
  - Indirect access space is used for most registers
  - Read operations to a reserved address or reserved bit fields return 0.
  - Write operations to reserved addresses or bit fields are ignored.
- Serial microprocessor interface
  - Compliance to Motorola serial processor interface (SPI) specification
  - Byte access
  - Direct accessed space directly
  - Indirect access space is accessed by an indirect access scheme
  - Read operations to a reserved address or reserved bit fields return 0.
  - Write operations to reserved addresses or bit fields are ignored.

JTAG

Complies with IEEE 1149.1 standard.

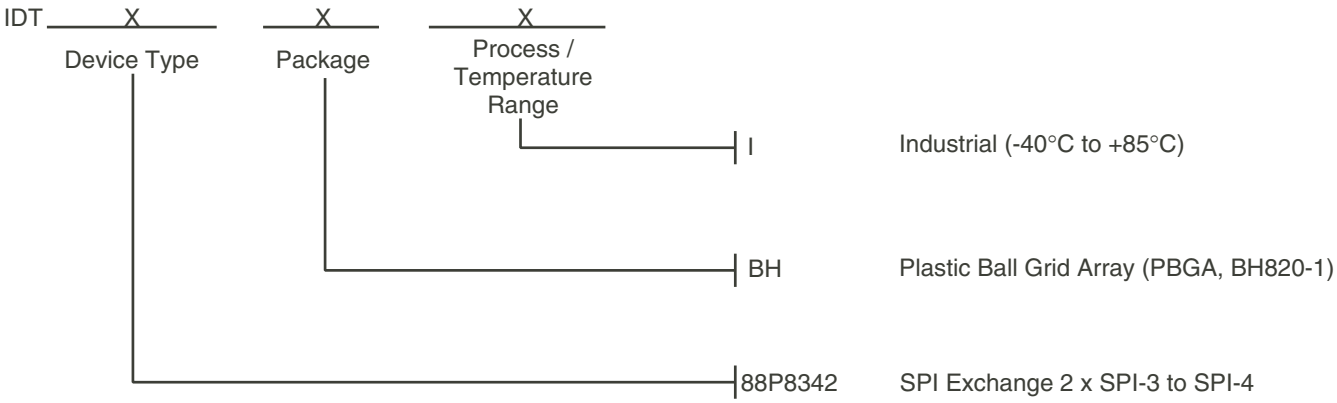
GPIO

Five GPIO signals are provided. Each signal may be independently defined as an input or an output pin.

The GPIO signals are implemented to leave the use of the GPIO pins as flexible as possible. The following can be defined per GPIO pin:

- Direction (1 bit per GPIO, options are In or Out)
- Address of bit to be written / read (N bits per GPIO, includes whole configurable / status memory map – i.e. data memory is not required)
- Value to read / write (5 bits – used when address in previous register is this address)

ORDERING INFORMATION



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CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
408-330-1533
email: SPI@idt.com