SPI-4 Exchange
Document Issue 1.0

IDT88K8483

Description

The IDT88K8483 is a 3-port SPI-4 Exchange device. The IDT SPI-4 Exchange devices build on IDT's proven SPI-4 implementation and packet fragment processor (PFP) design. The IDT88K8483 suits applications with slow backpressure response and other advanced networking applications when there is the need for duplicate ports to re-route data multiple times through the packet-exchange and temporary storage for complete in-flight packets.

The data on each SPI-4 interface logical port (LP) are mapped to a logical identifier (LID). A data flow between logical port addresses on the various interfaces is accomplished using LID maps that can be dynamically reconfigured. The device enables the connection of two SPI-4 devices to a network processor having one or more SPI-4 interfaces. Up to 18Mbit of additional buffer memory can be provided using the QDRII interface. Alternatively, the HSTL I/O may be used to provide a generic packet interface to a FPGA. The device supports a maximum of 128 logical ports.

Applications

- *Ethernet transport*
- *SONET / SDH packet transport line cards*
- *Broadband aggregation*
- *Multi-service switches*
- *IP services equipment*
- *Security firewalls*

Features

- **Functionality**
  - *Multiplexes logical ports (LPs) from SPI-4A and SPI-4B to SPI-4M*
  - *Optionally converts between interleaved packet transfers and whole packet transfers per logical port*
  - *Data redirection per LP between SPI-4A, SPI-4B and 10G FPGA*
  - *Per LP configurable memory allocation*
  - *Per LP memory expansion via QDR-II SRAM interface*
  - *3 separate clock generators allowing fully flexible, fully integrated clock derivations and generation*
- **Standard Interfaces**
  - *Two OIF SPI-4 phase 2: 80 - 450 MHz, 256 address range, 64 concurrently active LPs per interface*
  - *One OIF SPI-4 phase 2: 80 - 450 MHz, 256 address range, 128 concurrently active LPs*
  - *SPI-4 FIFO status channel options:*
  - *LVDS full-rate, LVDS quarter-rate, LVTTL quarter-rate*
  - *SPI-4 compatible with Network Processor Streaming Interface (NPSI NPE-Framer mode of operation)*
  - *HSTL Interface with selectable operating mode*

    160 - 200 MHz DDR packet interface, 64 concurrently active LPs; or

    QDR-II memory interface: 160 - 200MHz HSTL
  - *Serial or parallel microprocessor interface for control and monitoring*
  - *IEEE 1491.1 JTAG*

Block Diagram

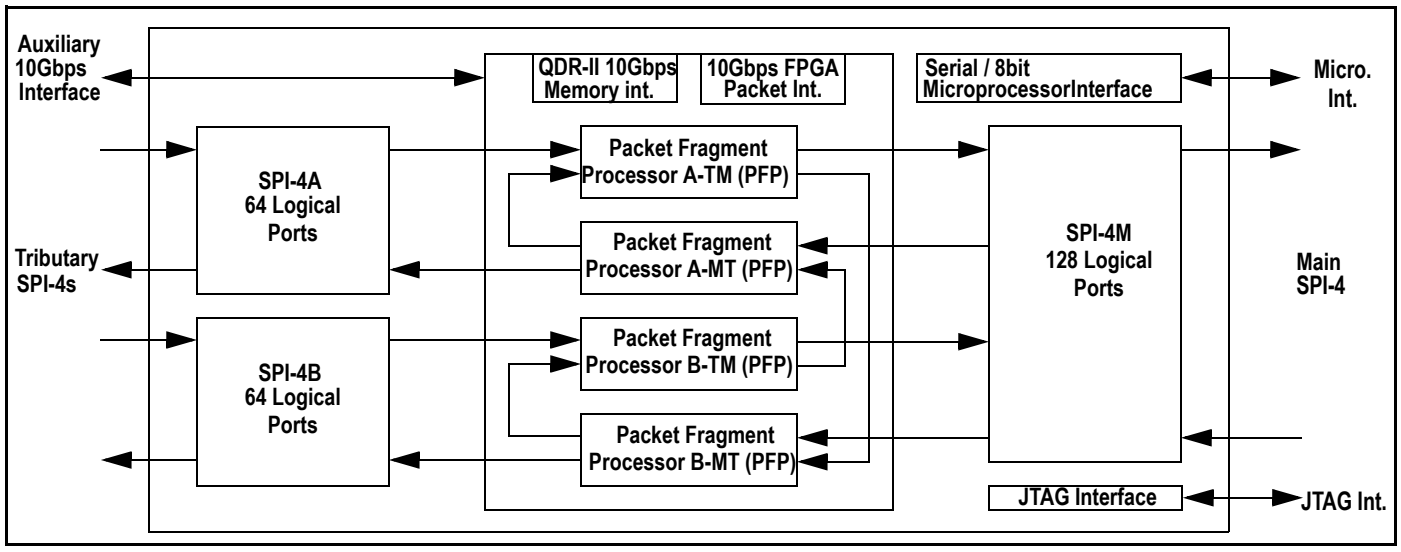

Figure 1 IDT88K8483 Block Diagram

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Pin Assignment

The following table shows the IDT88K8483 pins and their corresponding symbols.

Function	Pin
ADR0	E1
ADR1	E2
ADR2	D2
ADR3	C4
ADR4	D3
ADR5	B4
BOND0	R6
BOND1	P6
CSB	D5
DAT0	A5
DAT1	A4
DAT2	A3
DAT3	B3
DAT4	C3
DAT5	C2
DAT6	C1
DAT7	D1
DIV4	AB6
GPIO0	AE5
GPIO1	AD5
GPIO2	AC5
INTB	D4
MPM	E4
QDR_A0	L24
QDR_A1	M24
QDR_A10	R24
QDR_A11	R23
QDR_A12	R22
QDR_A13	T21
QDR_A14	R21
QDR_A15	P21
QDR_A16	N21
QDR_A17	M21
QDR_A2	N24

Table 1 IDT88K8483 Pinout (Part 1 of 19)

Function	Pin
QDR_A3	N23
QDR_A4	N22
QDR_A5	P22
QDR_A6	P23
QDR_A7	P24
QDR_A8	P25
QDR_A9	P26
QDR_CQ	N26
QDR_CQB	N25
QDR_D0	D25
QDR_D1	H22
QDR_D10	K23
QDR_D11	K24
QDR_D12	K25
QDR_D13	M22
QDR_D14	M23
QDR_D15	K26
QDR_D16	H26
QDR_D17	F26
QDR_D18	R25
QDR_D19	U26
QDR_D2	F23
QDR_D20	W26
QDR_D21	U25
QDR_D22	W25
QDR_D23	U24
QDR_D24	W24
QDR_D25	U23
QDR_D26	U22
QDR_D27	AC26
QDR_D28	AA26
QDR_D29	AC25
QDR_D3	H23
QDR_D30	Y25
QDR_D31	Y24
QDR_D32	AA23
QDR_D33	AA22

Table 1 IDT88K8483 Pinout (Part 2 of 19)

Function	Pin
QDR_D34	W23
QDR_D35	W22
QDR_D4	F24
QDR_D5	H24
QDR_D6	F25
QDR_D7	H25
QDR_D8	D26
QDR_D9	K22
QDR_IMP	AD25
QDR_K	L26
QDR_KB	L25
QDR_Q0	C25
QDR_Q1	G22
QDR_Q10	J23
QDR_Q11	J24
QDR_Q12	J25
QDR_Q13	L22
QDR_Q14	L23
QDR_Q15	J26
QDR_Q16	G26
QDR_Q17	E26
QDR_Q18	R26
QDR_Q19	T26
QDR_Q2	F22
QDR_Q20	V26
QDR_Q21	T25
QDR_Q22	V25
QDR_Q23	T24
QDR_Q24	V24
QDR_Q25	T23
QDR_Q26	T22
QDR_Q27	AB26
QDR_Q28	Y26
QDR_Q29	AB25
QDR_Q3	G23
QDR_Q30	AA25
QDR_Q31	AA24

Table 1 IDT88K8483 Pinout (Part 3 of 19)

Function	Pin
QDR_Q32	Y23
QDR_Q33	Y22
QDR_Q34	V23
QDR_Q35	V22
QDR_Q4	E24
QDR_Q5	G24
QDR_Q6	E25
QDR_Q7	G25
QDR_Q8	C26
QDR_Q9	J22
QDR_RB	K21
QDR_VREF	AD26
QDR_WB	L21
RDB	C5
RESETB	AF4
SPI4A_BIAS	A24
SPI4A_CLK_SEL	F21
SPI4A_ECTL_N	D15
SPI4A_ECTL_P	D14
SPI4A_ED[0]_N	E15
SPI4A_ED[0]_P	E14
SPI4A_ED[1]_N	E17
SPI4A_ED[1]_P	E16
SPI4A_ED[10]_N	A19
SPI4A_ED[10_P	A18
SPI4A_ED[11]_N	E21
SPI4A_ED[11]_P	E20
SPI4A_ED[12]_N	D21
SPI4A_ED[12]_P	D20
SPI4A_ED[13]_N	D22
SPI4A_ED[13]_P	E22
SPI4A_ED[14]_N	C21
SPI4A_ED[14]_P	C20
SPI4A_ED[15]_N	B21
SPI4A_ED[15]_P	B20
SPI4A_ED[2]_N	D17
SPI4A_ED[2]_P	D16

Table 1 IDT88K8483 Pinout (Part 4 of 19)

Function	Pin
SPI4A_ED[3]_N	C17
SPI4A_ED[3]_P	C16
SPI4A_ED[4]_N	B17
SPI4A_ED[4]_P	B16
SPI4A_ED[5]_N	A17
SPI4A_ED[5]_P	A16
SPI4A_ED[6]_N	E19
SPI4A_ED[6]_P	E18
SPI4A_ED[7]_N	D19
SPI4A_ED[7]_P	D18
SPI4A_ED[8]_N	C19
SPI4A_ED[8]_P	C18
SPI4A_ED[9]_N	B19
SPI4A_ED[9]_P	B18
SPI4A_EDCLK_N	A21
SPI4A_EDCLK_P	A20
SPI4A_ESCLK_N	A7
SPI4A_ESCLK_P	A6
SPI4A_ESCLK_T	D6
SPI4A_ESTA[0]_N	C7
SPI4A_ESTA[0]_P	C6
SPI4A_ESTA[1]_N	B7
SPI4A_ESTA[1]_P	B6
SPI4A_ESTA_T0	E7
SPI4A_ESTA_T1	D7
SPI4A_ICTL_N	E9
SPI4A_ICTL_P	E8
SPI4A_ID[0]_N	D9
SPI4A_ID[0]_P	D8
SPI4A_ID[1]_N	C9
SPI4A_ID[1]_P	C8
SPI4A_ID[10]_N	D13
SPI4A_ID[10]_P	D12
SPI4A_ID[11]_N	C13
SPI4A_ID[11]_P	C12
SPI4A_ID[12]_N	B13
SPI4A_ID[12]_P	B12

Table 1 IDT88K8483 Pinout (Part 5 of 19)

Function	Pin
SPI4A_ID[13]_N	A13
SPI4A_ID[13]_P	A12
SPI4A_ID[14]_N	C15
SPI4A_ID[14]_P	C14
SPI4A_ID[15]_N	B15
SPI4A_ID[15]_P	B14
SPI4A_ID[2]_N	B9
SPI4A_ID[2]_P	B8
SPI4A_ID[3]_N	A9
SPI4A_ID[3]_P	A8
SPI4A_ID[4]_N	E11
SPI4A_ID[4]_P	E10
SPI4A_ID[5]_N	D11
SPI4A_ID[5]_P	D10
SPI4A_ID[6]_N	C11
SPI4A_ID[6]_P	C10
SPI4A_ID[7]_N	B11
SPI4A_ID[7]_P	B10
SPI4A_ID[8]_N	A11
SPI4A_ID[8]_P	A10
SPI4A_ID[9]_N	E13
SPI4A_ID[9]_P	E12
SPI4A_IDCLK_N	A15
SPI4A_IDCLK_P	A14
SPI4A_ISCLK_N	A23
SPI4A_ISCLK_P	A22
SPI4A_ISCLK_T	C24
SPI4A_ISTA[0]_N	C23
SPI4A_ISTA[0]_P	C22
SPI4A_ISTA[1]_N	B23
SPI4A_ISTA[1]_P	B22
SPI4A_ISTA_T0	D23
SPI4A_ISTA_T1	D24
SPI4A_LVDSSTA	G21
SPI4A_RCLK	E23
SPI4A_VREF	B24
SPI4B_BIAS	AF24

Table 1 IDT88K8483 Pinout (Part 6 of 19)

Function	Pin
SPI4B_CLK_SEL	AA21
SPI4B_ECTL_N	AC15
SPI4B_ECTL_P	AC14
SPI4B_ED[0]_N	AB15
SPI4B_ED[0]_P	AB14
SPI4B_ED[1]_N	AB17
SPI4B_ED[1]_P	AB16
SPI4B_ED[10]_N	AF19
SPI4B_ED[10_P	AF18
SPI4B_ED[11]_N	AB21
SPI4B_ED[11]_P	AB20
SPI4B_ED[12]_N	AC21
SPI4B_ED[12]_P	AC20
SPI4B_ED[13]_N	AC22
SPI4B_ED[13]_P	AB22
SPI4B_ED[14]_N	AD21
SPI4B_ED[14]_P	AD20
SPI4B_ED[15]_N	AE21
SPI4B_ED[15]_P	AE20
SPI4B_ED[2]_N	AC17
SPI4B_ED[2]_P	AC16
SPI4B_ED[3]_N	AD17
SPI4B_ED[3]_P	AD16
SPI4B_ED[4]_N	AE17
SPI4B_ED[4]_P	AE16
SPI4B_ED[5]_N	AF17
SPI4B_ED[5]_P	AF16
SPI4B_ED[6]_N	AB19
SPI4B_ED[6]_P	AB18
SPI4B_ED[7]_N	AC19
SPI4B_ED[7]_P	AC18
SPI4B_ED[8]_N	AD19
SPI4B_ED[8]_P	AD18
SPI4B_ED[9]_N	AE19
SPI4B_ED[9]_P	AE18
SPI4B_EDCLK_N	AF21
SPI4B_EDCLK_P	AF20

Table 1 IDT88K8483 Pinout (Part 7 of 19)

Function	Pin
SPI4B_ESCLK_N	AF7
SPI4B_ESCLK_P	AF6
SPI4B_ESCLK_T	AC6
SPI4B_ESTA[0]_N	AD7
SPI4B_ESTA[0]_P	AD6
SPI4B_ESTA[1]_N	AE7
SPI4B_ESTA[1]_P	AE6
SPI4B_ESTA_T0	AB7
SPI4B_ESTA_T1	AC7
SPI4B_ICTL_N	AB9
SPI4B_ICTL_P	AB8
SPI4B_ID[0]_N	AC9
SPI4B_ID[0]_P	AC8
SPI4B_ID[1]_N	AD9
SPI4B_ID[1]_P	AD8
SPI4B_ID[10]_N	AC13
SPI4B_ID[10]_P	AC12
SPI4B_ID[11]_N	AD13
SPI4B_ID[11]_P	AD12
SPI4B_ID[12]_N	AE13
SPI4B_ID[12]_P	AE12
SPI4B_ID[13]_N	AF13
SPI4B_ID[13]_P	AF12
SPI4B_ID[14]_N	AD15
SPI4B_ID[14]_P	AD14
SPI4B_ID[15]_N	AE15
SPI4B_ID[15]_P	AE14
SPI4B_ID[2]_N	AE9
SPI4B_ID[2]_P	AE8
SPI4B_ID[3]_N	AF9
SPI4B_ID[3]_P	AF8
SPI4B_ID[4]_N	AB11
SPI4B_ID[4]_P	AB10
SPI4B_ID[5]_N	AC11
SPI4B_ID[5]_P	AC10
SPI4B_ID[6]_N	AD11
SPI4B_ID[6]_P	AD10

Table 1 IDT88K8483 Pinout (Part 8 of 19)

Function	Pin
SPI4B_ID[7]_N	AE11
SPI4B_ID[7]_P	AE10
SPI4B_ID[8]_N	AF11
SPI4B_ID[8]_P	AF10
SPI4B_ID[9]_N	AB13
SPI4B_ID[9]_P	AB12
SPI4B_IDCLK_N	AF15
SPI4B_IDCLK_P	AF14
SPI4B_ISCLK_N	AF23
SPI4B_ISCLK_P	AF22
SPI4B_ISCLK_T	AD24
SPI4B_ISTA[0]_N	AD23
SPI4B_ISTA[0]_P	AD22
SPI4B_ISTA[1]_N	AE23
SPI4B_ISTA[1]_P	AE22
SPI4B_ISTA_T0	AC23
SPI4B_ISTA_T1	AC24
SPI4B_LVDSTA	Y21
SPI4B_RCLK	AB23
SPI4B_VREF	AE24
SPI4M_BIAS	AD1
SPI4M_CLK_SEL	AE3
SPI4M_ECTL_N	R4
SPI4M_ECTL_P	P4
SPI4M_ED[0]_N	R5
SPI4M_ED[0]_P	P5
SPI4M_ED[1]_N	U5
SPI4M_ED[1]_P	T5
SPI4M_ED[10]_N	W1
SPI4M_ED[10_P	V1
SPI4M_ED[11]_N	AA5
SPI4M_ED[11]_P	Y5
SPI4M_ED[12]_N	AA4
SPI4M_ED[12]_P	Y4
SPI4M_ED[13]_N	AB4
SPI4M_ED[13]_P	AB5
SPI4M_ED[14]_N	AA3

Table 1 IDT88K8483 Pinout (Part 9 of 19)

Function	Pin
SPI4M_ED[14]_P	Y3
SPI4M_ED[15]_N	AA2
SPI4M_ED[15]_P	Y2
SPI4M_ED[2]_N	U4
SPI4M_ED[2]_P	T4
SPI4M_ED[3]_N	U3
SPI4M_ED[3]_P	T3
SPI4M_ED[4]_N	U2
SPI4M_ED[4]_P	T2
SPI4M_ED[5]_N	U1
SPI4M_ED[5]_P	T1
SPI4M_ED[6]_N	W5
SPI4M_ED[6]_P	V5
SPI4M_ED[7]_N	W4
SPI4M_ED[7]_P	V4
SPI4M_ED[8]_N	W3
SPI4M_ED[8]_P	V3
SPI4M_ED[9]_N	W2
SPI4M_ED[9]_P	V2
SPI4M_EDCLK_N	AA1
SPI4M_EDCLK_P	Y1
SPI4M_ESCLK_N	G1
SPI4M_ESCLK_P	F1
SPI4M_ESCLK_T	F4
SPI4M_ESTA[0]_N	G3
SPI4M_ESTA[0]_P	F3
SPI4M_ESTA[1]_N	G2
SPI4M_ESTA[1]_P	F2
SPI4M_ESTA_T0	G5
SPI4M_ESTA_T1	G4
SPI4M_ICTL_N	J5
SPI4M_ICTL_P	H5
SPI4M_ID[0]_N	J4
SPI4M_ID[0]_P	H4
SPI4M_ID[1]_N	J3
SPI4M_ID[1]_P	H3
SPI4M_ID[10]_N	N4

Table 1 IDT88K8483 Pinout (Part 10 of 19)

Function	Pin
SPI4M_ID[10]_P	M4
SPI4M_ID[11]_N	N3
SPI4M_ID[11]_P	M3
SPI4M_ID[12]_N	N2
SPI4M_ID[12]_P	M2
SPI4M_ID[13]_N	N1
SPI4M_ID[13]_P	M1
SPI4M_ID[14]_N	R3
SPI4M_ID[14]_P	P3
SPI4M_ID[15]_N	R2
SPI4M_ID[15]_P	P2
SPI4M_ID[2]_N	J2
SPI4M_ID[2]_P	H2
SPI4M_ID[3]_N	J1
SPI4M_ID[3]_P	H1
SPI4M_ID[4]_N	L5
SPI4M_ID[4]_P	K5
SPI4M_ID[5]_N	L4
SPI4M_ID[5]_P	K4
SPI4M_ID[6]_N	L3
SPI4M_ID[6]_P	K3
SPI4M_ID[7]_N	L2
SPI4M_ID[7]_P	K2
SPI4M_ID[8]_N	L1
SPI4M_ID[8]_P	K1
SPI4M_ID[9]_N	N5
SPI4M_ID[9]_P	M5
SPI4M_IDCLK_N	R1
SPI4M_IDCLK_P	P1
SPI4M_ISCLK_N	AC1
SPI4M_ISCLK_P	AB1
SPI4M_ISCLK_T	AD3
SPI4M_ISTA[0]_N	AC3
SPI4M_ISTA[0]_P	AB3
SPI4M_ISTA[1]_N	AC2
SPI4M_ISTA[1]_P	AB2
SPI4M_ISTA_T0	AC4

Table 1 IDT88K8483 Pinout (Part 11 of 19)

Function	Pin
SPI4M_ISTA_T1	AD4
SPI4M_LVDSTA	AF5
SPI4M_RCLK	AF3
SPI4M_VREF	AD2
SPIEN	E3
TCK	M6
TDI	W21
TDO	N6
TESTSE	J21
TIMEBASE	AE4
TMS	H21
TRSTB	V21
WRB	B5
VDDA25	AA17
VDDA25	AA10
VDDA25	F17
VDDA25	F10
VDDA25	G17
VDDA25	G10
VDDA25	L8
VDDA25	L7
VDDA25	U8
VDDA25	U7
VDDA25	Y17
VDDA25	Y10
VDDC12	H17
VDDC12	H16
VDDC12	H15
VDDC12	H14
VDDC12	H13
VDDC12	H12
VDDC12	H11
VDDC12	H10
VDDC12	H9
VDDC12	H19
VDDC12	H18
VDDC12	J17

Table 1 IDT88K8483 Pinout (Part 12 of 19)

Function	Pin
VDDC12	J16
VDDC12	J15
VDDC12	J14
VDDC12	J13
VDDC12	J12
VDDC12	J11
VDDC12	J10
VDDC12	J9
VDDC12	J19
VDDC12	J18
VDDC12	K10
VDDC12	K9
VDDC12	K19
VDDC12	K18
VDDC12	L10
VDDC12	L9
VDDC12	L19
VDDC12	L18
VDDC12	M10
VDDC12	M9
VDDC12	M19
VDDC12	M18
VDDC12	N10
VDDC12	N9
VDDC12	N19
VDDC12	N18
VDDC12	P10
VDDC12	P9
VDDC12	P19
VDDC12	P18
VDDC12	R10
VDDC12	R9
VDDC12	R19
VDDC12	R18
VDDC12	T10
VDDC12	T9
VDDC12	T19

Table 1 IDT88K8483 Pinout (Part 13 of 19)

Function	Pin
VDDC12	T18
VDDC12	U10
VDDC12	U9
VDDC12	U19
VDDC12	U18
VDDC12	V17
VDDC12	V16
VDDC12	V15
VDDC12	V14
VDDC12	V13
VDDC12	V12
VDDC12	V11
VDDC12	V10
VDDC12	V9
VDDC12	V19
VDDC12	V18
VDDC12	W17
VDDC12	W16
VDDC12	W15
VDDC12	W14
VDDC12	W13
VDDC12	W12
VDDC12	W11
VDDC12	W10
VDDC12	W9
VDDC12	W19
VDDC12	W18
VDDH15	M26
VDDH15	AE26
VDDH15	B26
VDDH15	M20
VDDH15	N20
VDDH15	V20
VDDH15	W20
VDDH15	Y20
VDDH25	G19
VDDH25	Y19

Table 1 IDT88K8483 Pinout (Part 14 of 19)

Function	Pin
VDDL12	AA13
VDDL12	AA12
VDDL12	F13
VDDL12	F12
VDDL12	G13
VDDL12	G12
VDDL12	M8
VDDL12	M7
VDDL12	N8
VDDL12	N7
VDDL12	Y13
VDDL12	Y12
VDDL25	AA14
VDDL25	AA9
VDDL25	AA8
VDDL25	AA18
VDDL25	F14
VDDL25	F9
VDDL25	F8
VDDL25	F18
VDDL25	G14
VDDL25	G9
VDDL25	G8
VDDL25	G18
VDDL25	H8
VDDL25	H7
VDDL25	P8
VDDL25	P7
VDDL25	V8
VDDL25	V7
VDDL25	W8
VDDL25	W7
VDDL25	Y14
VDDL25	Y9
VDDL25	Y8
VDDL25	Y18
VDDT33	A25

Table 1 IDT88K8483 Pinout (Part 15 of 19)

Function	Pin
VDDT33	A2
VDDT33	AF25
VDDT33	AF2
VSS	AA7
VSS	AA6
VSS	AB24
VSS	AE25
VSS	AE2
VSS	B25
VSS	B2
VSS	E6
VSS	E5
VSS	F7
VSS	F6
VSS	F5
VSS	G7
VSS	G6
VSS	H6
VSS	J6
VSS	K17
VSS	K16
VSS	K15
VSS	K14
VSS	K13
VSS	K12
VSS	K11
VSS	K6
VSS	L17
VSS	L16
VSS	L15
VSS	L14
VSS	L13
VSS	L12
VSS	L11
VSS	L6
VSS	M17
VSS	M16

Table 1 IDT88K8483 Pinout (Part 16 of 19)

Function	Pin
VSS	M14
VSS	M11
VSS	N17
VSS	N16
VSS	N12
VSS	N11
VSS	P17
VSS	P16
VSS	P11
VSS	R17
VSS	R16
VSS	R13
VSS	R11
VSS	T17
VSS	T16
VSS	T15
VSS	T14
VSS	T13
VSS	T12
VSS	T11
VSS	T6
VSS	U17
VSS	U16
VSS	U15
VSS	U14
VSS	U13
VSS	U12
VSS	U11
VSS	U6
VSS	V6
VSS	W6
VSS	Y7
VSS	Y6
VSS	M25
VSS	AA16
VSS	AA11
VSS	F16

Table 1 IDT88K8483 Pinout (Part 17 of 19)

Function	Pin
VSS	F11
VSS	G16
VSS	G11
VSS	K8
VSS	K7
VSS	T8
VSS	T7
VSS	Y16
VSS	Y11
VSS	K20
VSS	L20
VSS	P20
VSS	AA20
VSS	AA19
VSS	F20
VSS	F19
VSS	AA15
VSS	F15
VSS	G15
VSS	J8
VSS	J7
VSS	R8
VSS	R7
VSS	Y15
VSS	AE1
VSS	B1
VSS	U21
VSS	M13
VSS	M12
VSS	R12
VSS	P12
VSS	P14
VSS	P15
VSS	N13
VSS	N15
VSS	M15
VSS	R14

Table 1 IDT88K8483 Pinout (Part 18 of 19)

Function	Pin
VSS	R15
VSS	N14
VSS	P13
VTT075	G20
VTT075	H20
VTT075	J20
VTT075	R20
VTT075	T20
VTT075	U20
NP[1]	A1
NP[1]	A26
NP[1]	AF1
NP[1]	AF26

Table 1 IDT88K8483 Pinout (Part 19 of 19)

Pin Description Table

The following table lists the functions of the pins provided on the IDT88K8483. Some of the functions listed are multiplexed onto the same pin.

The active polarity of a signal is defined using a suffix. Analog signals ending with “P” are defined as being positive. Analog signals ending with “N” are defined as being negative. Digital signals ending with “B” are defined as being active, or asserted, when at a logic zero (low) level. All other digital signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Symbol[1]	I/O	Type[2]	Function	Comments	
SPI-4 Interface				**Link**	**PHY**
SPI4A_ED[15:0]_P SPI4B_ED[15:0]_P SPI4M_ED[15:0]_P SPI4A_ED[15:0]_N SPI4B_ED[15:0]_N SPI4M_ED[15:0]_N	O	LVDS	Egress Data Bus. This data bus is used to carry egress payload data and in-band control words.	TDAT[15:0]	RDAT[15:0]
SPI4A_EDCLK_P SPI4B_EDCLK_P SPI4M_EDCLK_P SPI4A_EDCLK_N SPI4B_EDCLK_N SPI4M_EDCLK_N	O	LVDS	Egress Data Clock. This clock is associated with the egress data bus (ED) and the control signal (ECTL).	TDCLK	RDCLK
SPI4A_ECTL_P SPI4B_ECTL_P SPI4M_ECTL_P SPI4A_ECTL_N SPI4B_ECTL_N SPI4M_ECTL_N	O	LVDS	Egress Control. This signal is high when a control word is present on the egress data bus (ED) and it is low otherwise.	TCTL	RCTL
SPI4A_ESTA[1:0]_P SPI4B_ESTA[1:0]_P SPI4M_ESTA[1:0]_P SPI4A_ESTA[1:0]_N SPI4B_ESTA[1:0]_N SPI4M_ESTA[1:0]_N	I	LVDS	Egress FIFO Status LVDS. These signals are used to carry egress round-robin FIFO status information, along with associated error detection and framing.	TSTAT[1:0]	RSTAT[1:0]
SPI4A_ESCLK_P SPI4B_ESCLK_P SPI4M_ESCLK_P SPI4A_ESCLK_N SPI4B_ESCLK_N SPI4M_ESCLK_N	I	LVDS	Egress Status Clock LVDS. This clock is associated with the egress FIFO status signals (ESTA).	TSCLK	RSCLK
SPI4A_ESTA_T[1:0] SPI4B_ESTA_T[1:0] SPI4M_ESTA_T[1:0]	I	LVTTL Pull-up	Egress FIFO Status LVTTL. These signals are used to carry egress round-robin FIFO status information, along with associated error detection and framing.	TSTAT[1:0]	RSTAT[1:0]
SPI4A_ESCLK_T SPI4B_ESCLK_T SPI4M_ESCLK_T	I	LVTTL Pull-up Schmitt Trigger	Egress Status Clock LVTTL. This clock is associated with the egress FIFO status signals (ESTA_T).	TSCLK	RSCLK

Table 2 Pin Description (Part 1 of 5)

Symbol[1]	I/O	Type[2]	Function	Comments	
SPI4A_ID[15:0]_P SPI4B_ID[15:0]_P SPI4M_ID[15:0]_P SPI4A_ID[15:0]_N SPI4B_ID[15:0]_N SPI4M_ID[15:0]_N	I	LVDS	Ingress Data Bus. This data bus is used to carry ingress payload data and in-band control words.	RDAT[15:0]	TDAT[15:0]
SPI4A_IDCLK_P SPI4B_IDCLK_P SPI4M_IDCLK_P SPI4A_IDCLK_N SPI4B_IDCLK_N SPI4M_IDCLK_N	I	LVDS	Ingress Data Clock. This clock is associated with the ingress data bus (ID) and the control signal (ICTL).	RDCLK	TDCLK
SPI4A_ICTL_P SPI4B_ICTL_P SPI4M_ICTL_P SPI4A_ICTL_N SPI4B_ICTL_N SPI4M_ICTL_N	I	LVDS	Ingress Control. This signal is high when a control word is present on the ingress data bus (ID) and it is low otherwise.	RCTL	TCTL
SPI4A_ISTA[1:0]_P SPI4B_ISTA[1:0]_P SPI4M_ISTA[1:0]_P SPI4A_ISTA[1:0]_N SPI4B_ISTA[1:0]_N SPI4M_ISTA[1:0]_N	O	LVDS	Ingress FIFO Status LVDS. These signals are used to carry ingress round-robin FIFO status information, along with associated error detection and framing.	RSTAT[1:0]	TSTAT[1:0]
SPI4A_ISCLK_P SPI4B_ISCLK_P SPI4M_ISCLK_P SPI4A_ISCLK_N SPI4B_ISCLK_N SPI4M_ISCLK_N	O	LVDS	Ingress Status Clock LVDS. This clock is associated with the ingress FIFO status signals (ISTA).	RSCLK	TSCLK
SPI4A_ISTA_T[1:0] SPI4B_ISTA_T[1:0] SPI4M_ISTA_T[1:0]	O	LVTTL Pull-up	Ingress FIFO Status LVTTL. These signals are used to carry ingress round-robin FIFO status information, along with associated error detection and framing.	RSTAT[1:0]	TSTAT[1:0]
SPI4A_ISCLK_T SPI4B_ISCLK_T SPI4M_ISCLK_T	O	LVTTL Pull-up Schmitt Trigger	Ingress Status Clock LVTTL. This clock is associated with the ingress FIFO status signals (ISTA_T).	RSCLK	TSCLK
SPI4A_BIAS SPI4B_BIAS SPI4M_BIAS		Analog	BIAS. This signal must be connected via an external pull-down 1% 3KΩ resistor to VSS.		
SPI4A_VREF SPI4B_VREF SPI4M_VREF		Analog	REF. These signals are reference for LVDS. These signals should be connected to VDDL12.		
SPI4A_LVDSSTA SPI4B_LVDSSTA SPI4M_LVDSSTA	I	CMOS Pull-down	Status Channel Control. This signal controls the status signal I/O type. A hardware reset or software reset must be perform after changing the level of this signal. 1 - LVDS status. 0 - LVTTL status.		
QDR-II Interface / Generic Interface (Auxiliary Interface)					
QDR_A[17:0]	O	HSTL	QDR_A[17:0] is QDR-II Address Bus. This bus is used to transfer the address to the QDR-II / FPGA devices. It is driven out on the rising edge of K and $\overline{K}$ clocks during write or read operation.		

Table 2 Pin Description (Part 2 of 5)

Symbol[1]	I/O	Type[2]	Function	Comments	
QDR_D[35:0]/ G_ECTL[3:0], G_EDAT[31:0]	O	HSTL	QDR_D[35:0] is QDR-II Output Data Bus. This bus is used to transfer the data to the QDR-II / FPGA devices. It is driven out on the rising edge of K and $\overline{K}$ clocks during write operation. G_ECTL[3:0] is Generic Interface Egress Control Bus. G_EDAT[31:0] is Generic Interface Egress Data Bus.		
QDR_Q[35:0]/ G_ICTL[3:0], G_IDAT[31:0]	I	HSTL	QDR_Q[35:0] is QDR-II Input Data Bus. This bus is used to transfer data from the QDR-II / FPGA devices. It is sampled on the rising edge of K and $\overline{K}$ clocks during read operation. G_ICTL[3:0] is Generic Interface Ingress Control Bus. G_IDAT[31:0] is Generic Interface Ingress Data Bus.		
QDR_RB	O	HSTL	QDR_RB is QDR-II Read Control. This active low signal is driven out on the rising edge of K clock. When it active, a read operation is initiated. When it deasserted, the read port is deselected.		
QDR_WB	O	HSTL	QDR_WB is QDR-II Write Control. This active low signal is driven out on the rising edge of K clock. When it asserted, a write operation is initiated. When it deasserted, the write port is deselected.		
QDR_K / G_ECLKP	O	HSTL	QDR_K is QDR-II Positive Output Clock. The rising edge of QDR_K is used to capture input data to the device and to drive out data from the device. G_ECLKP is Generic Interface Positive Egress Clock.		
QDR_KB / G_ECLKN	O	HSTL	QDR_KB is QDR-II Negative Output Clock. The rising edge of QDR_KB is used to capture input data to the device and to drive out data from the device. G_ECLKN is negative Generic Interface Egress Clock.		
QDR_CQ / G_ICLKP	I	HSTL	QDR_CQ is QDR-II Synchronous Positive Input Clock. The rising edge of QDR_CQ is tightly matched to the data inputs and can be used as a data valid indication. G_ICLKP is Generic Interface Positive Ingress Clock.		
QDR_CQB / G_ICLKN	I	HSTL	QDR_CQB is QDR-II Synchronous Negative Input Clock. The rising edge of QDR_CQB is tightly matched to the data inputs and can be used as a data valid indication. G_ICLKN is Generic Interface Negative Ingress Clock.		
QDR_VREF / G_VREF	I	Analog Reference	QDR_VREF is 0.75 Reference Voltage Input. This static input is used to set reference level for HSTL inputs and outputs as well as AC measurement points. This pin should be connected to $V_{DDH15}/2$. G_VREF is 0.75 Reference Voltage Input. This pin should be connected to $V_{DDH15}/2$.		
QDR_IMP / G_IMP	I	Reference	QDR_IMP is Reference Input. This signal must be connected via an external pull-down 100 OHM resistor to VSS. G_IMP is Reference Input. This signal must be connected via an external pull-down 100 OHM resistor to VSS.		
Microprocessor Interface					
ADR[5:0]	I	CMOS	ADR[5:0] is Microprocessor Address Bus. This bus is used to transfer the address from the micro-controller.		
DAT[7:0] / SDO	I/O	CMOS	DAT[7:0] is Microprocessor Data Bus. This bus is used to transfer the data between the device and the microprocessor. SDO (DAT[0]) is Serial Peripheral Interface (SPI) data.		

Table 2 Pin Description (Part 3 of 5)

Symbol[1]	I/O	Type[2]	Function	Comments	
WRB/SDI	I	CMOS Pull-up Schmitt Trigger	WRB is Microprocessor Write Control. Active low. SDI is Serial Peripheral Interface (SPI) Chip Select. Active low.		
RDB / SCLK	I	CMOS Pull-up Schmitt Trigger	RDB is Microprocessor Read Control. Active low. SCLK is Serial Peripheral Interface (SPI) Clock.		
CSB	I	CMOS Pull-up Schmitt Trigger	CSB is Microprocessor Chip Select. Active low.		
INTB	O	CMOS Open Drain	INTB is Microprocessor Interrupt. Active low.		
SPIEN	I	CMOS Pull-up	SPIEN is Serial Peripheral Interface (SPI) mode enable. Active high.		
MPM	I	CMOS Pull-up	MPM is Microprocessor mode Control. This signal controls the micro-controller mode. 1 - Intel Mode. 0 - Motorola Mode.		
JTAG Interface					
TRSTB	I	CMOS Pull-up	JTAG Reset. This active low signal asynchronously resets the boundary scan logic and the JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal.		
TCK	I	CMOS Pull-up Schmitt Trigger	JTAG Clock. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller.		
TMS	I	CMOS Pull-up	JTAG Mode. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.		
TDO	O	CMOS tri-state	JTAG Data Output. This is the serial data shifted out from the boundary scan logic or JTAG Controller.		
TDI	I	CMOS Pull-up	JTAG Data Input. This is the serial data input to the boundary scan logic or JTAG Controller.		
Miscellaneous Interface					
RESETB	I	CMOS Pull-down	Hardware Reset. Active low.		
TESTSE	I	CMOS Pull-down	Test Scan Enable. Active high. Input used for IDT factory test. This signal should be pulled down for normal operation.		
TIMEBASE	I/O	CMOS Pull-up	Time Base. A positive edge on this signal updates the PMON counters. Subsequent edges within approximately 4ms are be ignored.		
GPIO[2:0]	I/O	CMOS Pull-up	General Purpose I/O. These pins can be configured as general purpose I/O pins.		
Clock Interface					
SPI4A_RCLK SPI4B_RCLK SPI4M_RCLK	I	CMOS Pull-up Schmitt Trigger	Interface A/B/M Reference Clock.		
DIV4	I	CMOS Pull-up	Pre-scalar Select. Configuration pin.		

Table 2 Pin Description (Part 4 of 5)

Symbol[1]	I/O	Type[2]	Function	Comments	
SPI4A_CLK_SEL SPI4B_CLK_SEL SPI4M_CLK_SEL	I	CMOS Pull-up	Clock Select. Configuration pin.		
Power Supply and Ground					
VDDC12	PWR		1.2V Core Digital Power Supply.	76 pins total	
VDDL12	PWR		1.2V Digital Power Supply for LVDS.	12 pins total	
VDDH15	PWR		1.5V Digital Power Supply for HSTL.	8 pins total	
VDDL25	PWR		2.5V Digital Power Supply for LVDS.	24 pins total	
VDDH25	PWR		2.5V Digital Power Supply foe HSTL.	2 pins total	
VDDT33	PWR		3.3V Digital Power Supply for LVTTL.	4 pins total	
VDDA25	PWR		2.5V Analog Power Supply.	12 pins total	
VTT075	I/O		These pins are used for termination.	6 pins total	
VSS	PWR		Digital and Analog Ground.	111 pins total	
BOND[1:0]	IO		These pins must be connected to ground	2	

Table 2 Pin Description (Part 5 of 5)

1. In table 2 Pin Description the external pins with multiple functions have both symbols in the Symbol column (column 1). In table1 IDT 88K8483 Pinout the external pins with multiple functions have only the first symbol in the Function column (column 1).

2. All LVDS pins have 100Ω internal termination resistor.

Functional Description

The IDT88K8483 device is a three port SPI exchange device intended for use in Ethernet transport, SONET/SDH line cards, security firewalls, and multi-service switches. The SPI-4 interface is defined by the Optical Internetworking Forum.

The device can be used to provide rate adaptation, switching, aggregation and fragment to packet conversion between network processor units, multi-gigabit MACs, framers and switch fabric interface devices. A set of HSTL pins may be configured as a packet bus to an FPGA or as a QDR-II memory bus. The FPGA interface can be used to reduce the unnecessary overhead generated in the FPGA by a SPI-4 standard interface. QDR-II memory can be added as an expansion of internal memory provided in the device.

DATA PATH

In normal operation, there are two paths through the IDT88K8483 device: the SPI-4A or SPI-4B ingress to SPI-4M egress path, and the SPI-4 M ingress to SPI-4A and SPI-4B egress path. SPI-4 burst sizes are separately configurable for each physical port. Data enter in bursts on a SPI-4 ingress interface and are sent to the SPI-4 ingress port buffers. The bursts are mapped to a SPI-4 address and stored in the buffer segment pool by the packet fragment processor (PFP). The PFP forward the data to the SPI-4 Egress Port Buffer. The content of the Egress Port buffer is transferred to the SPI-4 egress interface and transmitted out in burst.

In addition to the data path described above, there are additional datapaths among the SPI-4 ports, FPGA interface, and microprocessor. Each SPI-4 interface has the ability to perform a per-LP loopback. In addition, the SPI-4A and SPI-4B interfaces can transfer packet bursts on a per-LP basis. All the SPI-4 interfaces can transfer packet bursts to the FPGA interface on a per-LP basis.

Each SPI-4 ingress LP (logical port) can be mapped through LID (Logical Identifier) to each one of the SPI-4 egress LPs

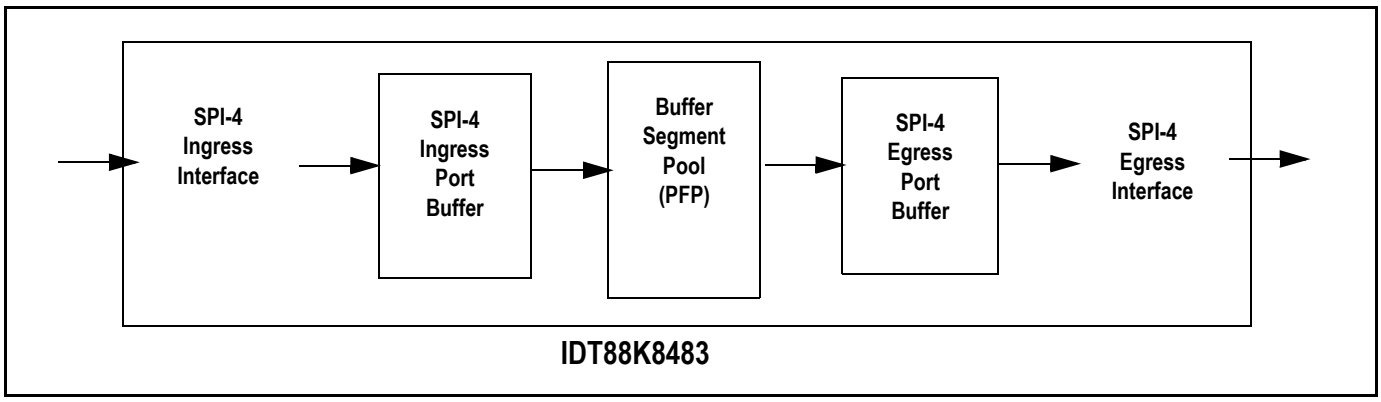


Figure 2 General Data Path

Data Structure

PFP Structure

There are 4 PFPs (Packet Fragment Processor) in the device - one per each port and direction. For example, for SPI-4A ingress to SPI-4M egress there is one PFP. Each PFP has 508 segments, and each segment has 256 bytes as shown in Figure 3 PFP Structure Example p.34. The user can program the LID allocation in the PFP to allocate the 508 segments to the LIDs that will be active. For example, the user can have 64 LIDs, and allocate 7 segments (1,792) bytes to each LID as shown in Figure 4 PFP Allocation Example p.34.

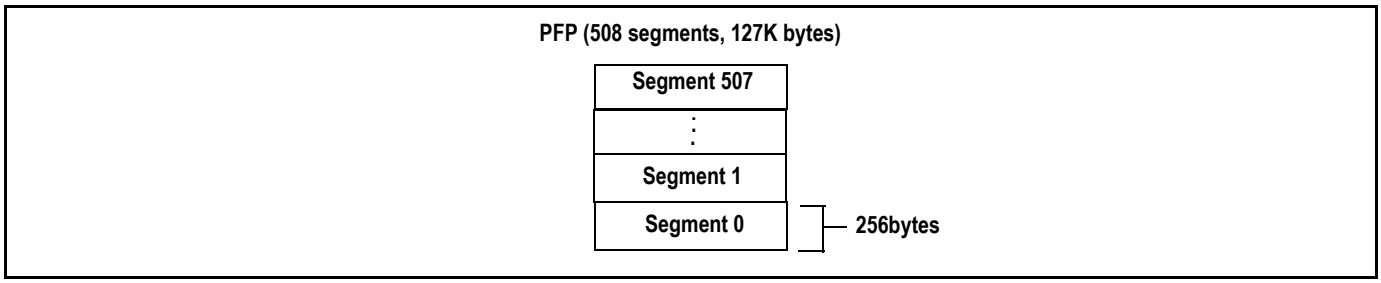


Figure 3 PFP Structure Example

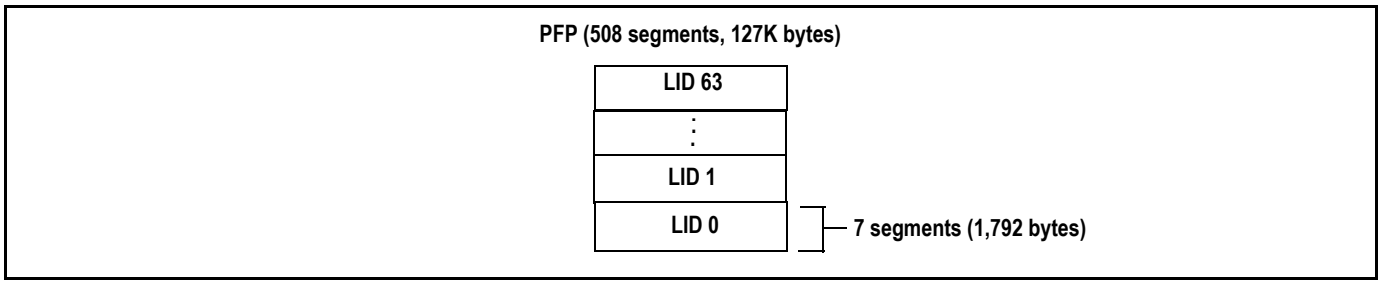


Figure 4 PFP Allocation Example

QDR-II External Memory Structure

The device can be connected to 18M bits QDR-II (2M usable data bytes) SRAM which can store up to 8K segments of 256 bytes as shown in Figure 5 QDR-II SRAM Structure Example p.34. The user can program the LID allocation in the QDR-II. For example, the user can have 64 LIDs, and allocate 128 segments (32Kbytes) to each LID as shown in Figure 6 QDR-II Allocation Example p.34.

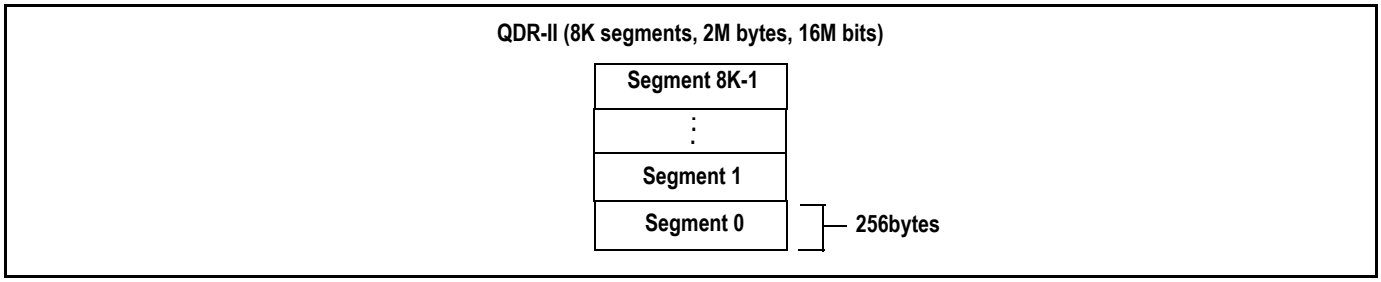


Figure 5 QDR-II SRAM Structure Example

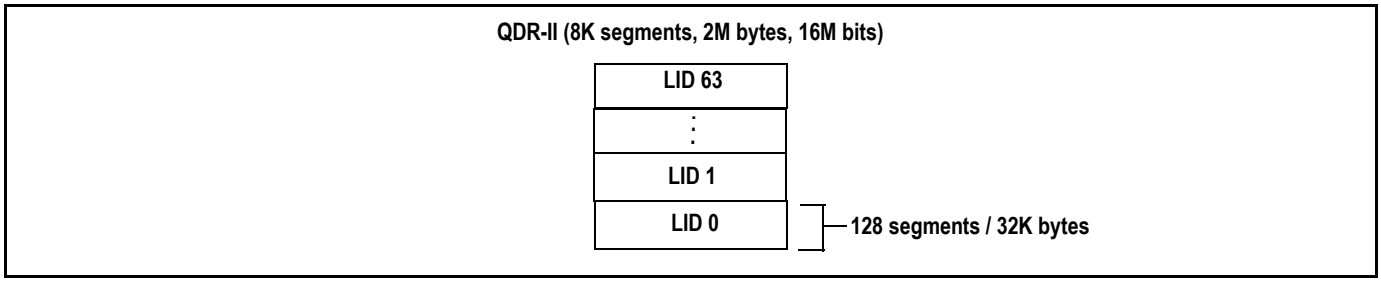


Figure 6 QDR-II Allocation Example

SPI-4 Ingress Port Buffer Structure

Each SPI-4 physical port in the ingress direction has 32 port buffers of 128 bytes as shown in Figure 7 SPI-4 Ingress Port Buffer Structure p.35. The buffers can be concatenated so that data flows from one FIFO into the next.

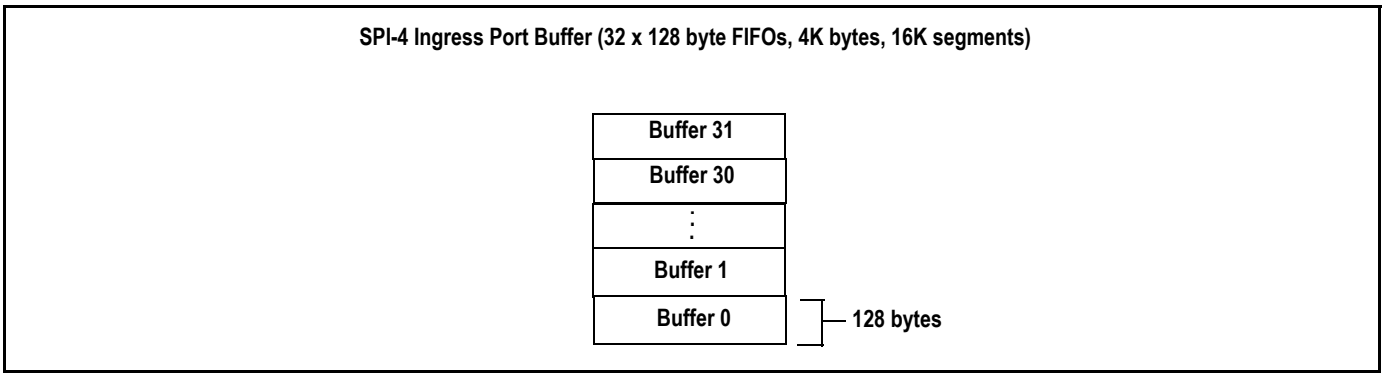


Figure 7 SPI-4 Ingress Port Buffer Structure

Flow Control

SPI-4 Ingress Flow Control

There are 3 main parameters for configuring the SPI-4 ingress flow control:

- Maximum number of segments per LID is configured in M field in the PFP Buffer Segment Assign Table (p. 120)
- Starving Free segments per LID is configured in THR_STARV field in the PFP Buffer Segment Assign Table (p. 120)
- Hungry Free segments per LID is configured in THR_HUNG field in the PFP Buffer Segment Assign Table (p. 120)

SPI-4 ingress flow control is described in greater detail in PFP Flow Control (p. 53)

SPI-4 Egress Flow Control

There are three LID status modes in the SPI-4 egress interface: starving, hungry and satisfied. In normal operation the SPI-4 egress interface is receiving starving status from the adjacent device through the status bus, so the LID status is starving, and the LID data is scheduled out in round robin. When the SPI-4 egress interface starts receiving hungry status from the adjacent device, the LID status is changed to hungry, and the LID data is scheduled out in round robin. When the SPI-4 egress interface starts receiving satisfied status from the adjacent device, the LID status is changed to satisfied, and the LID data is not scheduled out.

Each SPI-4 interface has four SPI-4 calendars: two for ingress and two for egress. Only one calendar in each direction is active in a specific time. There are 64 LIDs per PFP, and each calendar has maximum of 256 entries. Each calendar entry can be assign to a specific LID as shown in Figure 8 SPI-4 Egress Calendar Example p.36. According to the calendar order, the LIDs with starving status are scheduled in a round robin fashion with high priority, and the LIDs with hungry status are scheduled in a round robin fashion with low priority. All the LIDs with the starving status are scheduled first. The LIDs with the hungry status are scheduled only when there are no LIDs with starving status.

The LID status mode in the SPI-4 egress interface (status or credit mode) is configured by CREDIT_EN field in the PFP Flow Control Register (p. 125). If status mode is used (CREDIT_EN=0), then data is sent out until the LID status is changed (starving / hungry / satisfied).

If credit mode is used (CREDIT_EN=1), then when the credit is one, the device sends out one data burst, clears to zero the credit, and then waits for another credit from the SPI-4 interface status bus before issuing another LID burst. In credit mode, when the SPI-4 egress interface receives starving status or hungry status from the adjacent device through the status bus, it sets the LID credit to one. When the SPI-4 egress interface receives satisfied status from the adjacent device, it clears the LID credit to zero.

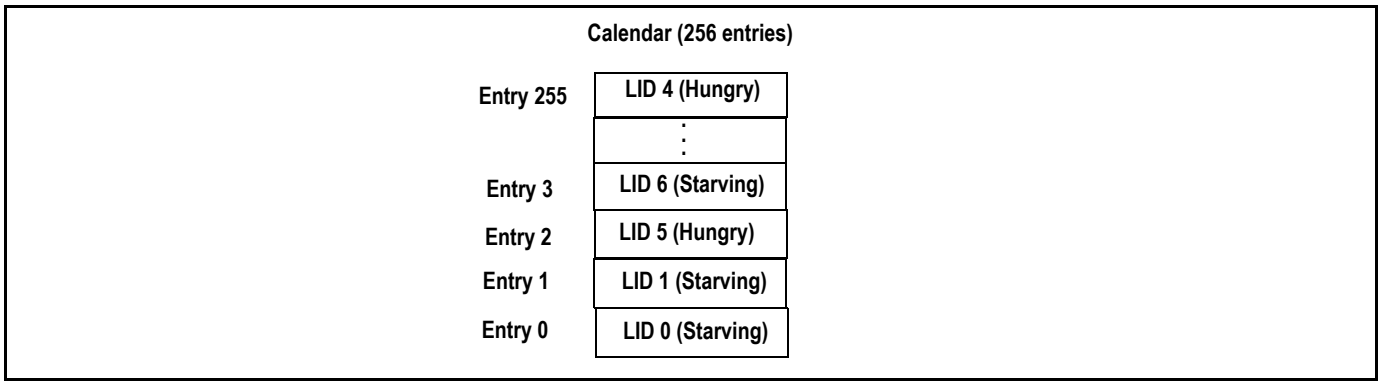


Figure 8 SPI-4 Egress Calendar Example

Data Path Detailed Description

There are several data paths in the device as shown in the figures below.

There are four PFPs in the device: PFP module A Tributary to Main (PFP-A-MT), PFP module A Main to Tributary (PFP-A-MT), PFP module B Tributary to Main (PFP-B-MT) and PFP module B Main to Tributary PFP-B-MT.

SPI-4 tributary to SPI-4 main data path conveys data from SPI-4 tributary ingress to SPI-4 main egress as shown in Figure 9 SPI-4 Tributary to SPI-4 Main Data Path p.36.

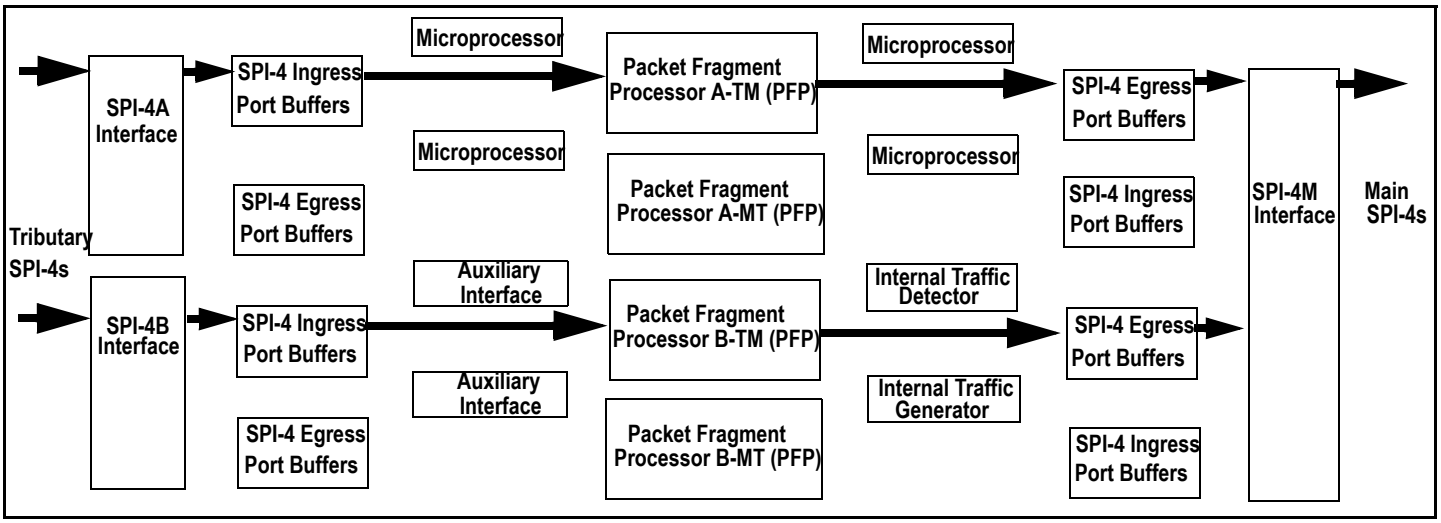


Figure 9 SPI-4 Tributary to SPI-4 Main Data Path

SPI-4 main to SPI-4 tributary data path conveys data from SPI-4 main ingress to SPI-4 tributary egress as shown in Figure 10 SPI-4 main to SPI-4 Tributary Data Path p.37.

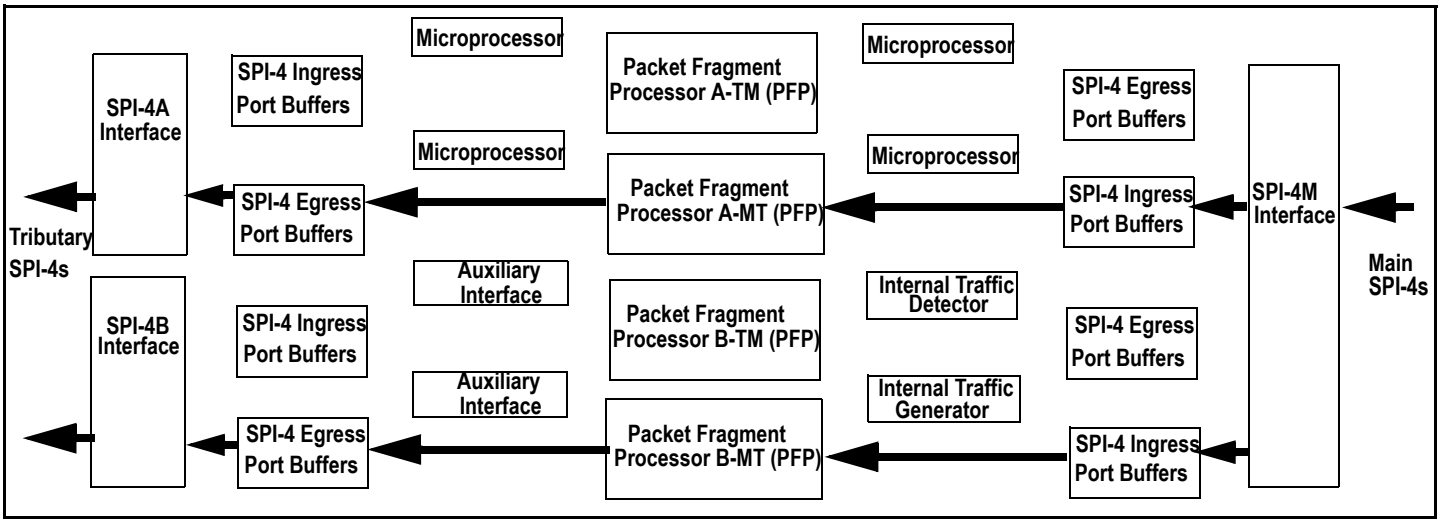


Figure 10 SPI-4 main to SPI-4 Tributary Data Path

PFP loop data path is sending data from PFP-A back to PFP-A or sending data from PFP-B back to PFP-B as shown in Figure 11 PFP Loop Data Path p.37.

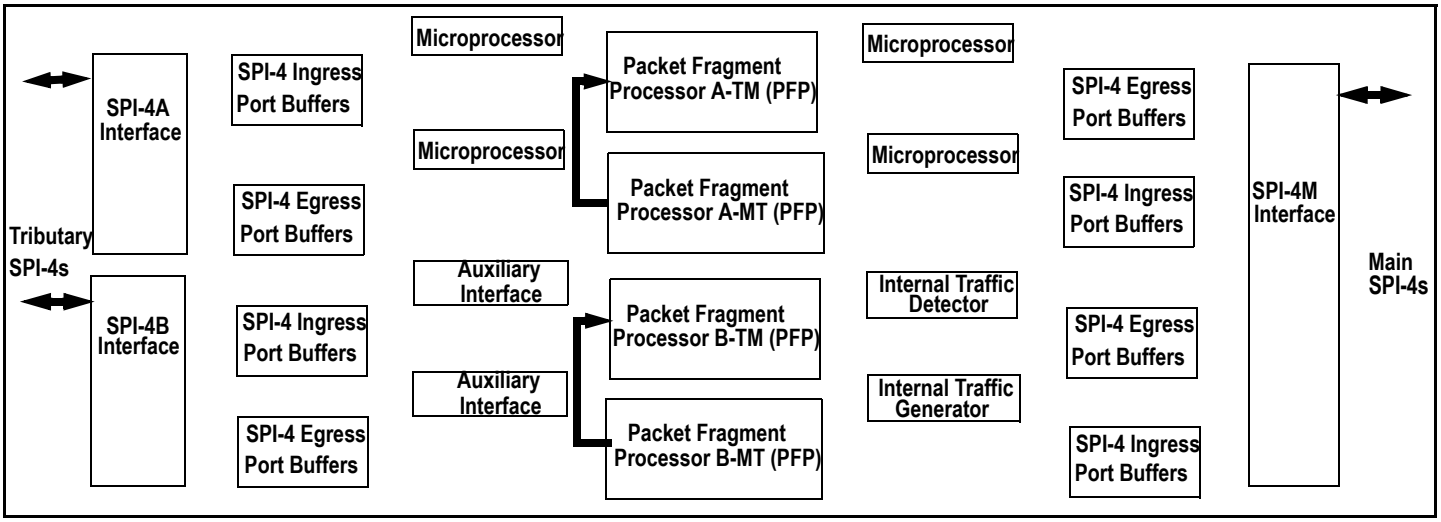


Figure 11 PFP Loop Data Path

Figure 12 Microprocessor, Auxiliary and Internal Traffic Detector/Generator Data Path p.38 describes the following data paths:

- Microprocessor data path is sending data from/to microprocessor interface to/from PFP-A.

- Auxiliary data path is sending data from/to Auxiliary interface to/from PFP-B.

- Internal traffic generator / detector data path is sending data from Internal Traffic Generator to PFP-B and from PFP-B to Internal Traffic Detector. The Internal Traffic Generator and the Internal Traffic Detector both use a Pseudo Random Bit Sequence (PRBS) pattern.

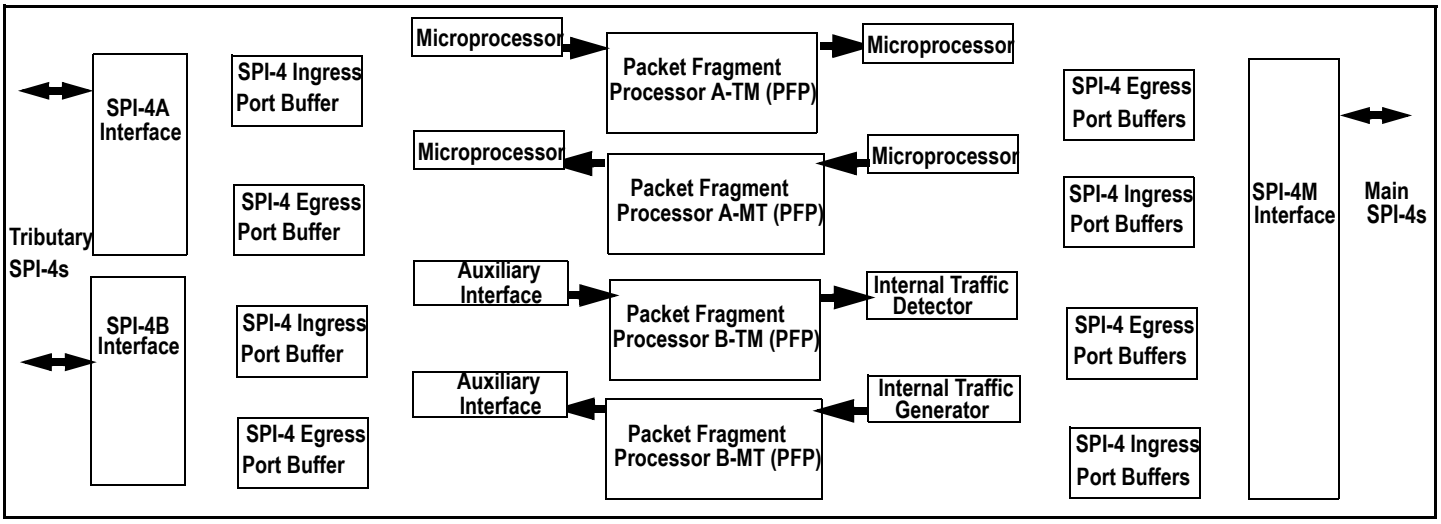


Figure 12 Microprocessor, Auxiliary and Internal Traffic Detector/Generator Data Path

PFP redirect data path conveys data from PFP-A to PFP-B or from PFP-B to PFP-A as shown in Figure 13 PFP Redirect Data Path p.38.

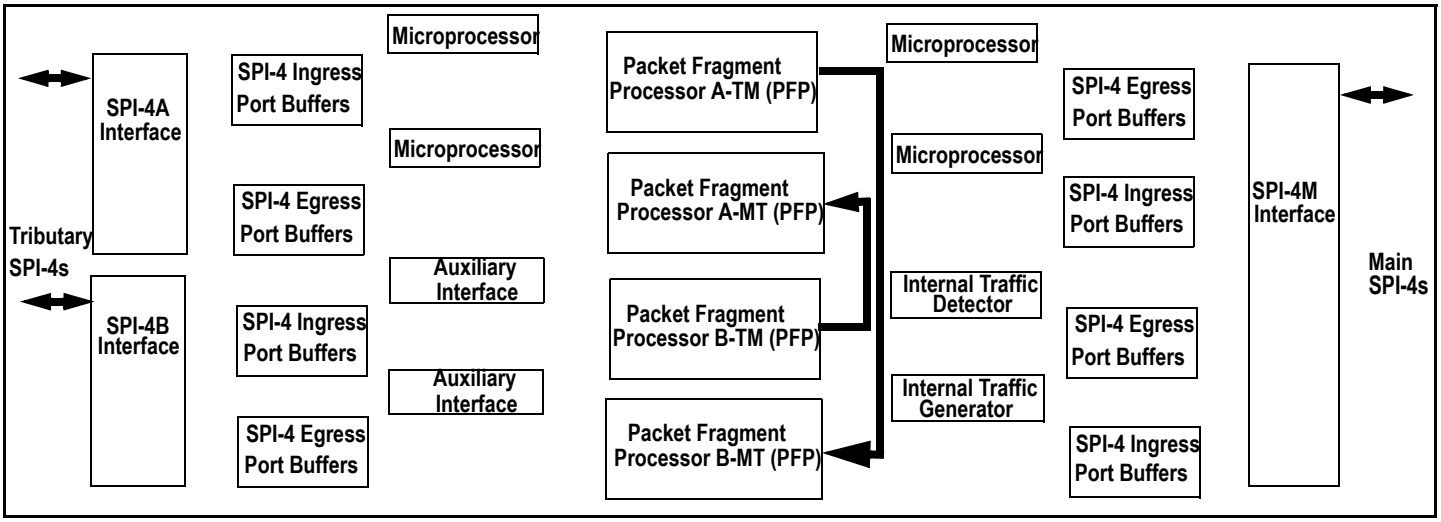


Figure 13 PFP Redirect Data Path

External Interfaces

The external interfaces provided on the IDT88K8483 device are three SPI-4 interfaces, SPI-4A, SPI-4B and SPI-4M, an interface to either a FPGA or a QDR-II bus, a pin-selectable serial or parallel microprocessor interface, a JTAG interface, and five general purpose input or output (GPIO) pins. The following information contains a set of the highlights of the features supported from the relevant standards, and a description of additional features implemented to enhance the usability of these interfaces for the system architect.

SPI-4A AND SPI-4B

Refer to the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1) for full details.

- *Two instantiations of the SPI-4 interface*
- *Clock rate is 77.76 - 450 MHz DDR*
- *Link and PHY interfaces are supported*
- *Logical port address range of 0 – 255 with support for between 1 and 64 simultaneously active logical ports*
- *MAXBURST parameters configurable from 16 to 256 bytes in 16 byte multiples*
- *256-entry FIFO status calendar*
- *Quarter-clock-rate LVTTL, or full-rate LVDS FIFO status signals are selectable per SPI-4 port*

SPI-4M

Refer to the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1) for full details.

- *One instantiation of the SPI-4 Main interface*
- *Clock rate is 87 - 450 MHz DDR*
- *Link and PHY interfaces are supported*
- *Logical port address range of 0 – 255 with support for between 1 and 128 simultaneously active logical ports*
- *MAXBURST parameters configurable from 16 to 256 bytes in 16 byte multiples*
- *256-entry FIFO status calendar*
- *Quarter-clock-rate LVTTL, or full-rate LVDS FIFO status signals are selectable per SPI-4 port*

FPGA INTERFACE

The FPGA interface is shared with the QDR-II interface. Selecting the FPGA interface enables the following features:

- *Clock rate is 160 - 200 MHz DDR source-synchronous*
- *Logical port address range of 0 – 63 with support for 64 simultaneously active logical ports*
- *DDR HSTL logic levels*

QDR-II INTERFACE

The QDR-II interface is shared with the FPGA interface. Selecting the QDR-II interface enables the following features:

- *Clock rate is 160 - 200 MHz QDR-II*
- *Up to 18 Mbit of QDR-II memory is supported*
- *QDR-II HSTL logic levels*

MICROPROCESSOR INTERFACE

Parallel microprocessor interface:

- *Eight bit data bus*
- *Six bit address bus*
- *Pin-selectable Intel or Motorola control signals*
- *Direct accessed space used for quick interrupt processing*
- *Expanded indirect access space used for provisioning*
- *Read operations to a reserved address or reserved bit fields return 0*
- *Write operations to reserved addresses or bit fields are ignored*

Serial microprocessor interface:

- *Compliance to Motorola Serial Peripheral Interface (SPI) specification*
- *Byte access*
- *Direct accessed space used for quick interrupt processing*
- *Expanded indirect access space used for provisioning*
- *Read operations to a reserved address or reserved bit fields return 0*
- *Write operations to reserved addresses or bit fields are ignored*

JTAG

- *Complies with the IEEE 1149.1 standard.*

GPIO

- *Three GPIO signals are provided. Each signal may be independently defined as an input or an output pin.*
- *The GPIO interface allows flexible use of the GPIO pins. The following can be defined per GPIO pin:*

  Direction: input or output

  Level: value to write if programmed to be an output, or value that is being read if programmed to be an input

SPI-4 Interface

Overview

SPI-4.2 as originally defined is an interface for packet and cell transfer between a physical layer (PHY) device and a link layer device (network processor), for aggregate bandwidths of OC-192 ATM and Packet over SONET/SDH (POS), as well as 10 Gb/s Ethernet applications. The SPI-4.2 protocol transfers data in variable length bursts. Associated with each burst is information such as logical port number (for a multi-port device such as a 10 x 1 GbE MAC), SOP, EOP. This information is collected by the SPI-4 interface and passed to the PFPs. The Optical Internetworking Forum (OIF) controls the SPI-4.2 Implementation Agreement document (available at http://www.oiforum.com).

The SPI-4 interface power down mode has to be disabled before configuring the interface. The SPI-4 interface also has to be configured before the interface is enabled. The SPI-4 interface LVDS outputs (except for the clock) can be powered down by setting to 1 the SPI4_PDN field in the SPI-4 Interface Enable Register (p. 106). The interface is enabled by setting to 1 the SPI4_EN field in the SPI-4 Interface Enable Register (p. 106).

The SPI-4 interface consists of separate ingress and egress interfaces as described in Figure 14 IDT88K8483 SPI-4 Connections Example p.42. The ingress and egress ports are unidirectional and independent of each other. Each port has 16 data signals, a clock, and a control signal, all of which use LVDS (differential) signaling, and are sampled on both edges of the clock. There are also ingress status port and egress status port. Each status port has 2 fifo status signals and a clock. The status port signal can be configured to LVDS (differential) or LVTTL by the status channel control pin LVDSSTA (SPI4A_LVDSSTA, SPI4B_LVDSSTA, SPI4AM_LVDSSTA). The ingress port supports dynamic alignment, and the egress port supports programmable skew.

The IDT88K8483 has three SPI-4 interfaces: one main SPI-4 interface (M) and two tributary SPI-4 interface (A and B). Each tributary SPI4 interface supports up to 64 logical ports. The main SPI4 interface supports up to 128 logical ports. The logical port in-band address are from 0 to 255.

The clock source for the SPI-4 ingress port is the SPI-4 interface input clock IDCLK (SPI4A_IDCLK_P, SPI4A_IDCLK_N, SPI4B_IDCLK_P, SPI4B_IDCLK_N, SPI4M_IDCLK_P and SPI4M_IDCLK_N). The source clock for the SPI-4 egress port is the internal SPI-4 clock generator.

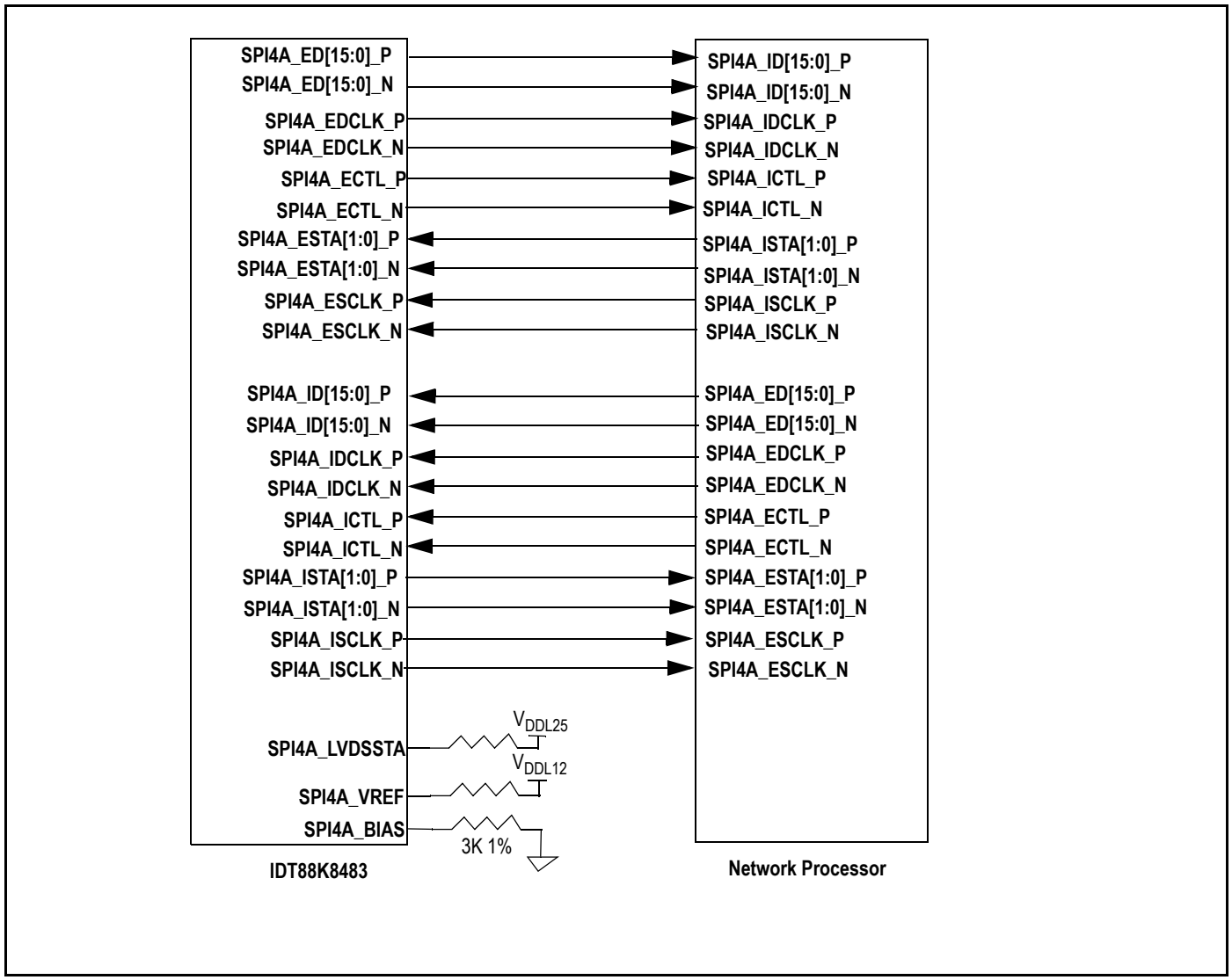


Figure 14 IDT88K8483 SPI-4 Connections Example

SPI-4 Ingress Data Channel

The SPI-4 ingress data channel is independent from the status channel. The data channel supports bit alignment and de-skew, error event detection and transfer termination. The status channel generates status frame, and controls the output skew per lane.

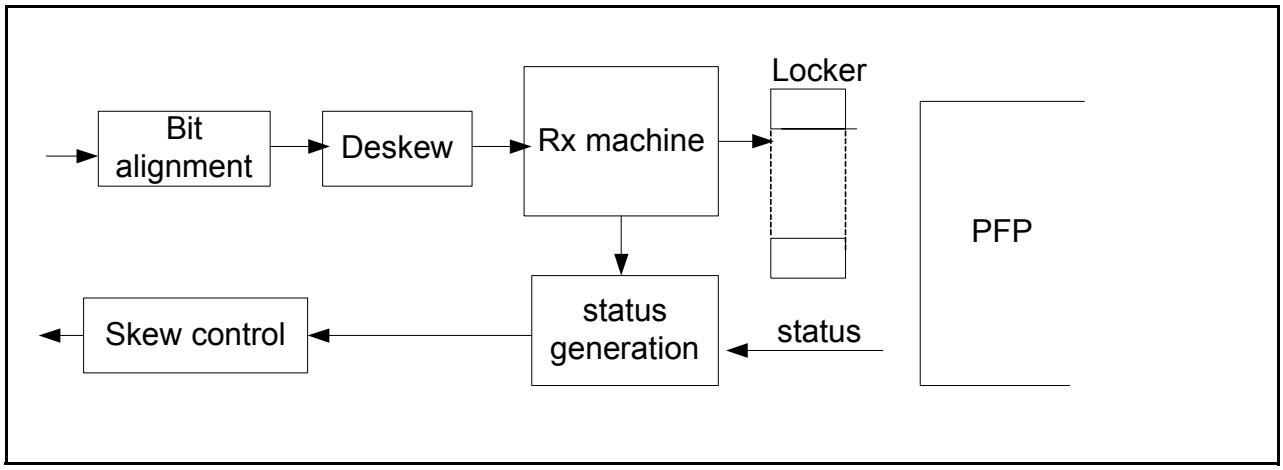


Figure 15 SPI-4 Ingress Block Diagram

Bit alignment

The bit alignment block is responsible for data and clock alignment. The bit alignment allows the clock to be used for correct data sampling and eliminate bit errors by providing adequate set-up and hold time margins.

The alignment selection is programed by AUTO_ALIGN field in the SPI-4 Ingress Automatic Alignment Control Register (p. 109). The device is responsible for an edge transition histogram for each lane (lane is defined as a deferential pair of data, control or status signals). The data is sampled by 10-phased-shifted clock during each clock cycle. Each 2 consecutive sampled values are XORed and accumulated during a fixed observation window to generate transition edge histogram.

The measurement histogram is triggered by writing to the LANE field in the SPI-4 Histogram Measure Launch Register (p. 117). The measurement process is indicated by the BUSY field in the SPI-4 Histogram Measure Status Register (p. 117). The BUSY field is set to 1 when a measurement is launched. The BUSY field is auto cleared to 0 when the measure is finished. The received bit stream is selected from the 10 samples. The tap selection is made automatically and is available in the TAP_SEL field in the SPI-4 Bit Alignment Result Register (p. 118).

The bit alignment sequence automatically carried out in the device as follows:

- Write lane number in the LANE field in the SPI-4 Histogram Measure Launch Register (p. 117).

- Poll the BUSY field in the SPI-4 Histogram Measure Status Register (p. 117). If BUSY is 0, then read the C[n] field in the SPI-4 Histogram Counter Register (p. 117) which indicates the counter value. The counter value is used to select the tap.

- Write the selected Tap value to TAP field in the SPI-4 Bit Alignment Result Register (p. 118).

De-skew

The De-skew block is responsible for alignment between the data signals. The De-skew block can de-skew +/-1bit. For diagnose purpose, an out of range offset between lines is provided. If the skew is more than 2 bits, then the I_DSK_OOR field in the SPI-4 Ingress Status Register (p. 108) is set. The I_DSK_OOR field is cleared when the offset is in range.

Receive State Machine

The ingress data channel has 2 states, IN_SYNCH and OUT_OF_SYNCH. The machine transitions from OUT_OF_SYNCH to IN_SYNCH if a number of consecutive error-free DIP-4 are detected. The number is configured by using the SPI-4 Ingress Configuration Register (p. 106). The machine stays in OUT_OF_SYNCH state if the interface is not enabled.

The status of the synchronization is indicated by I_SYNCV field in the SPI-4 Ingress Status Register (p. 108). Any transition on I_SYNCV will be captured by the PMON Event Interrupt Indication Register (p. 136). An interrupt is generated if interrupt options is enabled. The data channel synchronization status is fed to status channel generation logic for handshaking.

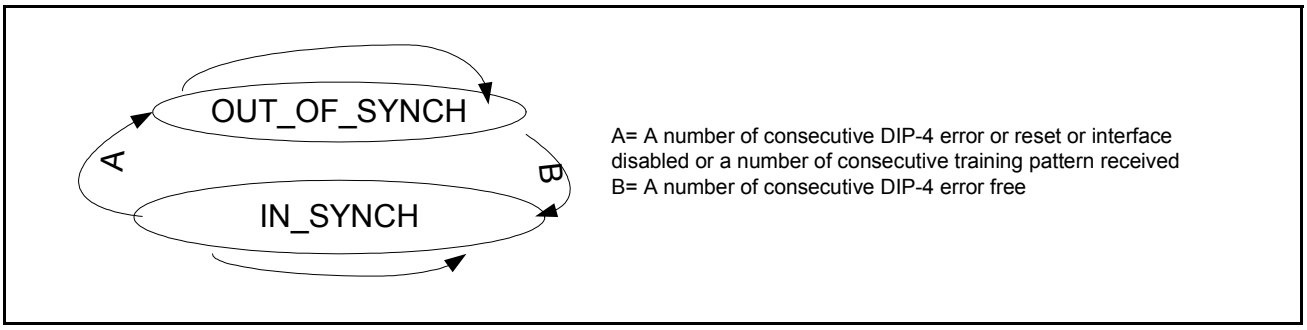


Figure 16 SPI-4 Ingress State Machine

The bus word may be payload data word, payload control word, idle control word or training word. It is classified by the CTL input signal and the content of the control field.

The DIP fields of the control word previous and subsequent payload data or training data are subjected to DIP checking. DIP checking is performed both in IN_SYNCH and OUT_OF_SYNCH state. In IN_SYNCH state, each DIP error generates a DIP-4 error event. This event is captured and forward to PMON.

The logical port information is carried in the payload control word. The following data words are associated with this logical port. The LP to LID mapping is defined by the SPI-4 Ingress LP to LID Mapping Table (p. 105). Transfers for inactive LPs are flushed, and an ingress inactive logical port event generates. The event and the associated logical port are forwarded to PMON. For each active logical port, data word, SOP, EOP, abort tag and length are put into associated ingress port buffer. For statistics purpose, the number of transfers and bytes are forwarded to PMON.

Multiple logical ports can not be mapped to the same LID. The logical port can not remapped in the IN_SYNCH state.

Errors handling scheme:

When a DIP4 error is received in the in IN_SYNCH state, a DIP4 error event is generated and an error tag is added to the packets being received.

When a reserved control word is received, a bus error event is generated and the control word is ignored.

When consecutive payload control words are received, a bus error event is generated and every control word is ignored except the last received.

When payload is received following an idle control word, a bus error event is generated.

When a transfer belonging to an inactive LP is received, an inactive transfer event is generated and the transfer is dropped.

When an unaligned transfer is received, a bus error event is generated.

SPI-4 Ingress Associated Status Channel

Status Generation

The device supports both LVTTL and LVDS status channel mode. The status mode (LVDS/LVTTL) is configured by LVDSSTA (SPI4A_LVDSSTA, SPI4B_LVDSSTA and SPI4M_LVDSSTA) pin. The level of the LVDSSTA pin is reflected by LVDS_STA field in the SPI-4 Ingress Status Register (p. 108).

When the device is in LVTTL status mode, and if ingress data channel is out of sync, it sends all '11'. When the device is in LVDS status mode, and if ingress data channel is out of sync, it sends training pattern. When the device is in sync, it sends calendar frame or period training. They are switched at the frame boundary.

The device supports one or two sets of calendars. If I_CSW_EN field in the SPI4 Ingress Calendar Switch Control Register (p. 109) is set to 1, then two sets of calendars are used. In this mode, a calendar selection word must be received immediately after the framing word for correct operation.

If CAL_SEL field in the SPI4 Ingress Calendar Switch Control Register (p. 109) is cleared to 0, then the device selects calendar 0 and the selection word is fixed to 01b. If CAL_SEL field in the SPI4 Ingress Calendar Switch Control Register (p. 109) is set to 1, then the device selects calendar 1, and the calendar selection word is fixed to 10b.

If the I_CSW_EN field is cleared to 0, then the DIP-2 is computed over all preceding status indications after the last '11' framing pattern.

If I_CSW_EN is set to 1, and I_DIP_CSW is set to 1, then the DIP-2 is computed over calendar selection word and all preceding status indications after last '11' framing pattern.

If I_CSW_EN is set to 1, and I_DIP_CSW is set to 0, then the DIP-2 is computed over all preceding status indications after last '11' framing pattern and excluding the calendar selection word.

The starving, hungry or satisfied indication for each status word for each logical port is based on the status from the PFP and the SPI-4 ingress port buffer fill level. See SPI-4 Ingress WATERMARK Register (p. 111).

The calendar length is configured by the I_CAL_LEN field in the SPI-4 Ingress Calendar 0 Configuration Register. (p. 107) while calendar length=I_CAL_LEN+1. In LVTTL mode, the I_CAL_LEN field can be programmed to any value. In LVDS mode, the I_CAL_LEN field must be programmed to 4n-1 (n is an integer).

Output Skew

The LVDS output lane skew is adjustable in order to provide greater flexibility for board layout. The clock outputs can be skewed over a range of 0 to 0.9 clock cycles with a resolution of 0.1 clock cycle. The data outputs can be skewed over a range of 0 to 0.3 clock cycle with a resolution of 0.1 clock cycle. The skews are controlled by the output delay registers.

Diagnostics Features

- Ingress data channel clock detect. The ingress data clock IDCLK (SPI4A_IDCLK_P, SPI4A_IDCLK_N, SPI4B_IDCLK_P, SPI4B_IDCLK_N, SPI4M_IDCLK_P, and SPI4M_IDCLK_N) is monitored. If there is no transition on IDCLK in a 2048 MCLK hopping window, then the DCLK_AV field in the SPI-4 Ingress Status Register (p. 108) is cleared to 0. The DCLK_AV flag transition from 1 to 0 generates an event towards the PMON, and the PMON captures this event.

- Ingress port buffer unavailable. If there is more data but no port buffer available, then the device discards the data, generates a SPI_4 port buffer unavailable event, and forwards the event to PMON.

- DIP-2 error insertion. A number of consecutive (less then 16) DIP-2 errors can be generated. The number of errors is configured by the DIP_E_NUM field in the SPI-4 Ingress Diagnostics Register (p. 109). When the I_ERR_INS field in the SPI-4 Ingress Diagnostics Register (p. 109) is set to 1, it triggers error insertion using the I_DIP_NUM field value. The I_ERR_INS field is self cleared when the correct number of errors is generated. The I_DIP_NUM field value is not changed by device.

- Force continuous training. The status channel generates continuous training pattern in LVDS protocol if I_FORCE_TRAIN field in the SPI-4 Ingress Diagnostics Register (p. 109) is set to 1. The status channel generates a continuous '11' pattern in LVTTL protocol if I_FORCE_TRAIN field is set to 1.

- Ingress port buffer fill level. The ingress port buffer fill level is indicated in the FILL_CURR field in the SPI-4 Ingress Fill Level Register (p. 110). The maximum port buffer fill level is configured by using the FILL_MAX field in the SPI-4 Ingress Training to out of sync threshold Register (p. 111).

SPI4 egress Data Channel

The SPI4 egress interface has data channel and status channel. The data channel carries transfers, and the status channel carries status. The output skew is per lane controllable. The status channel does bit alignment and de-skew in LVDS mode. The device receives status frame for controlling the data path flow. In packet mode, the TX machine must transmit a complete packet before it starts a transfer for another logical port.

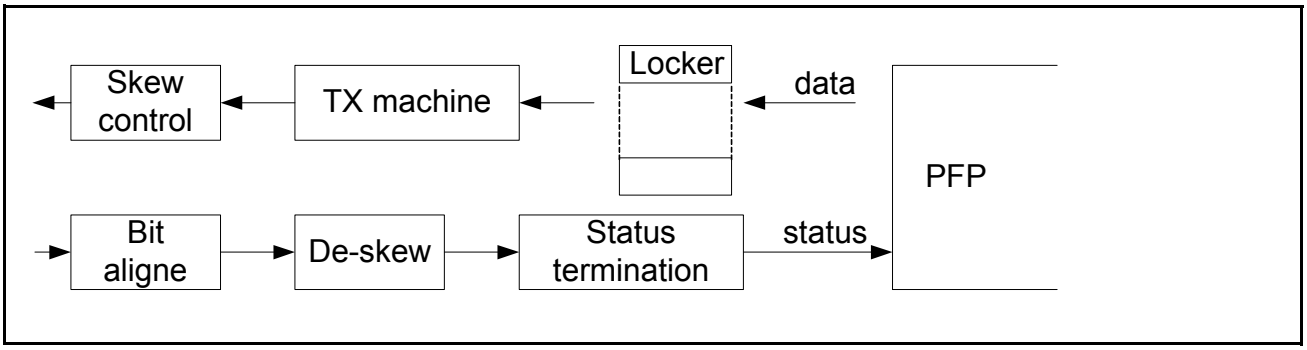


Figure 17 SPI-4 Egress State Block Diagram

Tx Machine

Control words are inserted only between the transfers. Once a transfer has begun, the data words are sent uninterrupted until a whole transfer is complete. The interval between the end of a given transfer and the next payload control word consists of zero or more idle control words and training patterns. Successive SOP must occur not less than 8 cycles apart. Figure 18 Egress word transition state machine p.46 shows the word transition on the interface. The adjacent device that generates the transfer have to meet the requirements as described in Figure 18 Egress word transition state machine p.46.

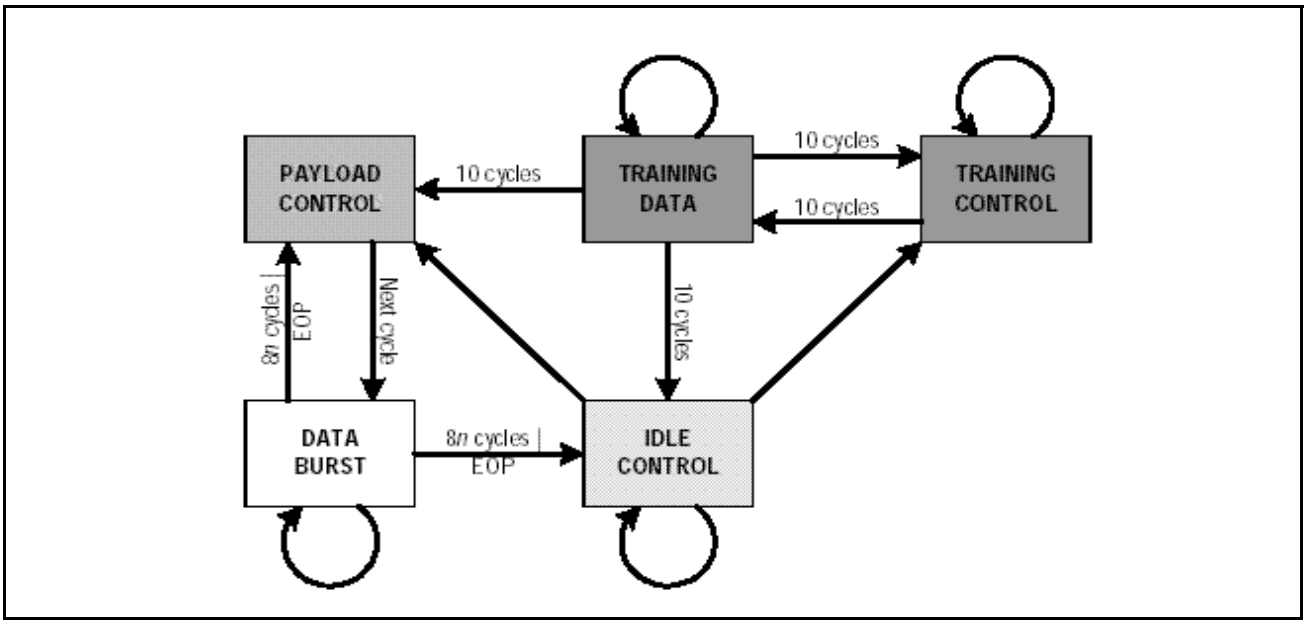


Figure 18 Egress word transition state machine

The SPI-4 interface loads data and overhead from the egress port buffer and generates transfer. The cycle to cycle behavior is described in Figure 18 Egress word transition state machine p.46. The number of idle control words between transfers is less than or equal to 4 if there is data for transmit. The LID to logical port mapping is configured by SPI-4 Ingress Training to out of sync threshold Register (p. 111). Multiple LID can not be mapped to the same logical port. LID can not be remapped in the IN_SYNCH status.

Packet mode and cut through mode selection is defined in PFP. The main SPI-4 transmit data from module A/B in round robin. In cut-through mode, the unit is one transfer, while In packet mode, the unit is one packet.

If only one byte of the SPI-4 16 bit wide data is valid, then 8 LSB (B7 to B0) are fixed to 0.

Egress associated status channel

Bit alignment

The alignment selection is programed by AUTO_ALIGN flag in the SPI-4 Egress Automatic Alignment Control Register (p. 115).

The device is responsible for edge transition histogram for each lane. The data is sampled by 10-phased shifted clock during each clock cycle. Each consecutive pairs of sampled values are XORed and accumulated during a fixed observation window to generate transition edge histogram.

The measure histogram is triggered by writing to the LANE field in the SPI-4 Histogram Measure Launch Register (p. 117). The measurement process is indicated by a BUSY flag in the SPI-4 Histogram Measure Status Register (p. 117). The BUSY field is set to 1 when a measurement is launched. The BUSY field is auto cleared to 0 when the measurement is finished. The status channel TAP is configured by the AUTO_ALIGN field in the SPI-4 Egress Automatic Alignment Control Register (p. 115).

The bit alignment sequence is as follows:

- Write lane number in the LANE field in the SPI-4 Histogram Measure Launch Register (p. 117).

- Poll the BUSY field in the SPI-4 Histogram Measure Status Register (p. 117). If BUSY is 0, then read the C[n] field in the SPI-4 Histogram Counter Register (p. 117) which indicates the counter value. The counter value is used to select the tap.

- Write the selected Tap value to TAP field in the SPI-4 Bit Alignment Result Register (p. 118).

De-skew

The De-skew block can de-skew +/-1bit. For diagnostic purpose, an out of range offset between lines is provided. If deskew is more than 2 bits, then the E_DSK_OOR field in the SPI-4 Egress Status Register (p. 115) is set. E_DSK_OOR field is cleared when in range.

Status Termination

The protocol (LVDS/LVTTL) is configured by SPI4_LVDSSTA input pin. The status channel has 2 states, IN_SYNCH and OUT_OF_SYNCH. A number of consecutive DIP-2 error-free values cause a transition from OUT_OF_SYNCH to IN_SYNCH state. This number is configured by SPI-4 Egress Configuration Register (p. 113). A number of consecutive DIP-2 errors will force the machine to OUT_OF_SYNCH state. This number is configured in the SPI-4 Egress Configuration Register (p. 113). In LVDS protocol mode, 12 consecutive “11” will force the machine to OUT_OF_SYNCH state. In LVTTL protocol mode, 12 consecutive ‘11’ will force the machine to OUT_OF_SYNCH state. The machine’s state is indicated by E_SYNCV field in the SPI-4 Egress Status Register (p. 115). Any transition on the E_SYNCV field is captured, and generates an interrupt if enabled.

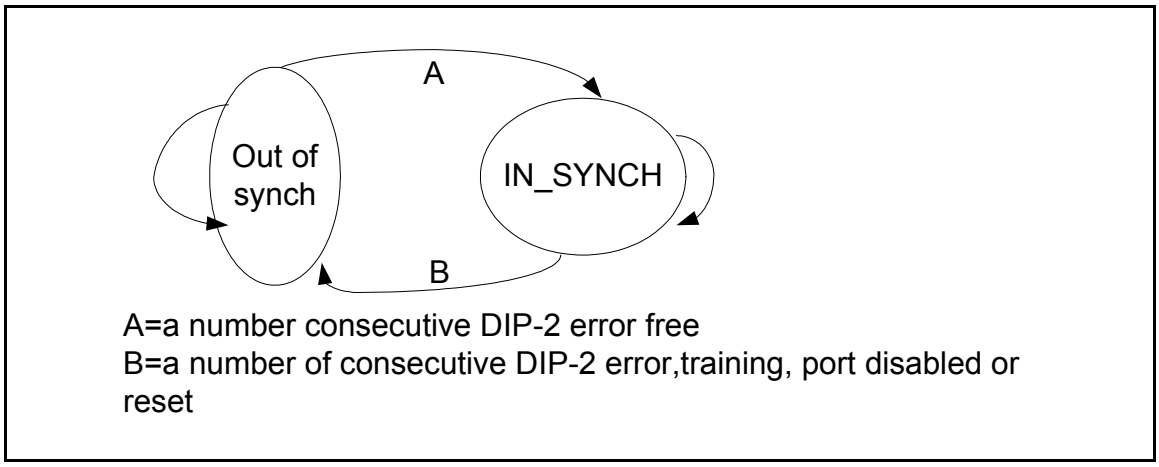


Figure 19 Status Channel State Machine

The device supports one or two sets of calendars. If E_CSW_EN field in the SPI-4 Egress Calendar Switch Control Register (p. 116) is set to 1, then two sets of calendars mode are used. In this case, a calendar selection word must be placed following the framing bit.

If CAL_SEL field in the SPI-4 Egress Calendar Switch Control Register (p. 116) is cleared to 0, then the device selects calendar 0, and the selection word is fixed to 01b. If CAL_SEL field is set to 1, then the device selects calendar 1, and the selection word is fixed to 10b.

If the E_CSW_EN field is cleared to 0, then the DIP-2 is computed over all preceding status indications after last '11' framing pattern. If E_CSW_EN field is set to 1, and E_DIP_CSW field is set to 1, then the DIP-2 is computed over calendar selection word and all preceding status indications after last '11' framing pattern. If E_CSW_EN field is set to 1, and E_DIP_CSW field is set to 0, then the DIP-2 is computed over all preceding status indications after last '11' framing pattern, excluding the calendar selection word.

In IN_SYNCH state, each DIP-2 error generates a DIP-2 error event towards to PMON. A single DIP-2 error sets all calendar LP's status to 'satisfied'. In IN_SYNCH state, the status is updated per cycle rather than updated all LP at the end of the frame. In OUT_OF_SYNCH state, the calendar' LP's status are fixed to 'satisfied'. In the two-calendar modes, the MSB of calendar ID is extracted to CAL_ID field in SPI-4 Egress Calendar Switch Control Register (p. 116). The CAL_ID field does not change in single calendar mode or in out of sync state.

The calendar length is configured in the E_CAL_LEN field in the SPI-4 Egress Calendar 0 Configuration Register (p. 114). In LVTTL mode, the E_CAL_LEN field can be programmed with any value. In LVDS mode, the E_CAL_LEN field must be programmed with 4n-1 (n is an integer).

No status channel option

There is an option to configure the device to no status channel mode by the NO_STAT field in the SPI-4 Egress Configuration Register (p. 113). In No status mode, the Egress synchronization is fixed at out of sync, there is no DIP-2 error check, and per LP status is fixed to 'starving'.

Diagnose features

- Egress status channel clock detect. If there is no transition on MCLK clock in a 2048 MCLK hopping window, then the SLCK_AV field in the SPI-4 Egress Status Register (p. 115) is cleared to 0. The SLCK_AV field transition from 1 to 0 generates an event forward to PMON. In LVDS I/O mode, the device detects "no transition" on the LVDS input clock.

- DIP-4 error insertion. A number of consecutive (less than 16) DIP-4 errors can be generated. The number of error is configured by the E_DIP_NUM field in the SPI-4 Egress Diagnostics Register (p. 115). When the E_ERR_INS field in the SPI-4 Egress Diagnostics Register (p. 115) is set to 1, error insertion is triggered using the E_DIP_NUM field value.The E_ERR_INS field is self cleared when the correct number of errors is generated. The E_DIP_NUM field value is user-configured and is not changed internally.

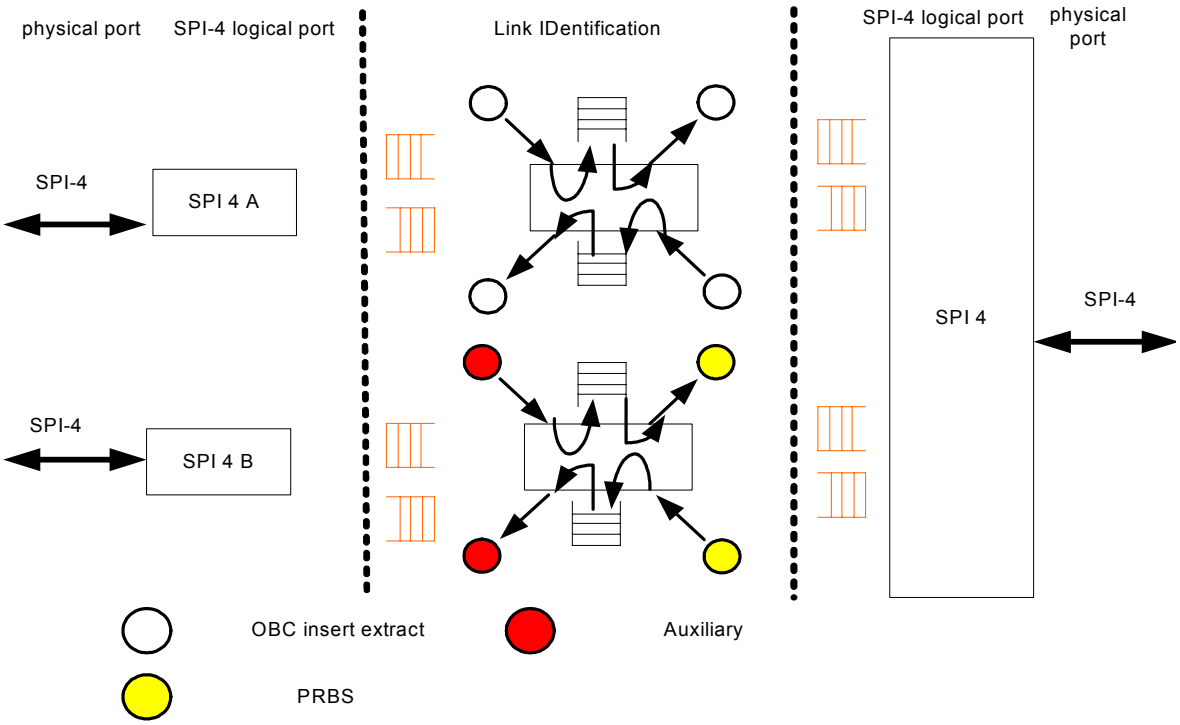
- Force continuous training. The data channel generates continuous training pattern if E_FORCE_TRAIN field in the SPI-4 Egress Diagnostics Register (p. 115) is set to 1.

- Egress port Buffer fill level. The egress Port Buffer fill level is indicated in the FILL_CUR field in the SPI-4 Egress Fill Level Register (p. 116). The maximum port buffer fill level is configured by using the FILL_MAX field in the SPI-4 Egress Max Fill Level Register (p. 116).

Insert and Extract paths

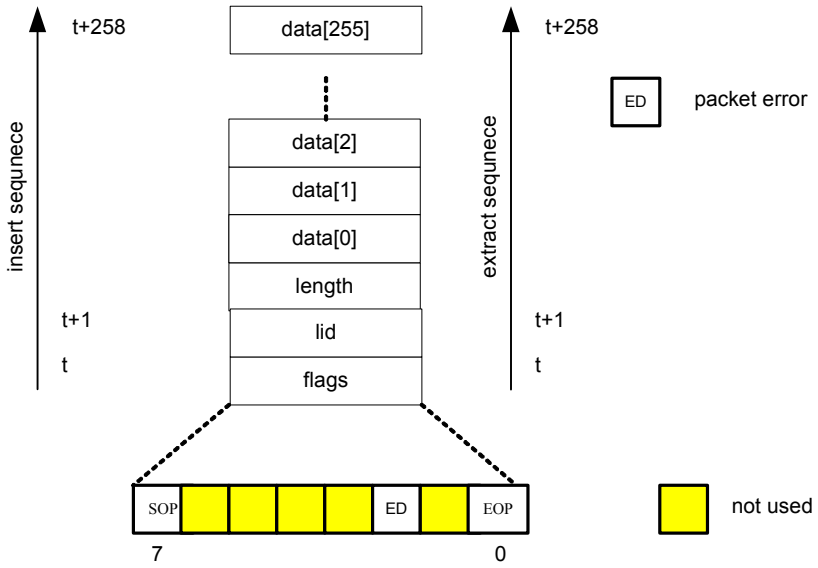
OBC insert/extract path

A useful feature for diagnostics is the OBC (On Board Controller) insert and extract path.



The OBC insert and extract paths are provided on both directions of the packet fragment processor A. They are intended for low bandwidth communications channels like operation administration, maintenance functions etc. The OBC insert, inserts packets into the SPI4 stream via the OBC insert locker which is 256 bytes and packets from the SPI4 stream can be extracted via the OBC extract locker which is 256 bytes. Both insertion and extraction can be done on both side of PFP-A.

The format for PFP insertion is as depicted in the following figure.



OBC insert

The first byte indicates the SOP or EOP and also whether the packet is error tagged or not by writing into the ED bit. The second byte is the lid information, which tells the OBC controller, which lid the packet goes to. The 3rd byte is the length of the packet in bytes. After this overhead is written, the packet is written into the OBC insert locker, not to exceed 256 bytes. If the packet length exceeds 256 bytes, then the first 256 bytes is written into the locker, transferred to the PFP and when the locker is empty, the remaining bytes of the packet is written into the insert locker. The pseudo code is given below.

```
Begin: Is {packet_length > 256}
if yes {set flag = (SOP = 1 << 7) || (EOP = 0)} else {set (SOP = 1 << 7) || (EOP = 1)}
if yes {set length = 256} else { set length = packet_length}
Direct Read DATA_AVAILABLE flag in PFP T-M insert control register (Register Offset=0x0) (p. 96) // Availability of OBC insert FIFO
if {result = 0}
   write flag into PFP T-M insert data register(Register Offset=0x1) (p. 97)
   write lid_number to PFP T-M insert data register(Register Offset=0x1) (p. 97)
   write length to PFP T-M insert data register(Register Offset=0x1) (p. 97)
   write packet_data to PFP T-M insert data register(Register Offset=0x1) (p. 97)    //if length >256, write 256 bytes in run1.
   write 0x1 to PFP T-M extract control register (Register Offset=0x2) (p. 97)      // to launch data. This causes data to be read into the PFP and
                                                                                    //clear the FIFO and setting the DATA_AVAILABLE bit to 0.
if {packet_length>256} {
set remaining_length = packet_length - 256
set packet_length = remaining_length
goto Begin
}
```

OBC extract

The OBC extract process also works in the same way. The OBC extract FIFO can hold up to 256 bytes of data. The registers used in this process are PFP T-M extract control register (Register Offset=0x2) (p. 97) and PFP T-M extract data register (Register Offset=0x3) (p. 97). The pseudo code for the extract process is as follows

```
Begin:
Direct read PFP T-M extract control register (Register Offset=0x2) (p. 97)
if {result = 0} return    // result = 0Indicates that the OBC extract FIFO is empty
  else
Read 39
set EOP=result && 0x01     // the first bit of the first byte read indicates whether packet in the extract FIFO is>256 bytes.
Read PFP T-M extract data register (Register Offset=0x3) (p. 97)  // The second byte gives the LID info
Read PFP T-M extract data register (Register Offset=0x3) (p. 97)  // The 3rd byte gives the length of the packet stored in the FIFO
for {i=0} {i<length} {i++} {
   Read PFP T-M extract data register (Register Offset=0x3) (p. 97)  // Read the packet data till the length specified
}
write 0x0 to PFP T-M extract control register (Register Offset=0x2) (p. 97)   // to clear the extract FIFO.
if {EOP != 1} goto Begin
```

Packet Fragment Processor (PFP)

Overview

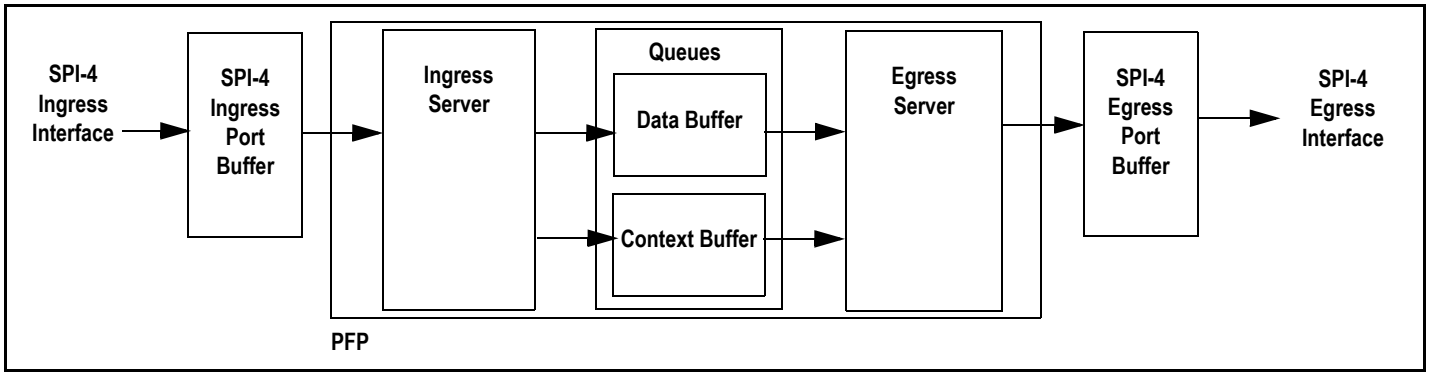


Figure 20 PFP Block Diagram

The Packet Segment Pool (PFP) is an internal block which is used for queuing and scheduling. There are four PFPs in the device - one for each SPI-4 tributary port and direction: PFP module A tributary to main (PFP-A-MT), PFP module A main to tributary (PFP-A-MT), PFP module B tributary to main (PFP-B-MT) and PFP module B main to tributary PFP-B-MT. The PFP includes the ingress server, queues and egress server as described in Figure 20 PFP Block Diagram p.52. The queues include two types of buffers: data buffer and context buffer. The data buffer stores the payload and the context buffer stores the payload location in the data buffer. For each PFP, the content buffer has 4K entries which are equal assigned between the LIDs. For each PFP, the data buffer has 127K bytes, which are divided into 508 segments of 256 bytes. M field in the PFP Buffer Segment Assign Table (p. 120) configures the number of segments in the data buffer for each LID.

The PFP can be programed to over-booking mode by setting to 1 the OVBK_EN field in the PFP Buffer Management Configuration Register (p. 123). In non over-booking mode, the segments allocation is static, and the data buffer space is not shared between the LIDs, so the maximum number of segments for each LID is M. In over booking mode, the segment allocation is dynamic, and the data buffer space can be overlapped between the LIDs, so the maximum number of segments for each LID is up to 8 times the value of M segments, depending on how much the other LIDs are occupied. In over- booking mode, it is recommended that back-pressure is not used at the PFP egress in order to avoid deadlock. When using over-booking mode, the global threshold should be programed in the BUF_THR field in the PFP Buffer Management Configuration Register (p. 123).

The ingress server transfer data from the ingress port buffers to the data buffers. The ingress server sequence is: read ingress port buffer, request data buffer segment, move data to data buffer and put the payload location information in the context buffer. The ingress server checks the SOP/EOP sequence. If the ingress server detects SOP-EOP-EOP sequence or EOP-SOP-SOP sequence, then it sends illegal sequence event to PMON. If the ingress server detects buffer overflow, then it sends over flow event to PMON. If the ingress server detects a too-long packet, then it truncates the packets, adds SOP/EOP and error tag accordingly, and sends cut-down event to PMON. The packet length is programed in the MAX_LEN field in the PFP Maximum Packet Length Register (p. 128).

The egress server is responsible for ensuring that per port quality of service is maintained, and it includes the scheduler which has both round robin priority mode and high/low priority mode. The scheduler schedules segments, or complete packets spanning several segments, from the data buffer to egress port buffer. The device can be programed to priority mode by setting to 1 the WEIGHT_E field in the PFP Queue Weighting Enable Register (p. 124). The LID priority can be programmed to high by setting to 1 the WEIGHT field in the PFP Egress Weight And Direction Register (p. 122). When the priority mode is enabled, the scheduler serves first the high priority segments before the low priority segments. When the priority mode is enabled, if high priority LID receives starving or hungry status from the egress interface, then the device sets the internal LID status to starving and uses the starving maximum burst size (MAX_BURST_S field in the PFP Egress Burst Size Table (p. 122)). When the priority mode is enabled, if low priority LID receives starving or hungry status from the egress interface, then the device sets the internal status to hungry and it uses the hungry max burst size (MAX_BURST_H field in the PFP Egress Burst Size Table (p. 122)).

The egress has four directions: SPI-4 tributary to SPI-4 main or SPI-4 main to SPI-4 tributary, redirect or loopback, extract and discard. The egress direction for each LID is programed in the DIR field in the PFP Egress Weight And Direction Register (p. 122). The egress direction can be programmed on-the-fly, as long as traffic is not present.

The egress also has the flexibility to be programmed for burst or non-burst mode and status or credit mode transfer control. When BURST_EN field in the PFP Flow Control Register (p. 125) is set to 1, the burst mode is enabled, and the same LID can transfer more than one segment of data from the data buffer to the egress port buffer. If the burst mode is not enabled, then the LID can transfer only one segment of data at a time from the data buffer to the egress port buffer, and the PFP can schedule the next segment for the LID only after the current segment has been transmitted. When CREDIT_EN field in the PFP Flow Control Register (p. 125) sets to 1, the credit mode is enabled, and the device uses the LID credit.

The maximum burst size can be configured separately for starving status and for hungry status. The maximum burst size for starving status is configured in the MAX_BURST_S field in the PFP Egress Burst Size Table (p. 122). The maximum burst size for hungry status is configured in the MAX_BURST_H field in the PFP Egress Burst Size Table (p. 122).

The egress can be programmed to interleave packet mode and packet mode. The packet mode for each LID is configured by setting to 1 the PKT_MODE in the PFP Egress Packet Mode Control Registers (p. 123). In interleave mode the scheduler schedules parts of the packet. In packet mode the scheduler schedule the whole packet. When the egress is packet mode, and it receives back-pressure in the middle of sending a packet, it finishes sending the current packet before stalling any subsequent packets queued for transmission.

PFP Flow Control

PFP Ingress Flow Control for non over booking mode

There are 3 main parameters for configuring the SPI-4 ingress flow control for non over booking mode:

- Maximum number of segments per LID is configured in M field in the PFP Buffer Segment Assign Table (p. 120).

- Starving Free segments per LID is configured in THR_STARV field in the PFP Buffer Segment Assign Table (p. 120).

- Hungry Free segments per LID is configured in THR_HUNG field in the PFP Buffer Segment Assign Table (p. 120).

There are three status options per LID in the SPI-4 ingress PFP: starving hungry and satisfied. In SPI-4 ingress PFP for LP0 (for example), in normal operation there are enough free segments, so the LID status is starving, and the SPI-4 ingress interface is sending starving status to the adjacent device through the status bus. When the number of free segments is less than THR_STARV (for example 100 segments), the LID status is changed to hungry, and the SPI-4 ingress interface starts sending hungry status to the adjacent device. When the number of free segments is less than THR_HUNG (for example 50 segments), the LID status is changed to satisfied, and the SPI-4 ingress interface starts sending satisfied status to the adjacent device.

When the number of free segments is again more than THR_HUNG (for example 50 segments), the LID status is changed to hungry, and the SPI-4 ingress interface starts sending hungry status to the adjacent device through the status bus. When the number of free segments is again more than THR_STARV (for example 100 segments), the LID status is changed to starving, and the SPI-4 ingress interface starts sending starving status to the adjacent device.

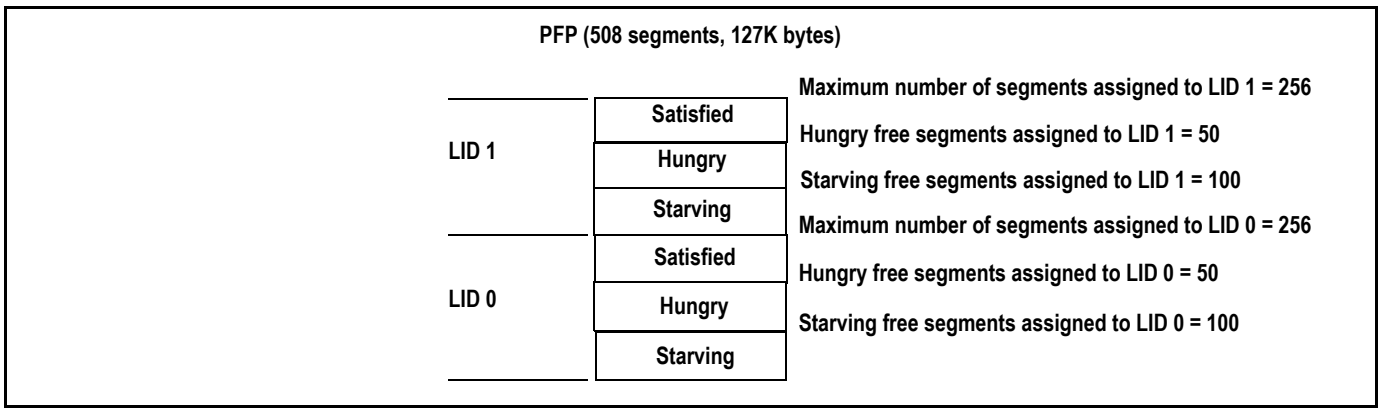


Figure 21 PFP Ingress Flow Control Example

According to the status information from the QDR-II LID, the PFP LID, and the flow control mode the device generates the status indication to the SPI-4 interface as shown in Table 3: “SPI-4 Status Information” (p. 56). The device gets the QDR-II LID status information from the QDR-II interface, and the PFP LID status information from the PFP logic. The device gets the flow control mode from the EBP_EN field in the PFP Egress Packet Mode Control Registers (p. 123). See more information about the PFP/QDR-II flow control in the QDR-II Flow Control (p. 56).

PFP Ingress Flow Control for over booking mode

There are 4 main parameters for configuring the PFP ingress flow control for over booking mode:

- Maximum number of segments per LID is configured in M field in the PFP Buffer Segment Assign Table (p. 120).

- Starving Free segments per LID is configured in THR_STARV field in the PFP Buffer Segment Assign Table (p. 120).

- Hungry Free segments per LID is configured in THR_HUNG field in the PFP Buffer Segment Assign Table (p. 120).

- Global Free segments per LID is configured in the BUF_THR field in the PFP Buffer Management Configuration Register (p. 123).

There are three status options per LID in the SPI-4 ingress PFP: starving hungry and satisfied. In SPI-4 ingress PFP for LP0/LP1 (for example), in normal operation there are enough free segments, so the LIDs status are starving, and the SPI-4 ingress interface is sending starving status to the adjacent device through the status bus. When the number of free segments for each LID is less than THR_STARV (for example 400 segments), the LID status is changed to hungry, and the SPI-4 ingress interface starts sending hungry status to the adjacent device. When the number of free segments for each LID is less than THR_HUNG (for example 300 segments), the LID status is changed to satisfied, and the SPI-4 ingress interface starts sending satisfied status to the adjacent device. When the total number of free segments for all the LIDs is less than BUF_THR (for example 50 segments), the status of all the LIDs are changed to satisfied, and the SPI-4 ingress interface starts sending satisfied status to the adjacent device.

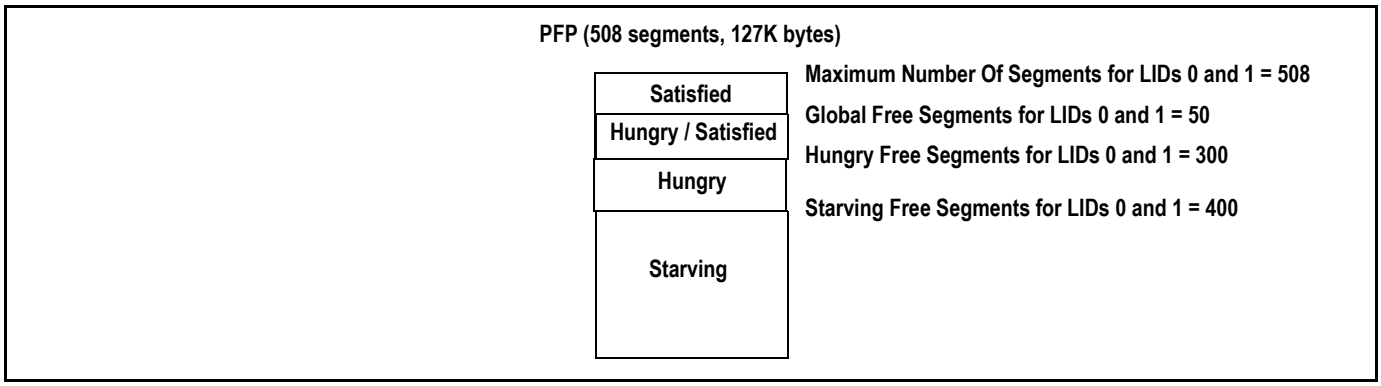


Figure 22 PFP Flow Control Example For Over Booking Mode

Detailed examples:

Example 1. LID0 gets data for 120 segments and LID2 gets data for 120 segments, so LID0 has 392 free segments and LID0 has 392 free segments. In this case, the number of free segments for LID0 is less than THR_STARV (400), so LID0 sends hungry status to the adjacent device. The number of free segments for LID1 is also less than THR_STARV (400), so LID1 sends hungry indication to the adjacent device.

Example 2. LID0 gets data for 220 segments and LID1 gets data for 220 segments, so LID0 has 292 free segments and LID1 also has 292 free segments. In this case, the number of free segments for LID0 is less than THR_HUNG (300), so LID0 sends satisfied status to the adjacent device. The number of free segments for LID1 is also less than THR_HUNG (300), so LID1 sends satisfied indication to the adjacent device.

Example 3. LID0 gets data for 250 segments and LID2 gets data for 250 segments, so the total number of occupied segments for both LID0 and LID1 is 500, and the total number of free segments for both LID0 and LID1 is 12. In this case, the total number of free segments for both LID0 and LID1 is less than BUF_THR (50), so LID0 and LID1 send satisfied status to the adjacent device.

QDR-II Interface

Overview

The auxiliary interface has two modes: QDR-II interface mode and generic interface mode. The auxiliary interface mode (QDR-II or generic) is configured by the MEM field in the Auxiliary Interface Configuration Register (p. 129). The auxiliary interface has to be configured before the interface is enabled. The auxiliary interface outputs (except for the clock) can be powered down by setting to 1 the AUX_PDN field in the Auxiliary Interface Enable Register (p. 129). The interface is enabled by setting to 1 the AUX_EN field in the Auxiliary Interface Enable Register (p. 129).

The QDR-II interface can be connected to 18M bit QDR-II burst of two SRAM with 36 bit data at 200 MHz. The interface has 36 bits input data bus, 36 bits output data bus (four bytes) and 18 bits address bus. The 36 bits data bud include 32 bits payload data and 4 bits overhead. The interface has also QDR_K and QDR_KB output clocks and QDR_CQ and QDR_CQB input clocks. The device supports up to 64 independent FIFOs in the memory, and a full duplex 10Gbps data-stream to and from the memory. It also supports flow control per LID.

The QDR_VREF signal should be connected to 0.75V generated from the VDDH15 power supply using regulator or potential divider such as the MAX1510 as shown in Figure 42 IDT88K8483 VDDA25 Filter Circuit p.75.

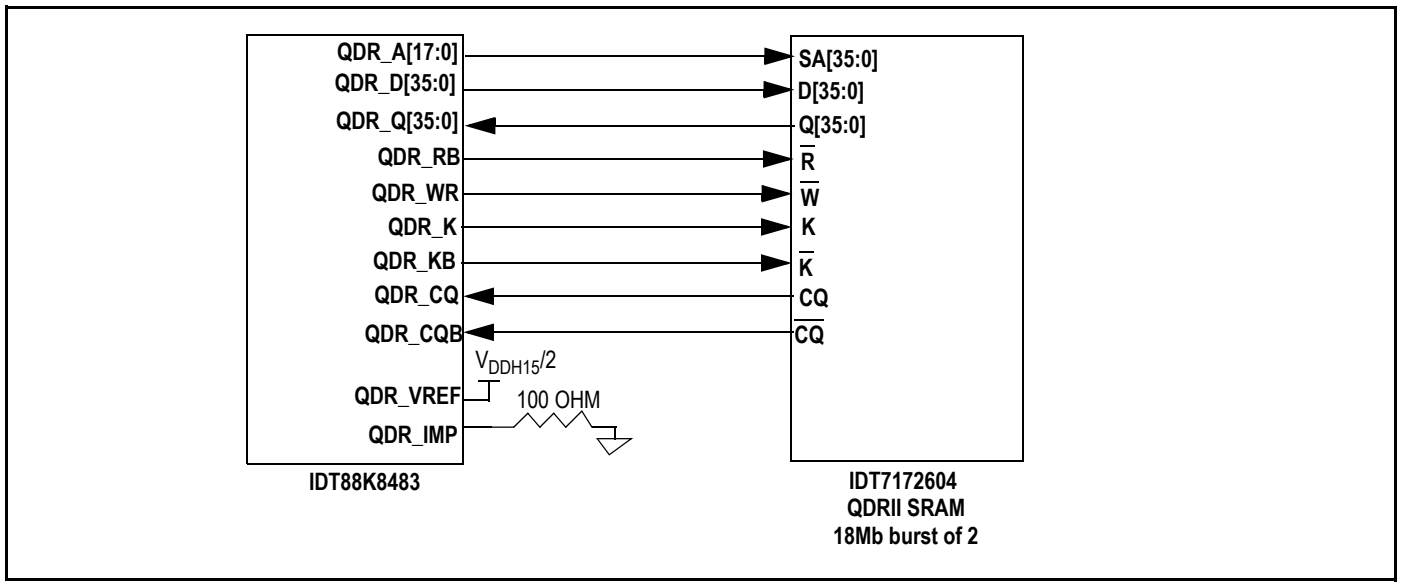


Figure 23 IDT88K8483 and IDT7172604 QDR-II SRAM connections

QDR-II Transfer format

In a single write burst a transfer with 1 to 256 bytes is stored in the memory. A format is defined to map the 1 to 256 bytes in a proprietary transfer format. The format adds 4 overhead bits to each 32 payload bits group. The transfer format overhead includes the total length of the payload (in units of bytes), packet delineation and error tags. The first two overhead fields of a transfer format contain the higher bit of the transfer length, and the transfer beginning field. The third overhead field contains packet delineation and error tag. The fourth overhead field contains the last two bits of the transfer length. All the remaining overhead fields are fixed to 0'b0000.

The minimum length of the transfer format is 4 words (36 bit). The payload is padded with a fixed 0xFF pattern. The transfer length is equal to an integer multiple of 2 words (36 bit).

Memory segmentation

The external SRAM is segmented in a configurable number of FIFOs with equal size. The number of the FIFOs is configured by EBC field in the Auxiliary Interface Configuration Register (p. 129). The memory is managed based on memory segment size of 256byte.

QDR-II Flow Control

The IDT88K8483 gets the QDR-II FIFO status information from the QDR-II interface, and the PFP LID status information from the PFP logic. The IDT88K8483 can be configured to one of two different flow control modes using the EBP_EN field in the PFP Egress Packet Mode Control Registers (p. 123). According to the status information from the QDR-II FIFO and the PFP LID, and the flow control mode, the device generates the status indication to the SPI-4 interface as shown in Table 3 SPI-4 Status Information (p. 56).

If EBP_EN field in the PFP Egress Packet Mode Control Registers (p. 123) is 0 then the flow control mode is mode 1 - packet assembling, no back-pressure or occasional (emergency) backpressure (for example when egress is not rate limited).

If EBP_EN field in the PFP Egress Packet Mode Control Registers (p. 123) is 1 then the flow control mode is mode 2 - buffering, frequent back-pressure (for example rate limited egress).

- When the QDR-II flow control mode is mode 1, the device sends the PFP status to the SPI-4 interface.

- When the QDR-II flow control mode is mode 2, the device sends status to the SPI-4 interface based on the QDR-II status. If the QDR-II status is satisfied or hungry, then the device sends satisfied status to the SPI-4 interface. If the QDR-II status is starving, then the device sends starving status to the SPI-4 interface.

QDR-II FIFO Status	SPI-4 Interface Status (Flow Control Option 2)
starving	starving
hungry	satisfied
satisfied	satisfied
starving	starving
hungry	satisfied
satisfied	satisfied
starving	starving
hungry	satisfied
satisfied	satisfied

Table 3 SPI-4 Status Information

Flow Control Mode 1 - Packet Assembling

In the packet assembling option the IDT88K8483 receives the data in interleaved mode and it sends the data in packet mode (non-interleave mode). In this option the PFP and the QDR-II should be programed to packet mode by setting to 1 the PKT_MODE field in the PFP Egress Packet Mode Control Registers (p. 123) and the PKT_MODE field in the Auxiliary Packet Mode Configuration Register (p. 131). In this case, the device reassemble the interleave data from each channel to packet by monitoring the SOP and EOP indication. It starts the packet with the SOP indication and ends the packet with the EOP indication. The device sends the data in packet mode from the QDR-II to the PFP and then to the port buffers and to the SPI-4 interface.

An application example for flow control mode 1 (packet mode) is described in Figure 24. In this example the device is in over-booking mode, the PFP is used only as a temporary storage, so the packets should be sent immediately from the PFP. Therefore, there is not enough memory for scheduling too many packets, and there cannot be frequent back-pressure. If there is too many back pressure the storage space is limited, and the over-booking mode is not efficient. Since in this case there is no much back-pressure, there is no need to transfer the back-pressure from the QDR-II to the PFP and to the interface. Therefore, the IDT88K8483 sends the PFP status to the interface.

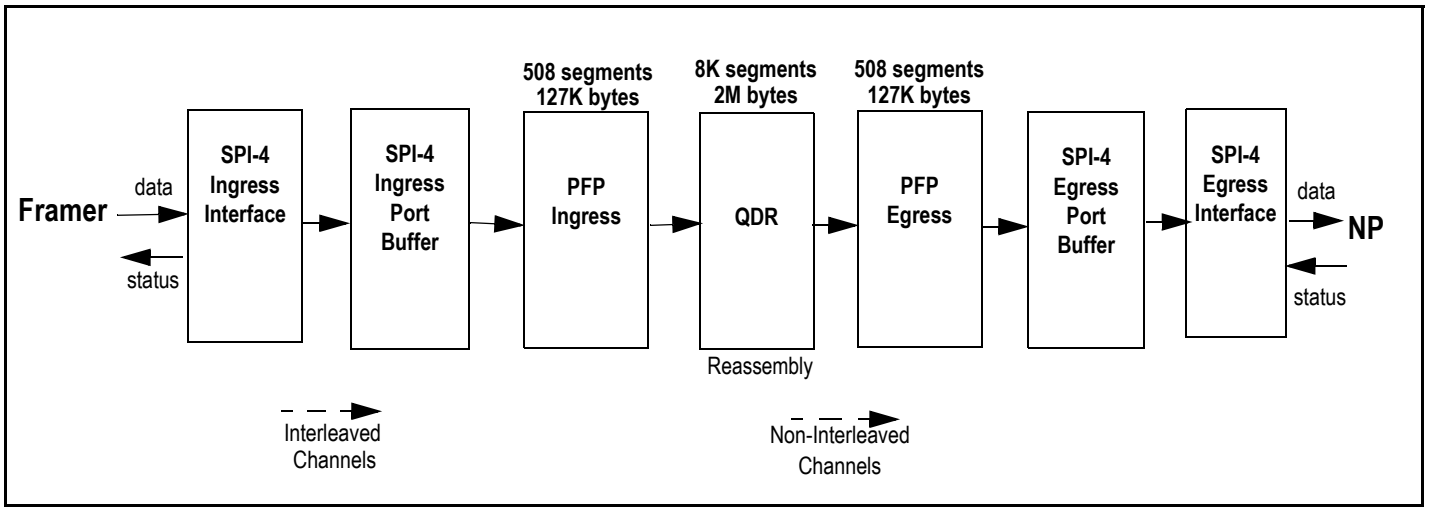


Figure 24 Flow Control Mode 1 Application Example

Flow Control Mode 2 - Buffering

In the buffering option the IDT88K8483 gets the data in interleaved mode or in packet mode and it sends the data in packet mode or in interleave mode. In this option, the EBC[2:0] field in the (p. 129) should be configured to the number of FIFOs in the QDR-II (64, 32, 16, 8 or 4) as described in Figure 25 QDR-II FIFOs Allocation Example For Buffering Option p.57. Each FIFO gets the same amount of buffer size.

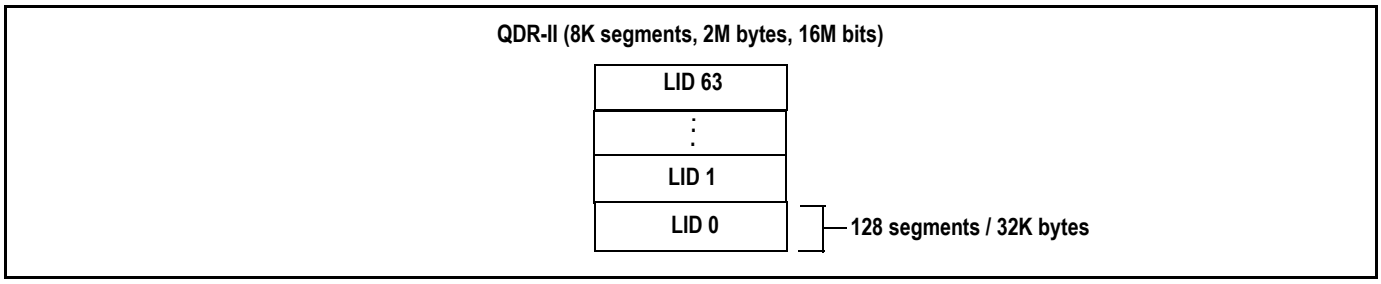


Figure 25 QDR-II FIFOs Allocation Example For Buffering Option

In buffering option, the PFP and the QDR-II should be programed to packet mode by setting to 1 the PKT_MODE field in the PFP Egress Packet Mode Control Registers (p. 123) and the PKT_MODE field in the Auxiliary Packet Mode Configuration Register (p. 131). In addition, the EBP_THR field in the Auxiliary Early Backpressure Threshold Register (p. 131) should be programmed with the early back-pressure threshold value. Also, the flow control mode 2 should be enabled in the PFP by setting to 1 the EBP_EN field in the PFP Egress Packet Mode Control Registers (p. 123). The device fixes the Second Free Segments (Second Free Segments) to 6 as shown in Figure 26 QDR-II Flow Control Example For Buffering Option p.58.

There are three status options per FIFO in the QDR-II: starving hungry and satisfied. In the QDR-II for LP0 (for example), in normal operation there are enough free segments, so the FIFO status is starving, and the QDR-II is sending starving status to the PFP. When the number of free segments is less than EBP_THR (for example 100 segments), the QDR-II FIFO status is changed to hungry, and the QDR-II starts sending hungry status to the PFP. When the number of free segments is less than the Second Free Segments (6 segments), the QDR-II FIFO status is changed to satisfied, and the QDR-II starts sending satisfied status to the PFP.

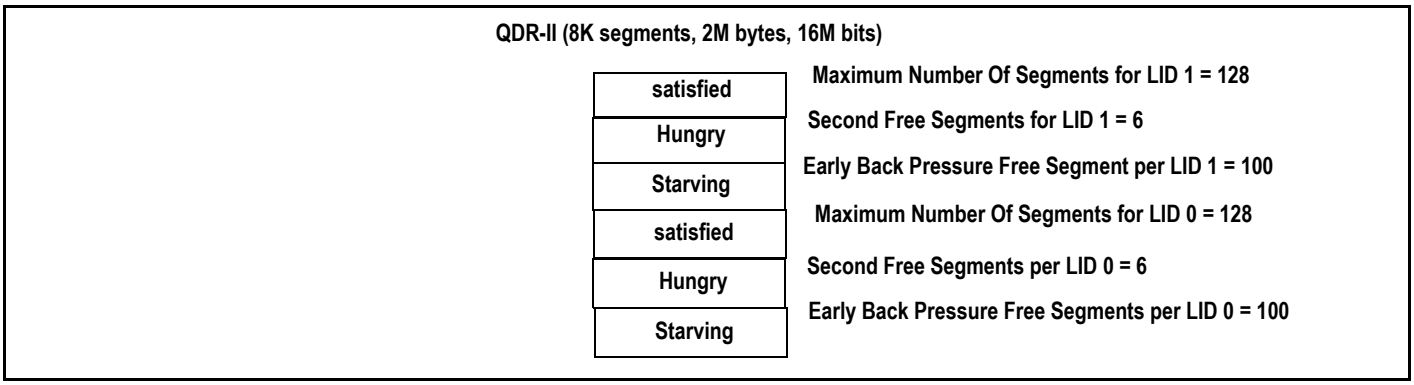


Figure 26 QDR-II Flow Control Example For Buffering Option

An application example for flow control mode 2 is described in Figure 22. In this case there is no over-booking, and there can be frequent back-pressure.

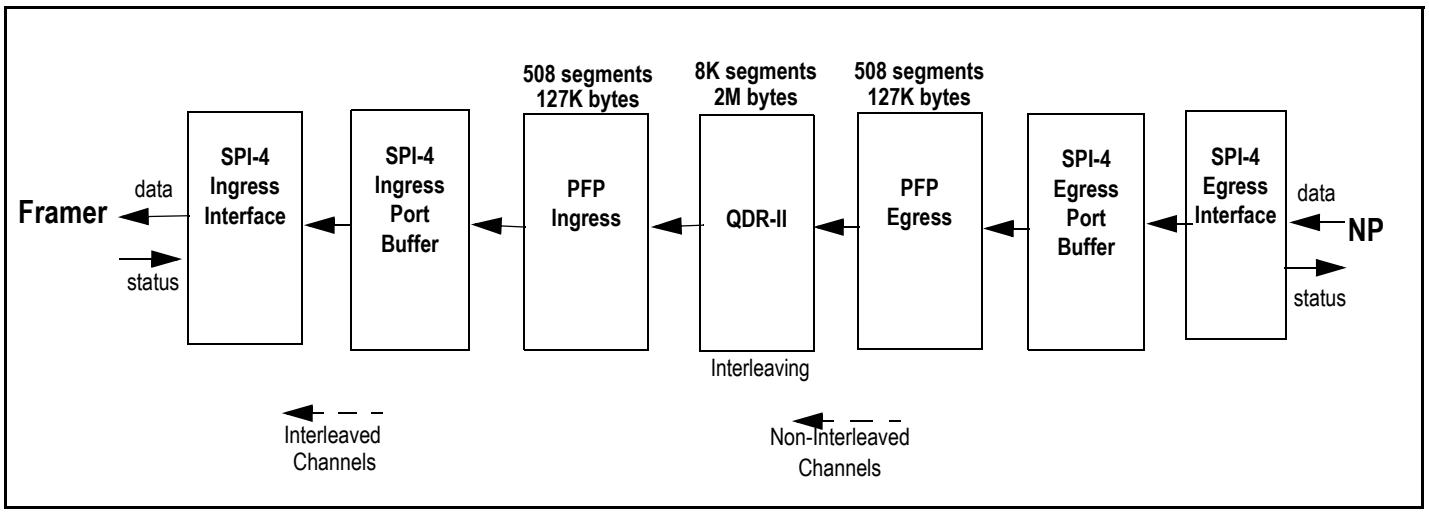


Figure 27 Flow Control Mode 2 Application Example

Impedance Matching Control

The auxiliary interface egress side has impedance matching control. It has on chip test circuit that automatically adjusts the impedance of the auxiliary interface egress data and control signals according to the 100 OHM pull down resistor that is connected to the QDR_IMP external signal.

Generic Interface

Overview

The auxiliary interface has two modes: QDR-II interface mode and generic interface mode. The auxiliary interface mode (QDR-II or generic) is configured by the MEM field in the Auxiliary Interface Configuration Register (p. 129). The auxiliary interface has to be configured before the interface is enabled. The auxiliary interface outputs (except for the clock) can be powered down by setting to 1 the AUX_PDN field in the Auxiliary Interface Enable Register (p. 129). The interface is enabled by setting to 1 the AUX_EN field in the Auxiliary Interface Enable Register (p. 129).

The generic interface can be connected to an FPGA. The interface has 32 bits ingress data bus, 4 bits ingress control bus, 32 bits egress data bus and 4 bits egress control bus. The 4 bits control bus carries the control information that indicates the transfer type, and the 32 bits data bus curries the transfer data. The interface has also differential CLK ingress clock and differential CLK egress clock.

The ingress flow control messages are transmitted on the egress channel. The egress flow control messages are transmitted on the ingress channel. The flow control mechanism provides both per link level flow control and interface level flow control.

The G_VREF signal should be connected to 0.75V generated from the VDDH15 power supply using regulator or pot-divider like MAX1510 as shown in Figure 42 IDT88K8483 VDDA25 Filter Circuit p.75.

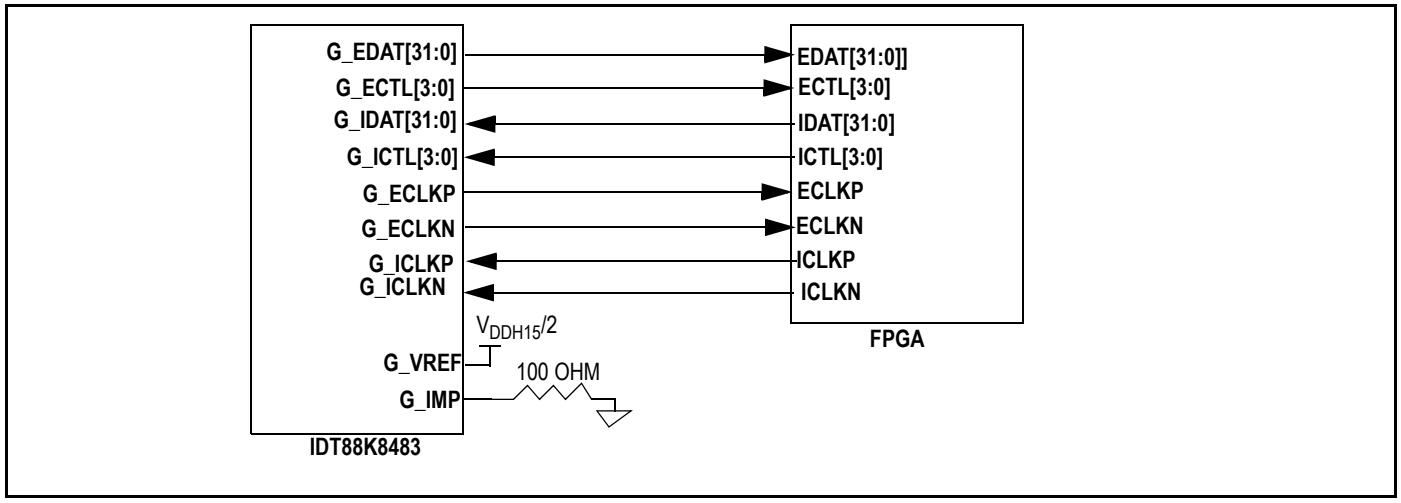


Figure 28 IDT88K8483 and FPGA connections

Transfer Format for Normal Data

The generic interface format is defined to map 1-256 bytes payload in a proprietary transfer format. The transfer format for normal data is shown in Figure 29 (DM is DUMMY information). The minimum payload transfer length is 2 words (1 word is 1 data cycle). The first word of a transfer carries the LID information. LID[5:0] is mapped into B[5:0] of the first byte. The control field of the first transfer is SOP or SOT.

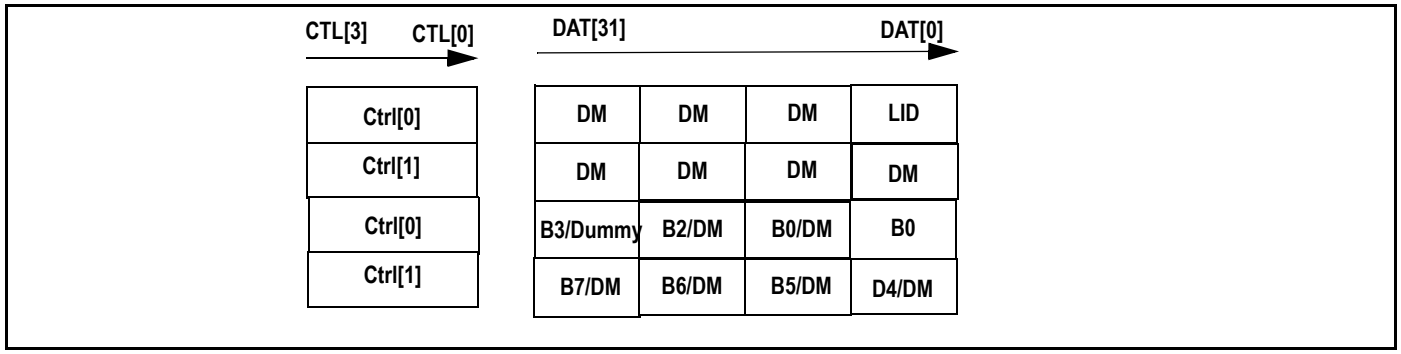


Figure 29 Generic Interface - Transfer Format for Normal Data

The LID field in the Transfer Format for Normal Data includes the LID number (LID0,LID2,LID3,...). The control field is encoded to indicate the type of data word as described in Table 4.

ctrl[1], ctrl[0]	Description
00000000	EOP 1B without error tag
00000001	EOP 2B without error tag
00000010	EOP 3B without error tag
00000011	EOP 4B without error tag
00000100	EOP 5B with error tag
00000101	EOP 6B without error tag
00000110	EOP 7B without error tag
00000111	EOP 8B without error tag
00001000	EOP 1B with error tag
00001001	EOP 2B with error tag
00001010	EOP 3B with error tag
00001011	EOP 4B with error tag
00001100	EOP 5B with error tag
00001101	EOP 6B with error tag
00001110	EOP 7B with error tag
00001111	EOP 8B with error tag
00010000	SOP
00010001	SOT
00010010	EOT
00010011	Normal data, mated receive side ready
00010100	Normal data, mated receive side full
00010101	Status word, mated receive side ready
00010110	Status word, mated receive side full
00010111~11111111	Reserved

Table 4 Generic Interface - Control Field Coding

Transfer Format for Status Word

The transfer format for Status word is shown in Figure 30. The LID information is the PFP back-pressure status (starving, hungry, or satisfied).

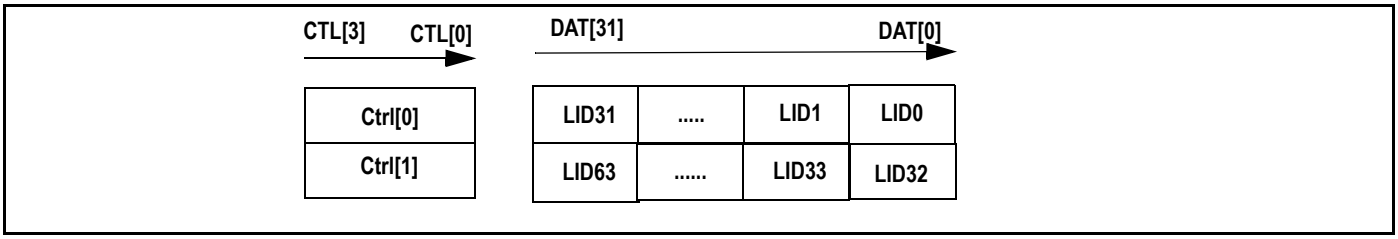


Figure 30 Generic Interface - Transfer Format for Stratus Word.

Interface Operation

The egress channel generates the transfer format and the local status information. The ingress channel detects the transfer format and status information from the adjacent device.

Each word of the ingress interface is classified by decoding the control field. The reserved control field is ignored. The device extracts the LID from the first word of a transfer, and the following payload belongs to this LID.

The egress channel generates the transfer format. The data is transferred to the interface, and the link level status word can interrupt the transfer.

Flow Control

The FPGA has link level back-pressure and interface level back pressure. The interface level back-pressure information is carried on the control signal (ICTL[3:0] and ECTL[3:0]). The link level flow control is using the transfer format status word.

Impedance Matching Control

The auxiliary interface egress side has impedance matching control. It has on chip test circuit that automatically adjusts the impedance of the auxiliary interface egress data and control signals according to the 100 OHM pull down resistor that is connected to the G_IMP external signal.

Microprocessor Interface

Overview

The microprocessor interface can be in serial mode or in parallel mode. When the external signal SPIEN is cleared to 0, the interface is in parallel mode, and when SPIEN signal is set to 1, the interface is in serial mode.

The parallel microprocessor interface can be connected directly to a suitable processor or to a FPGA as shown in Figure 31 Microprocessor Interface - Parallel Mode p.62. The interface has 8 bits data bus and 6 bits address bus. The interface has also write, read, chip select and interrupt signals. In addition there is a mode signal: MPM. When MPM signal is set to 1, the interface is in Intel mode, and when MPM signal is cleared to 0, the interface is in Motorola mode.

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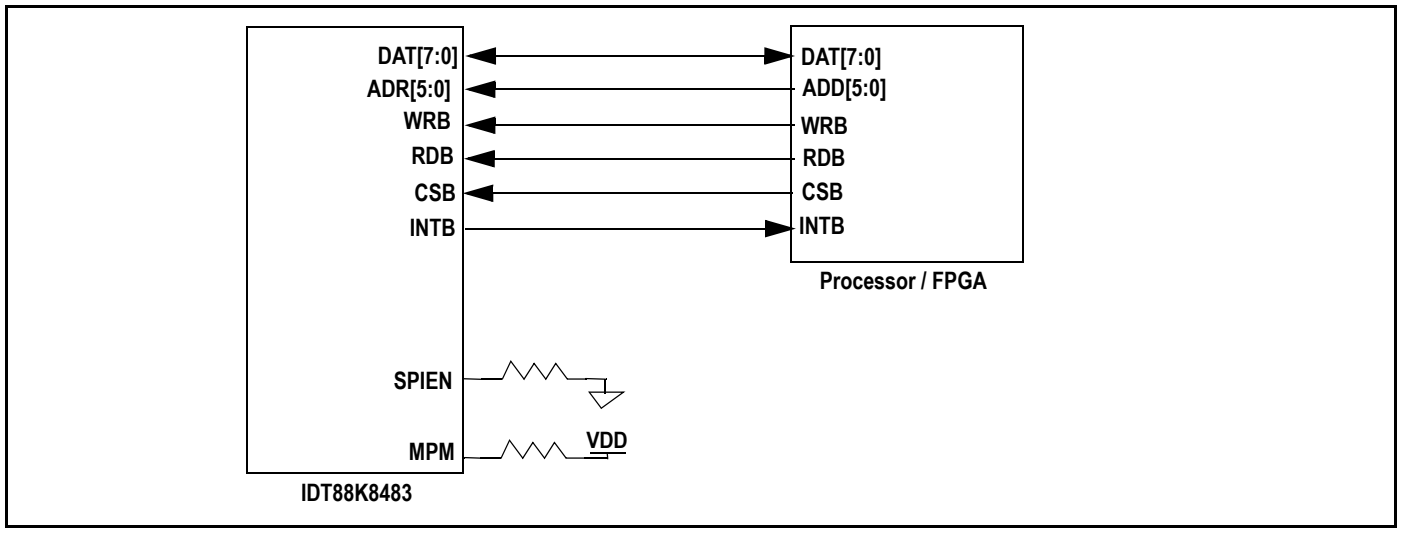


Figure 31 Microprocessor Interface - Parallel Mode

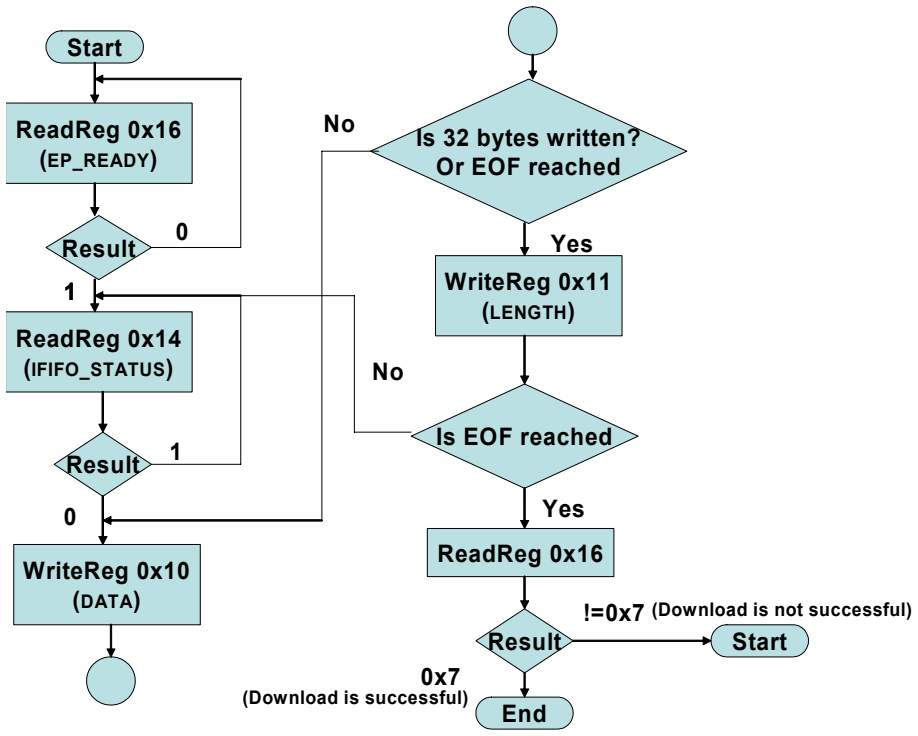
The serial microprocessor interface can be connected directly to a suitable processor or to a FPGA. The interface has data, chip select and clock signals.The microprocessor interface timing is based on the main clock domain. One microprocessor interface cycle is four main clock cycles.

Embedded Processor Download

The embedded processor has 2 mailboxes, I_FIFO and O_FIFO each of which has a 32 byte FIFO. Mailbox I_FIFO is used for firmware download from the host to the embedded processor. Refer to page 90 and page 92 for registers related to the mailbox FIFOs.

The embedded processor is first checked to see if it is ready for download. This is done by reading direct register 0x16. If the result is 0x1, then further downloading steps take place as indicated in the flowchart below.

The download should take place in the little endian format. If the download file is in big endian format and since the downloading takes place in 16 bit words, the lower byte should be swapped with the upper byte.



Firmware download flowchart

Example for download sequence

An example pseudo code of how the download sequence is implemented is shown below

```
DOWNLOAD {
Write RST=0x1     // RST field is in Global Software Reset Register (p. 90)
Read EP_STATE  // Field is in Embedded Processor State Register (p. 92)
IF(EP_STATE == 1) {
   While( !EOF) {            // Read binary data until end of file is encountered
      While(IFIFO_STATUS != 0) && (time < Wait_time)) {    // Field is in Microprocessor Mailbox Input FIFO Status Register (p. 91)
       IF(time == Wait_time)
           return “Wait time error”
        else {
          Write I_FIFO = 32 bytes Binary data or less than 32 if EOF is encountered
 // I_FIFO is in Microprocessor Mailbox Input FIFO Data Register (p. 90)
          Write Length = Binary data length written to I_FIFO   // Length field is in Microprocessor Mailbox Input FIFO Length Register (p. 90)
                    // Writing to the Length register causes the embedded processor to download from the I_FIFO mailbox.
            }
    }    // End of While STATUS loop
  }    // End of while !EOF loop
}    // End of IF Ep_State loop
```

} // End of Download

Interrupt

The device captures events in the Primary Interrupt Indication Register (p. 98). The Interrupt status fields in the Primary Interrupt Indication Register (p. 98) are cleared by writing 1 to the appropriate field.

The device has two interrupt levels: a primary level and a secondary level. The primary level status indicates the interrupt status of module A/B/COMMON. The secondary level status indicates the interrupt status per module.

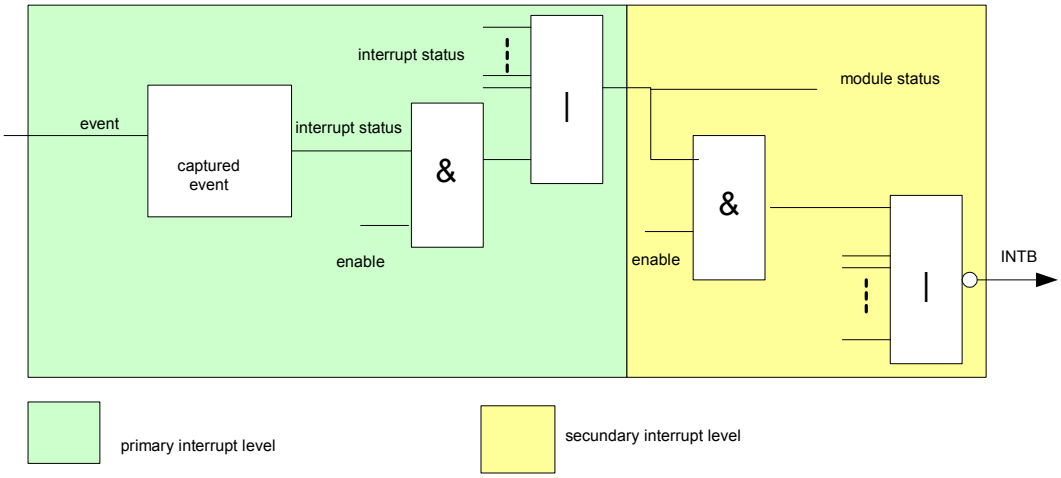


Figure 32 Interrupt Scheme

PMON

PMON Events

There are few event types: Field associated non-critical event, Field associated critical event, Non field associated events. The events are described in the tables below.

When a Field associated non-critical event is captured, the LID or LP (which is associated the event) is captured, and the table register records the latest captured LID or LP.

For field associated critical event, only one kind of critical event is defined, and it is per lid captured. TM_OVF field in the PMON Buffer Overflow Source Register (p. 142) indicates the OR result of 64 LIDs status of T_M direction. MT_OVF field in the PMON Buffer Overflow Source Register (p. 142) indicates the OR result of 64 LIDs status of M_T direction.

Non field associated events are captured without any associated field.

Event Name	Associated Field	Definition
Main ingress inactive LP	LP	This event is raised when an inactive Logical Port is encountered.
T-M illegal SOP	LID	Please refer to page 52 for an explanation for when this event is raised.
T-M illegal EOP	LID	Please refer to page 52 for an explanation of when this event is raised.
M-T illegal SOP	LID	Please refer to page 52 for an explanation of when this event is raised.
M-T illegal EOP	LID	Please refer to page 52 for an explanation of when this event is raised.
T-M packet cut down	LID	Please refer to page 52 for an explanation of when this event is raised.
M-T packet cut down	LID	Please refer to page 52 for an explanation of when this event is raised.

Table 5 Field Associated Non-Critical Event List

Event Name	Associated Field	Definition
T-M buffer overflow	LP	Global buffer overflow or per link overflow.
M-T buffer overflow (LID0-63)	LID	Global buffer overflow or per link overflow.

Table 6 Field Associated Critical Event List

Event Name	Remark	Definition
Tributary SPI4 ingress locker unavailable		Tributary SPI4 ingress locker unavailable
Main SPI4 ingress locker unavailable		SPI4 interface
Tributary ingress data clock loss		SPI4 interface
Tributary egress status clock loss		SPI4 interface
Main ingress data clock loss	Valid for module A	SPI4 interface
Main egress status clock loss	Valid for module A	SPI4 interface
Tributary SPI4 DIP-2		SPI4 interface
Tributary SPI4 DIP-4		SPI4 interface
Tributary SPI4 bus error		Please refer to page 44 for an explanation of bus error.
Tributary ingress synch status change		SPI4 interface
Tributary Egress synch status change		Tributary Egress synch status change.
Main SPI4 DIP-2	Valid for module A	SPI4 interface
Main SPI4 DIP-4	Valid for module A	SPI4 interface
Main SPI4 bus error	Valid for module A	SPI4 interface
Main ingress synch status change	Valid for module A	SPI4 interface
Main Egress synch status change	Valid for module A	

Table 7 Non Field Associated Event List

Counters

There are two types of counters: Per LID counters and per module counters. The Per LID counters are described in the PMON Per LID Counter Table (p. 144). The per module counters are described in the PMON Per Module/Interface Counter Table (p. 144).

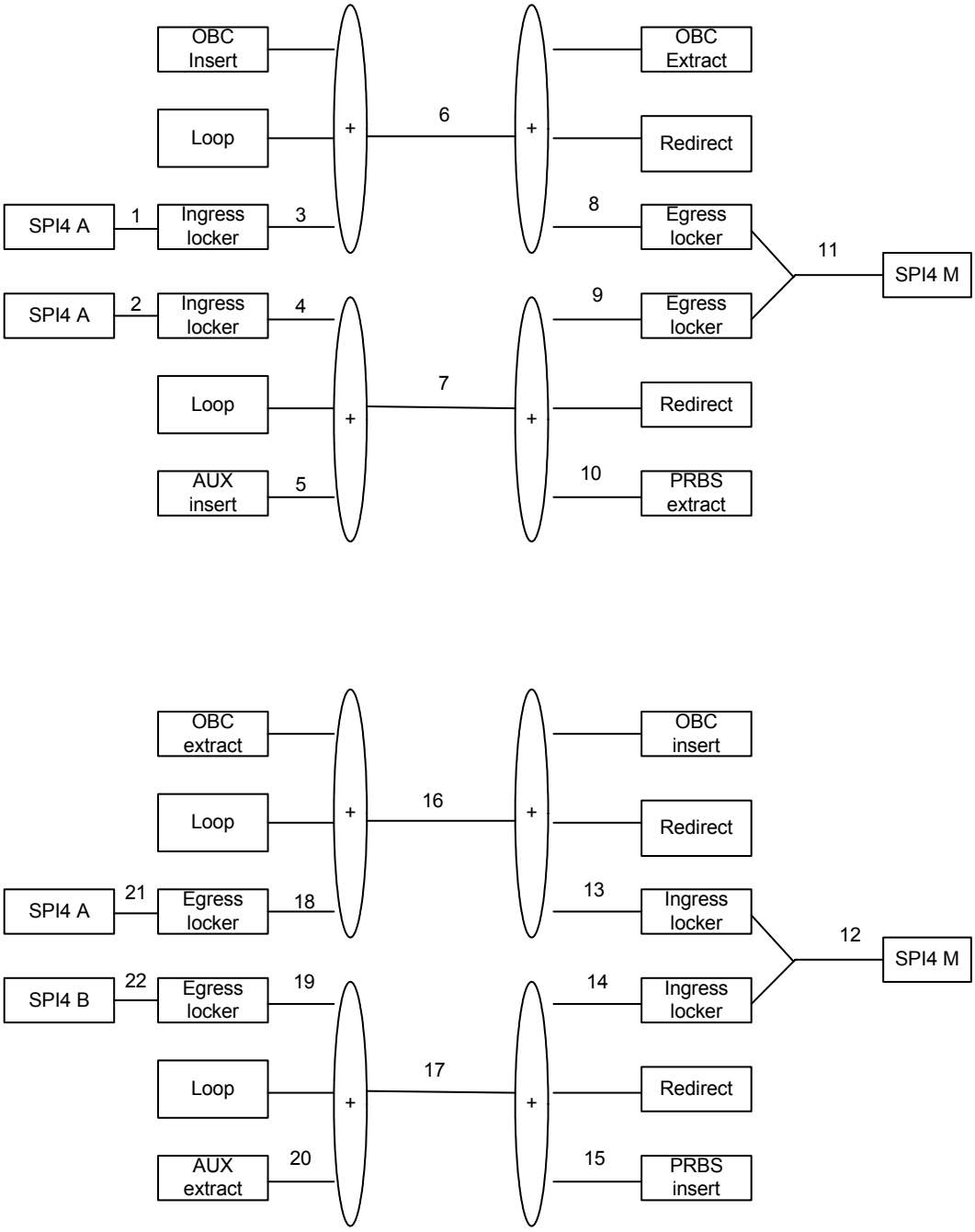


Figure 33 PMON Measure Points

Time base

A single PMON time base is provided for the device. The time base can be generated internally or externally according to the INTERNAL field in PMON 1ms Timer Register (p. 145). The internal time base can be generated by a free running timer or OBC according to the TIMER field in the PMON 1ms Timer Register (p. 145). The time base sources are described in the Table 8.

[INTERNAL, TIMER, MANUAL]	Time base trigger source
3'b0xx	The time base is generated externally.
3'b11x	The internal time base is generated by a free running timer.
3'b10x	The internal time base is generated by OBC.

Table 8 Time Base Source

Internal PMON Time Base

The device has a 1ms accurate timer. The 1ms timer register specifies the number of MCLK for generating 1ms time intervals. A 10ms event is generated based on the 1ms timer, and forwarded to the interrupt module and to the internal embedded processor.

In internal timer mode, the device generates one time base trigger in each second. In internal OBC mode, writing 1 to the MANUAL field in the PMON 1ms Timer Register (p. 145) generates a time base trigger. The one second is generated based on the 1ms timer.

The time base trigger generates a 16-MCLK high pulse to TIMEBASE pin, and it updates the PMON counters. The time base trigger also generates a TIMEBASE interrupt event to the interrupt module. The delay between the time base trigger and the TIMEBASE interrupt event is 3 to 4ms. Subsequent trigger is ignored during the this period. The internal PMON time base wave form is shown in Figure 34.

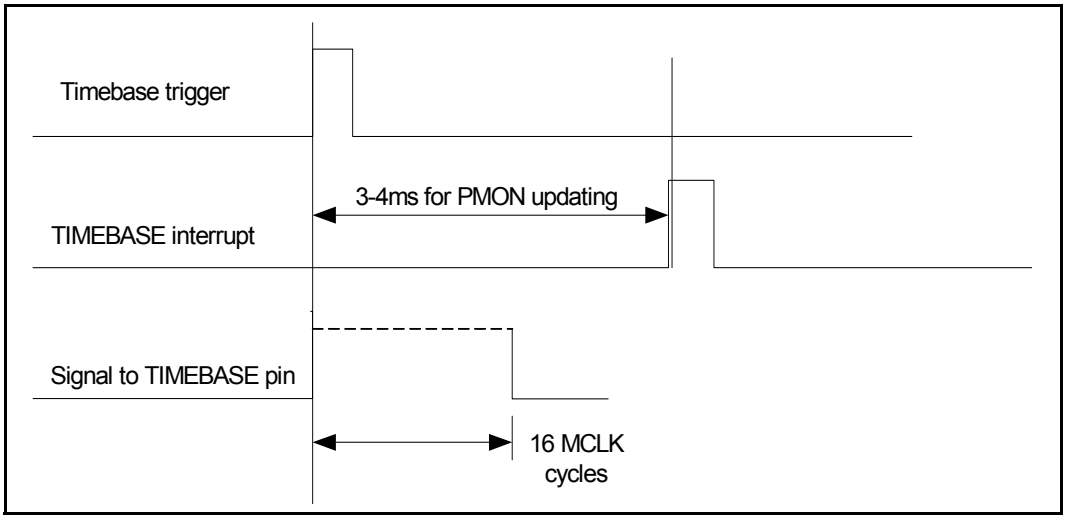


Figure 34 Internal PMON Time Base

External PMON Time Base

A positive edge on the TIMEBASE pin generates an externally time base trigger. The time base trigger updates the PMON counters, and generates a TIMEBASE interrupt to the interrupt module. The delay between the time base trigger and the TIMEBASE event is 3 to 4 ms. Subsequent trigger is ignored during this period. The external PMON time base wave form is shown in Figure 35.

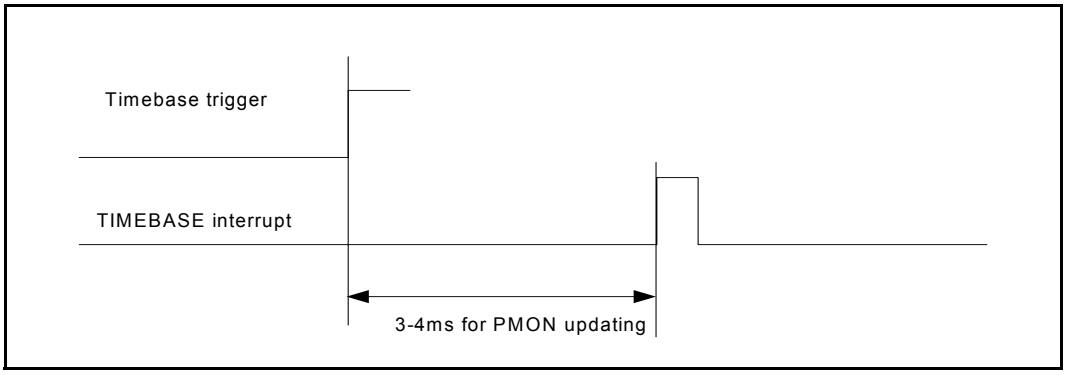


Figure 35 External PMON Time Base

Clock

IDT88K8483 has three programmable clock generators (main, tributary A and tributary B). One clock generator (main) is type M and two clock generators (tributary A and tributary B) are type T. There are three input clocks SPI4A_RCLK, SPI4B_RCLK and SPI4M_RCLK. Each one of the clock inputs is a clock source to one of the three internal clock generators. The device also has 4 clock configuration signals (DIV4, SPI4A_CLK_SEL, SPI4B_CLK_SEL, and SPI4M_CLK_SEL) for programing the clock generators. The clock generator type M includes the following blocks: Prescaler, PLL and three independent dividers as described in Figure 36 Clock Generator Type M p.70. The clock generators type T include the following blocks: Prescaler, PLL and two independent dividers as described in Figure 37 Clock Generator Type T p.70.

CKSEL (external input signal: SPI4A_CLK_SEL, SPI4B_CLK_SEL, SPI4M_CLK_SEL)	EDCLK / ISCLK_T (external output signals)	Operation Mode
0	plloclk / 2 (plloclk is internal signal)	Full rate
1	plloclk / 8 (plloclk is internal signal)	Quarter rate

Table 9 CLK_SEL signals configuration

The external configuration signals SPI4A_CLK_SEL, SPI4B_CLK_SEL and SPI4M_CLK_SEL configure the Divider 1 frequency to divide by 2 or 8 as described in Table 9. The external signals SPI4A_CLK_SEL, SPI4B_CLK_SEL and SPI4M_CLK_SEL value are reflected by CK_SEL_A, CK_SEL_B and CK_SEL_C fields in the Clock Control Input Status Register (p. 104). The external configuration signal DIV4 configures the prescaler frequency to divide by 4 or 1 as described in Table 10. The external signal DIV4 value is reflected by DIV_FOUR field in the Clock Control Input Status Register (p. 104).

DIV4 (external input signal)	pllrclk (internal signal)	Operation Mode
0	RCLK / 1 (RCLK is external input signal: SPI4A_RCLK, SPI4B_RCLK, SPI4M_RCLK)	Full rate
1	RCLK / 4 (RCLK is external input signal: SPI4A_RCLK, SPI4B_RCLK, SPI4M_RCLK)	Quarter rate

Table 10 DIV4 signal configuration

Clock Generator Type M

Clock generator type M generates the internal clock MCLK and the external SPI-4 main interface clocks (EDCLK, ISCLK, ISCLK_T) as shown in Figure 36 Clock Generator Type M p.70. The MCLK clock is used for the generic interface, the PFP block and the PMON block. The clock generator source is the external signal SPI4M_RCLK. The MCLK frequency is selected by the N field in the MCLK Divider Sticky Register (p. 104). The N field value can be modified at any time during normal operation. The SPI-4 operation rate is selected by the external signal SPI4M_CLK_SEL. The external signal DIV4 configures the prescaler frequency to divide by 4 or 1.

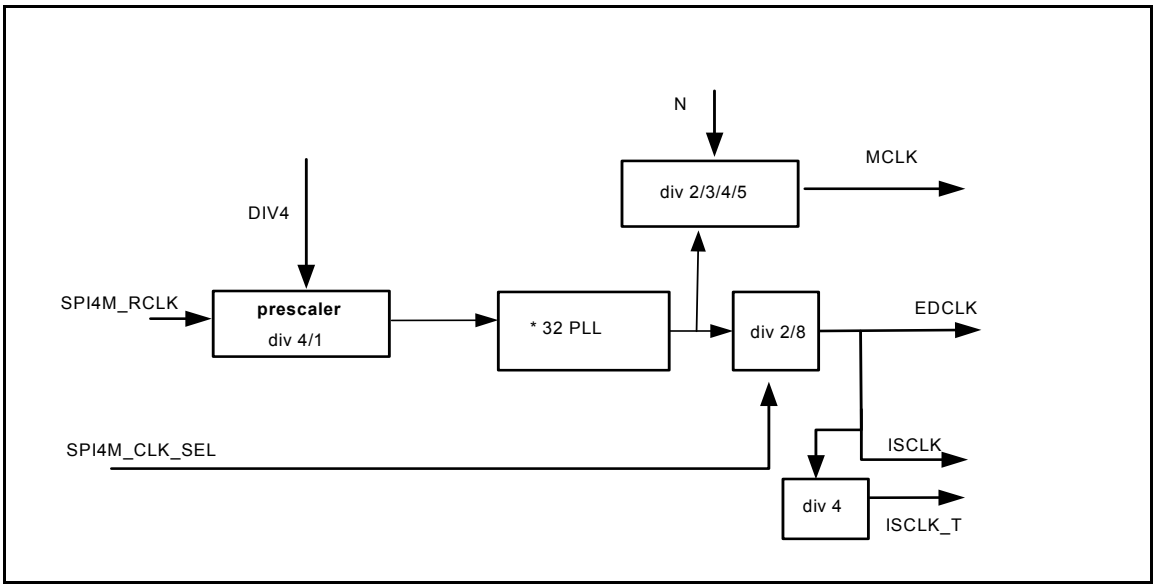


Figure 36 Clock Generator Type M

Clock Generator Type T

Clock generator type T generates the SPI-4 tributary interface clocks (EDCLK, ISCLK, ISCLK_T) as shown in Figure 37 Clock Generator Type T p.70. The clock generator sources are the external signals SPI4A_RCLK and SPI4B_RCLK. SPI-4 operation rate is selected by the external signals SPI4A_CLK_SEL and SPI4B_CLK_SEL. The external signal DIV4 configures the prescaler frequency to divide by 4 or 1.

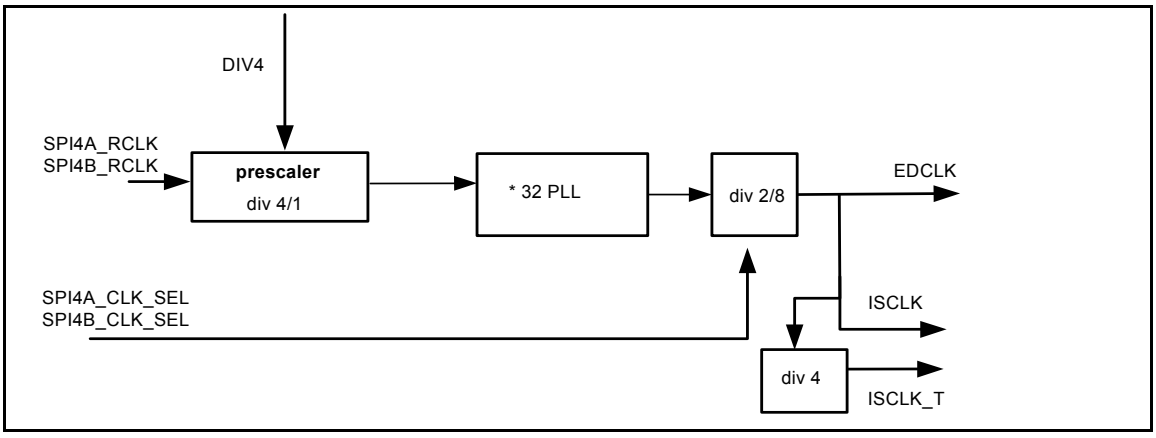


Figure 37 Clock Generator Type T

Design Consideration

System Reset

There are two methods for resetting the IDT88K8483: hardware reset and software reset. During reset the output clocks are not toggled.

Hardware Reset

The RESETB input requires an active low pulse to reset the internal logic.

Software Reset

The software reset is triggered by setting to 1 the RST field in Global Software Reset Register (p. 90). The response to a software reset is identical to a hardware rest except that software reset does not change the N field in the MCLK Divider Sticky Register (p. 104), so it does not impact the clock generators. After software reset the microprocessor should have delay of at least 2ms before accessing the device.

Power On Sequence

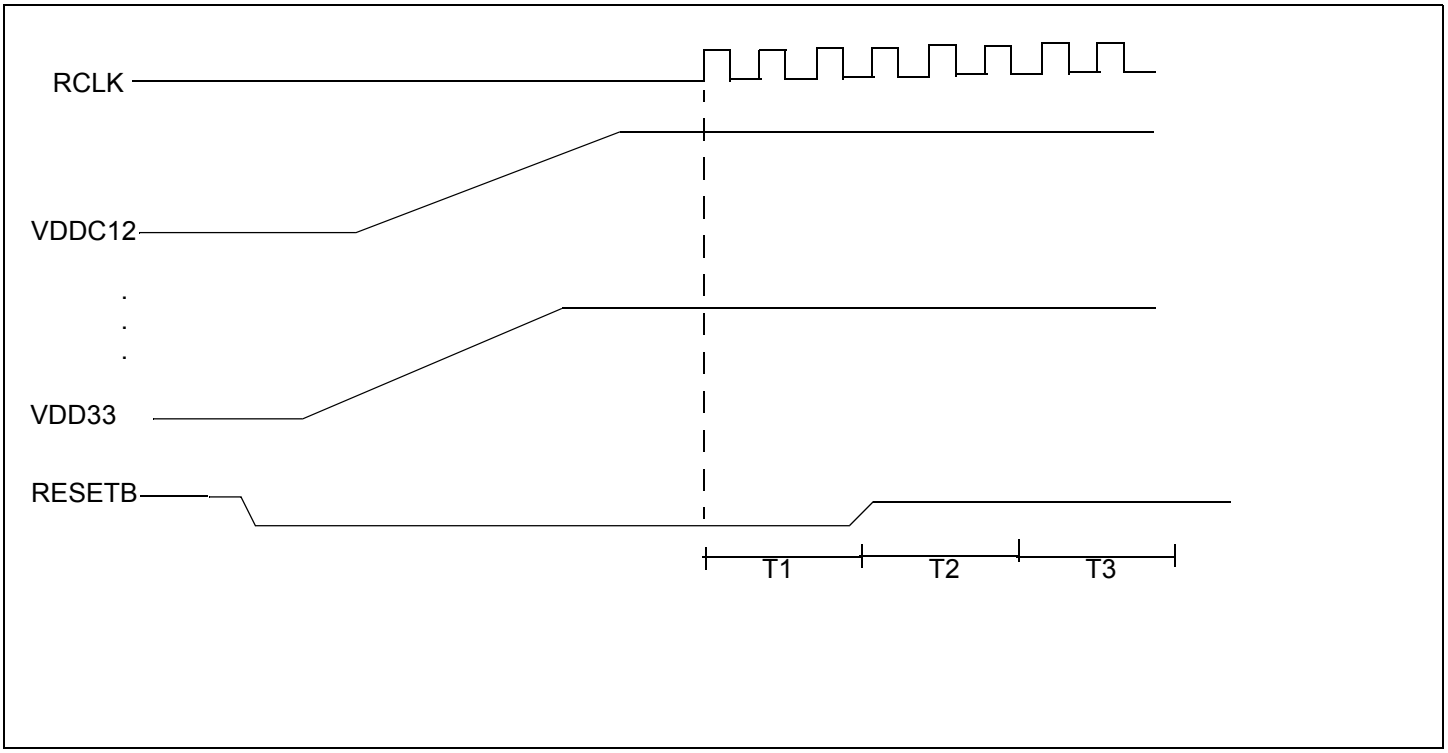


Figure 38 Power-on-Reset Sequence

A correct power-on-reset sequence is crucial for the normal behavior of the device. The power-on-reset sequence includes the following signals: RCLK (SPI4A_RCLK, SPI4B_RCLK, SPI4M_RCLK), VDD (VDD33, VDDL25, VDDH25, VDDH15, VDDL12, VDDC12, VTT) and RESETB (RESETB). Figure 38 Power-on-Reset Sequence p.71 illustrates the recommended implementation for the power-on-reset sequence for the device. IDT recommends powering up the 3.3V (VDD33) power supply first, the 2.5V (VDDL25, VDDH25) power supply second, the 1.5V (VDDH15) power supply third, the 1.2V (VDDC12, VDDL12) power supply fourth, and the 0.75V (VTT) power supply last. The power supplies can be also powered up in the same time. There is no requirement for the minimum or maximum delay between the power-up of the power supplies. The power supplies should be powered off in the reverse order. The power ramp should not be faster than 100us.

When the power supplies are powered up, the RESETB signal should be at low level. During power-on-reset, after the VDD, RCLK and the configuration signals are stable, the RESETB signal should remain at a low level at least 10ms (symbol “T1”) to reset the internal logic. After the RESETB pulse ends, the device starts generating the SPI-4 external output clocks and the MCLK internal clock.

After the RESETB pulse ends, a delay of 2ms should be added (symbols “T2” and “T3”) before accessing the device for initialization and configuration. This allows the internal logic to be stable. During T2 (at least 1ms delay) the device performs internal memories initialization, and during T3 (at least 1ms delay) the device run a boot code from the internal embedded processor ROM.

After T3, the user should poll the CHIP_READY field in the Embedded Processor State Register (p. 92), and wait until it is 1. When the CHIP_READY field is 1, the user should download the firmware binary file from the external microprocessor to the IDT88K8483 embedded processor RAM.

JTAG

IEEE Boundary Scan standard 1149.1, informally known as JTAG (Joint Test Action Group), is a testing standard that uses software to reduce testing costs by eliminating the need for a sophisticated in-circuit test equipment. The inclusion of boundary-scan registers in integrated circuits greatly improves the testability of boards. Boundary scan provides a mechanism for testing component input, output and inter-connections. Devices containing boundary scan have the capability of driving or observing the logic levels on I/O pins by utilizing the TAP (Test Access Port). The TAP controller, a 16-state Moore-type state machine, dictates the control of all JTAG activities through four pins: TDI (Test Data Input), TDO (Test Data Output), TMS (Test Mode Select), and TCK (Test Clock).

Data is passed serially from one device to the next, thus forming a boundary-scan path or chain from TDI (Test Data Input) that originates at the test controller and returns there, through the scan path, to TDO. To test the external interconnect, devices drive values at their outputs and observe input values received from other devices. An external test controller compares the received data with expected results. Any device can be temporarily removed from the boundary-scan path by bypassing its internal shift registers, and passing the serial data directly onto the next device. This allows efficient testing of a selected device without incurring the overhead of traversing through other devices. JTAG testing can also be used to check the inter connectivity of external memory devices by generating read and write test vectors independent of the chip functionality. The read and write vector results can then be read back to ensure that the memory devices are connected correctly.

Design for Test

IDT strongly recommends that its customers use JTAG testing for both prototypes and production boards. Large pin count devices, and in particular ball grid arrays require confidence in the correct assembly of the initial prototype boards. The IDT88K8483 chip has 672 pins FCBGA. Bed-of-nails testing does not allow the testing of BGA mounting to the board. JTAG testing is very effective at isolating assembly errors down to individual signals in a very short time.

During the board bring-up process, several weeks have been spent identifying problems that turned out to be incorrectly assembled boards, particularly BGAs not mounted correctly to the board. Using JTAG enables the issues to be immediately identified if design for test is considered from the outset. It is possible for the customer to generate comprehensive JTAG tests within a week of becoming familiar with the appropriate equipment and tools. The time between Gerber files going to fabrication and the board’s return can be used to generate the appropriate JTAG tests, thus limiting schedule impact. The effort is also much less than that required to develop functional diagnostic tests to exercise and test every individual pin. JTAG results in considerable time saving during the prototype bring-up, which can be one of the most significant causes of delays in overall time-to-market.

IDT's bring-up strategy is based on the assumption that the customer’s board is correctly assembled, and has been tested to ensure proper assembly before attempting to run any functional tests.

IDT88K8483 JTAG Testing

The IDT88K8483 supports board-level testing through the use of a JTAG test port. The test port comprises the following pins: JTDI (Test Data Input), TDO (Test Data Output), TMS (Test Mode Select), TCK (Test Clock), and TRSTB (Test Reset). The TCK clock frequency is up to 10MHz.

When JTAG testing is used on the board, all the devices should be JTAG daisy-chained, TDO to TDI as shown in Figure 39 JTAG Daisy Chain p.73. Note that the pins on the JTAG connector are named so that TDI drives the TDI of the first device and TDO is driven by TDO of the last device. Also, the TCK, TMS and TRSTB signals of all the devices should be connected together and driven from the JTAG connector.

The internal JTAG logic of each device powers up in an unknown state, so it is necessary at power-on to reset it to the Test-Logic-Reset state so that the chip operates properly. This can be done in one of the three different ways:

1. TRSTB is pulled low by a resistor. TRSTB must also connect to the JTAG connector, and the JTAG tester must drive TRSTB high for JTAG testing.
2. A low pulse is applied to TRSTB at power on as shown in Figure 40 TRSTB Signal During Power-On Reset p.73. Note that a falling edge is not required on TRSTB. TRSTB can then be held high as long as TMS is also pulled high, thereby keeping the logic in the reset state. This method is appropriate if the JTAG tester does not drive TRSTB.
3. TCK can be clocked five or more times while TMS is held high. In this case, TRSTB can be pulled high. This method is also appropriate if the JTAG tester does not have TRSTB.

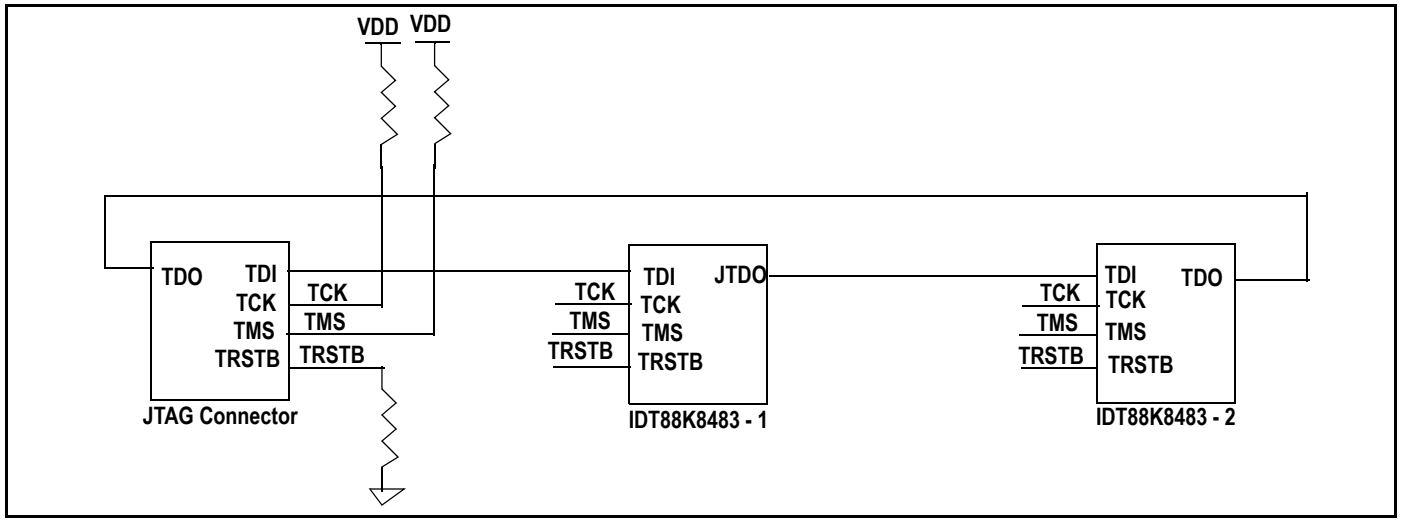


Figure 39 JTAG Daisy Chain

The TRSTB signal is an option reset pin and may not be available on all JTAG test connectors. TRSTB should be held high during JTAG testing. Once in the Test-Logic-Reset test, the JTAG logic will remain in this state as long as TMS is high, regardless of the state of TRSTB.

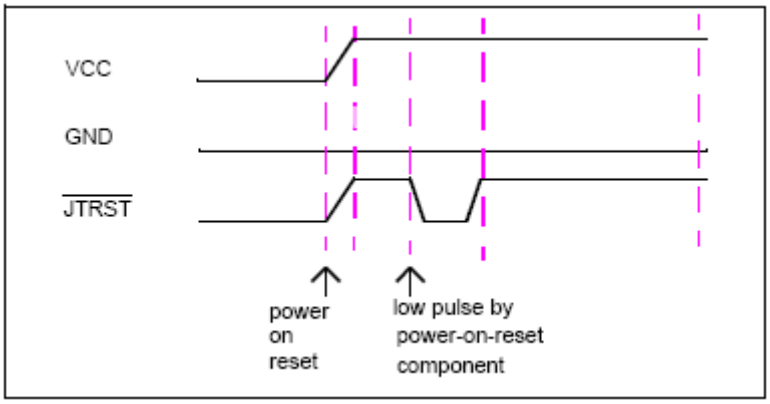


Figure 40 TRSTB Signal During Power-On Reset

The TCK signal should be carefully routed on board according to standard layout design to minimize skew and noise problems.

JTAG specifications require that pull-up resistors be supplied internally to the TDI, TRSTB, and TMS pins in the chips. Very long JTAG chains or parts from different vendors may present significant loading to the controller. To compensate for this, the designer should include buffers on TMS, TRSTB and TCK to account for unknown device impedance. For systems with several components, the designer should use a high fan-out buffer.

Ensure that the buffer has sufficient drive capability to supply all loads. When using a buffer to drive any of the JTAG TAP pins, it may be necessary to include an external resistor to ensure the pin is set to the correct state when the buffer is idle. Thus, TRSTB should have an external resistor to ground when driven by an external buffer and TMS and TCK should each have an external pull-up.

The JTAG instructions are described in Table 11. The JTAG ID information is described in Table 12.

Instructions	Instruction Codes	Function Description
EXTEST	000	Test the function to other devices
IDCODE	001	Used to connect the identification register
HIGHZ	100	Set outputs to Hi-Z state
CLAMP	011	Clamp the output latches
SAMPLE	010	Sample all the inputs and outputs
RUNBIST	110	BIST
USERCODE	101	User code
BYPASS	111	Used to bypass the device

Table 11 JTAG Instruction Code

Version	Part Number	Manufacture ID	Fixed
0	0x4af	0x33	1

Table 12 JTAG ID

GPIO

The device has 3 general purpose input/output pins. The pins' direction is independently controlled by the DIR_OUT field in the GPIO Direction Register (p. 145). The logical level on the pins is controlled by the LEVEL field in the GPIO Level Register (p. 146). The LEVEL field reflects the status of any bit which is selected from the indirect access space if enabled. A bit in the indirect access space can be selected by the ADDRESS and BIT fields in the GPIO Link Table (p. 146). A bit can be enabled by the REFLECT_EN field in the GPIO Link Table (p. 146). IDT recommends to connect all the unused GPIO signals to an FPGA or microprocessor pins for debugging purpose.

Power Supply

The IDT88K8483 Power Supplies can be generated as shown in the design example in Figure 41 IDT88K8483 Power Supply Generation Example p.75. The IDT88K8483 system should have the following:

1. Connect the V_{DDA25} signals through filter to The V_{DDH25} / V_{DDL25} signals as described in Figure 42 IDT88K8483 VDDA25 Filter Circuit p.75.
2. Connected together the V_{DDH25} signals and the V_{DDL25} signals.
3. Separate the V_{DDC12} signals and V_{DDL12} signals.
4. Generate the V_{DDL25} / V_{DDH25} signals from V_{DDT33} signals.
5. Generate the V_{TT075} signals from V_{DDH15} signals.

6. Connect the V_{SPI4A_VREF}, V_{SPI4B_VREF} and V_{SPI4M_VREF} signals through filter to VDDL12 signals as described in Figure 43 IDT88K8483 SPI4x_VREF Filter Circuit p.75.

7. Generate the V_{QDR_VREF}/V_{G_VREF} signals from the V_{DDH15} power supply using regulator or pot-divider like MAX1510 ($V_{DDH15}/2$).

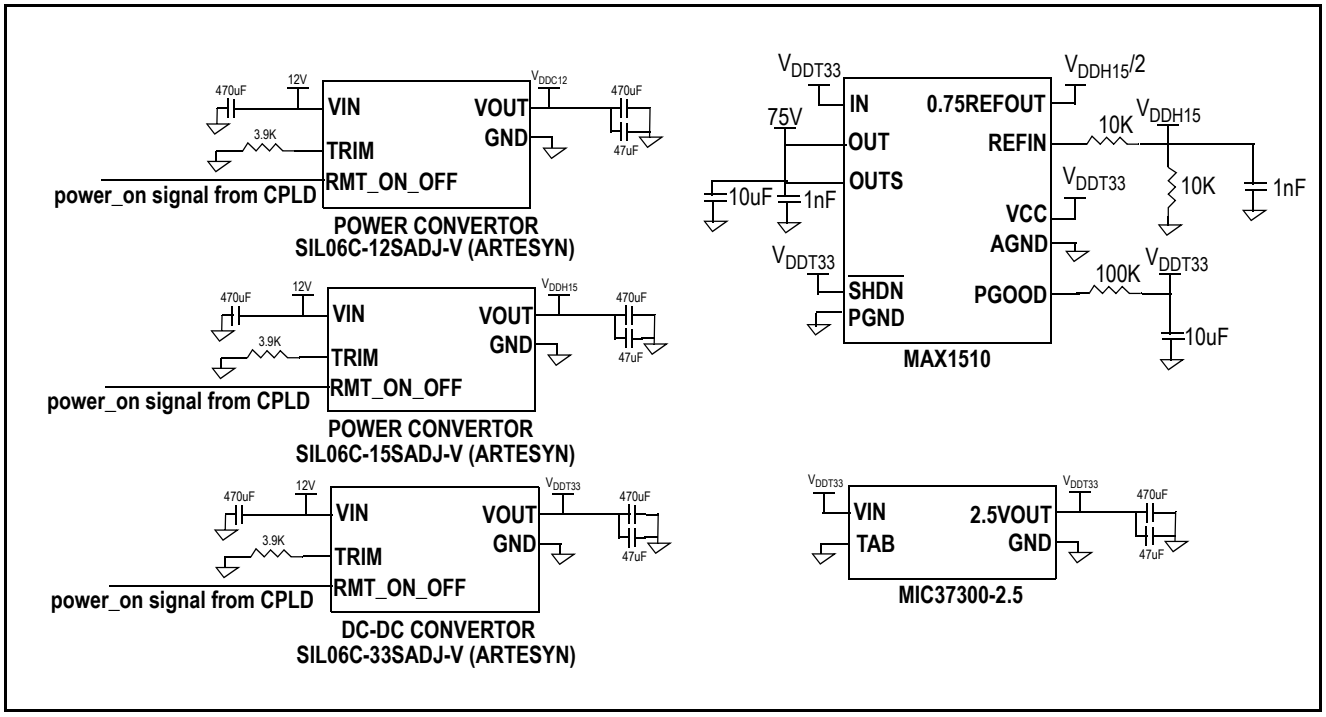


Figure 41 IDT88K8483 Power Supply Generation Example

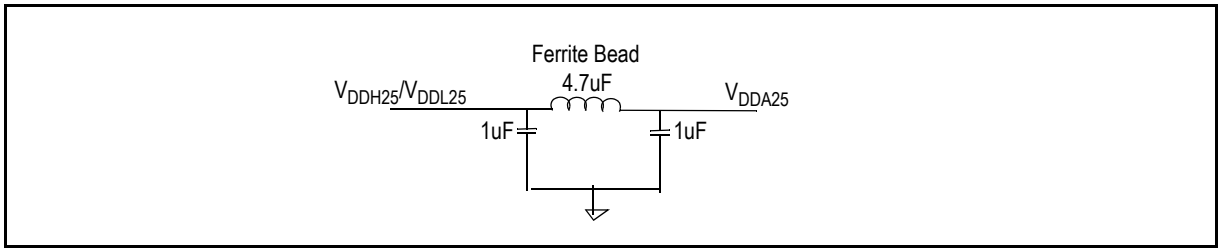


Figure 42 IDT88K8483 VDDA25 Filter Circuit

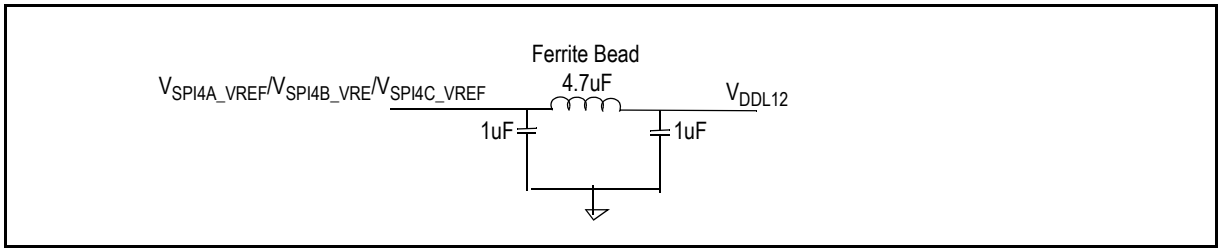


Figure 43 IDT88K8483 SPI4x_VREF Filter Circuit

Configuration Sequence

Before writing the configuration flow, design and determine the device configuration including:

- Specific application
- Data path
- Mapping relation between link and logic port
- Working mode of each link

The device configuration flow is as follows:

1. Download the firmware binary file to the embedded processor and check if the chip has been initialized to a state that user can access it.

2. Configure the PMON timebase, if you want to use the internal timer.

3. Configure the PFP including the following parameters: link id number, buffer size, cut through/packet mode, backpressure threshold, burst size, weight and direction, etc.

4. Configure the SPI4 interface, including ingress/egress logical port mapping, calendar configuration, interface initialization and enabling, and synchronization check.

5. Initialize auxiliary interface memory/generic mode, if you use auxiliary interface.

6. Initialize PRBS module, if you use PRBS insert/extract.

7. During the traffic test check the device status by reading various information, such as PMON statistic information, PFP/SPI4 status information and interrupt information.

Note: Please refer to the **programming guide** for device configuration examples.

Registers

Register Organization:

There are two types of register in the IDT88K8483:

- **Direct Registers:** Direct registers are used for high-priority registers such as interrupts and for access to the indirect registers. Direct registers can be accessed more quickly than indirect registers. All direct access registers are one byte wide. Direct registers used for accessing indirect registers are known as indirect access registers.They consist of 8 bit address registers, data registers and control registers.The direct registers address space, size and type is shown in Table 13.

Register Address Size (Bits)	Register Address Range (HEX)	Register Data Size (Bits)	Type
8^{I}	0x0 to 0x25	8^{I}	Read/Write, Read Only, Write Only.

Table 13 Direct Register Table

- **Indirect registers:** Indirect access registers are used for configuration, maps, etc. They are accessed via the direct register space by means of a protocol which maps microprocessor interface pins A[5:0] D[7:0] and control pins to internal register space A[19:0], D[31:0], and Control[7:0]. The indirect register address space and register size is shown in Table 14.

Register Address Size (Bits)	Register Data Size (Bits)	Type
20^{I}	8^{I} or 32^{I}	Read/Write, Read Only, Write Only.

Table 14 Indirect Register Table

Register Access Protocol.

Direct Access

The direct access registers have 8 bit data (one byte data) and 8 bits address as shown in table 13.These are accessed via the microprocessor interface.

- Read operations to a reserved address or reserved bit fields return 0.
- Write operations to reserved address or bit fields are discarded.

Indirect Access

The indirect access scheme uses the indirect access address register, indirect access control register and indirect access data register to map a 24 bit indirect address, and 32 bit data into the indirect register. The control register validates the access request and performs operations accordingly. The direct registers used for indirect access are shown in Table 15.

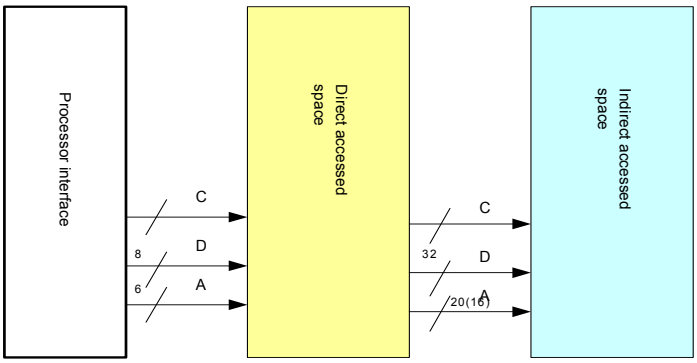


Figure 44 Indirect Register Access Scheme

Direct Register Address (HEX)	Register Size (Bits)	Used for	Type
0x1a	8	Indirect access control	Read/Write
0x1b	8	Indirect access data (BYTE 0)	Read/Write
0x1c	8	Indirect access data (BYTE 1)	Read/Write
0x1d	8	Indirect access data (BYTE 2)	Read/Write
0x1e	8	Indirect access data (BYTE 3)	Read/Write
0x1f	8	Indirect access address (BYTE 0)	Read/Write
0x20	8	Indirect access address (BYTE 1)	Read/Write
0x21	8	Indirect access address (BYTE 2)	Read/Write

The Indirect Register Accessing scheme:

Address Name	No of Bytes	Description
Segment Base	3	Address based on User Registers or IDT reserved registers.
Module Base	2	Address based on Module A, B or Common module which includes the SPI4 interfaces, PFPs and associated PMONs, insert, extract registers.
Block Base	2	Address based on blocks of registers related to SPI4 Ingress and Egress interfaces, related PFPs and PMONs, Auxillary interface, Processor interface.
Register Offset	1	Address of the individual registers for each Block Base.

3 Byte Indirect register Address = 3 Byte Segment Base Address **+**

2 Byte Module Base Address **+**

2 Byte Block Base Address **+**

1 Byte Register Offset

Indirect Read and Write Operation:

- **Indirect Write Access Operation**
  - The OBC reads the BUSY flag in the Microprocessor Indirect Access Control Register (p. 93). It proceeds only when the flag is cleared.
  - The indirect WRITE access operation is triggered by a write operation in the indirect access control register. This is achieved by setting field RWN to 0 in the Microprocessor Indirect Access Control Register (p. 93).
  - The process sets the BUSY flag in the indirect access control register immediately and verifies the indirect address.
  - When the address is out of bounds, no internal memory is accessed and the BUSY flag is cleared.
  - When the address is within bounds the indirect write operation is achieved as soon as possible.
  - The BUSY flag is cleared as soon as the Write operation is completed and the address is auto incriminated
  - The ERROR field in the Microprocessor Indirect Access Control Register (p. 93) indicates an errorcode.Correct operation returns ERROR = 0.

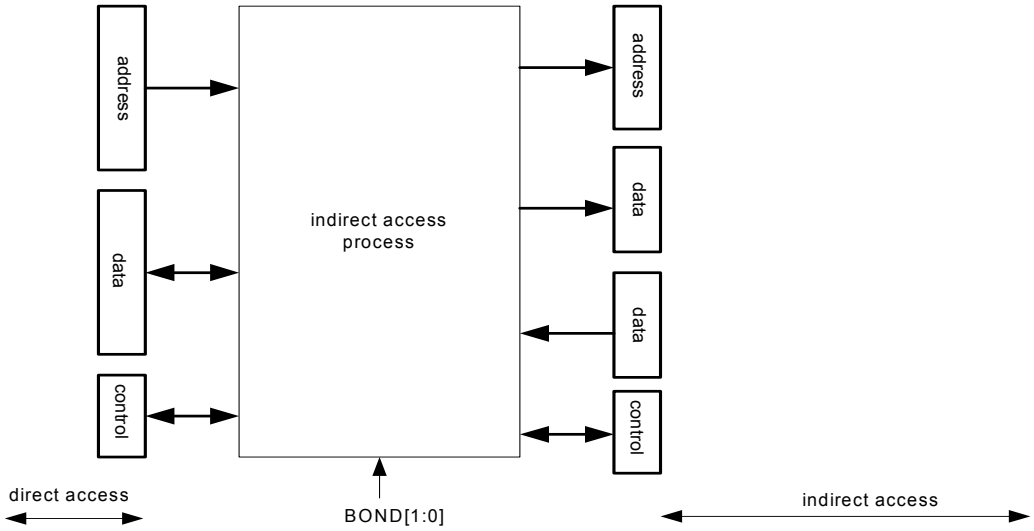


Figure 45 Indirect access module

- **Indirect Read Access Operation**
  - The indirect READ access operation is triggered by a read operation to the indirect access control register. This is achieved by setting field RWN to 1 in the Microprocessor Indirect Access Control Register (p. 93).
  - The process sets the BUSY flag in the indirect access control register immediately and verifies the indirect address.
  - When the address is out of bounds, no internal memory is accessed and the BUSY flag is cleared. Also the indirect access data registers(p.85) are cleared.
  - When the address is within bounds the indirect read operation is achieved as soon as possible.
  - The BUSY flag is cleared as soon as the Read operation is completed and the address is automatically incremented.
  - The ERROR field in the Microprocessor Indirect Access Control Register (p. 93) indicates an error code. Correct operations return ERROR = 0.

Register Map

Direct Registers Map

Register Offset	Register Name
0x 0	PFP T-M insert control register for module A (p. 96)
0x 1	PFP T-M insert data register for module A (p. 97)
0x 2	PFP T-M extract control register for module A (p. 97)
0x 3	PFP T-M extract data register for module A (p. 97)
0x 4	PFP M-T insert control register for module A (p. 97)
0x 5	PFP M-T insert data register for module A (p. 97)
0x 6	PFP M-T extract control register for module A (p. 98)
0x 7	PFP M-T extract data register for module A (p. 98)
0x 8	Primary Interrupt Indication Register (p. 98)
0x 9	Primary Interrupt Enable Register (p. 99)
0x a	Secondary Interrupt Module A Indication Register (p. 100)
0x b	Secondary Interrupt Module A Enable Register (p. 100).
0x c	Secondary Interrupt Module B Indication Register (p. 101)
0x d	Secondary Interrupt Module B Enable Register (p. 101)
0x e	Secondary Interrupt COMMON Indication Register (p. 102)
0x f	Secondary Interrupt COMMON Enable Register (p. 103)
0x 10	Microprocessor Mailbox Input FIFO Data Register (p. 90)
0x 11	Microprocessor Mailbox Input FIFO Length Register (p. 90)
0x 12	Microprocessor Mailbox Output FIFO Data Register (p. 91)
0x 13	Microprocessor Mailbox Output FIFO Length Register (p. 92)
0x 14	Microprocessor Mailbox Input FIFO Status Register (p. 91)
0x 15	Microprocessor Mailbox Output FIFO Status Register (p. 92)
0x 16	Embedded Processor State Register (p. 92)
0x 17	Reserved
0x 18	Reserved
0x 19	Reserved
0x1a	Microprocessor Indirect Access Control Register (p. 93)
0x 1b	Microprocessor Indirect Access Data Register - 1 (p. 93)
0x 1c	Microprocessor Indirect Access Data Register - 2 (p. 94)
0x 1d	Microprocessor Indirect Access Data Register - 3 (p. 94)
0x 1e	Microprocessor Indirect Access Data Register - 4 (p. 95)
0x 1f	Microprocessor Indirect Access Address Register - 1 (p. 95)
0x 20	Microprocessor Indirect Access Address Register - 2 (p. 95)

Table 15 Direct Registers Map (Part 1 of 2)

Register Offset	Register Name
0x 21	Microprocessor Indirect Access Address Register - 3 (p. 95)
0x 22	Global Software Reset Register (p. 90)
0x 23	Reserved.
0x 24	Reserved.
0x 25	Reserved.

Table 15 Direct Registers Map (Part 2 of 2)

Indirect Registers Map

- **Indirect Register Addressing = Segment Base Address + Module Base Address + Block Base Address + Register_Offset**

Segment Base Address

There are five **segments** defined for indirect registers as shown in Table 16.. Only the USER_SEG is used by the users.

Segment base Address	Segment Base Name	Segment Base Description
0x00000	USER_SEG	User register
0x10000	RESERVED	Registers reserved for use by IDT
0x20000	RESERVED	Registers reserved for use by IDT
0x30000	RESERVED	Registers reserved for use by IDT
0x40000	RESERVED	Registers reserved for use by IDT

Table 16 Indirect Registers Map - Segment Base Address

Module Base Address

There are three **modules** defined for indirect registers as shown in Table 17.

Module Base Address	Module Base Name	Module Base Description	Function
0x0000	Module_A	Tributary SPI-4 A, PFP A and associated PMON, insert/extract registers	SPI-4, PFP, PMON
0x2000	Module_B	Tributary SPI-4 B, PFP B and associated PMON, insert/extract registers	SPI-4, PFP, PMON
0x8000	Common	Main SPI-4, clock generator, GPIO and chip version registers	SPI-4, PFP, PMON

Table 17 Indirect Registers Map - Module Base Address

Block Base Address and Register Offset

There are **block bases** defined for module registers (tributary SPI-4 A, PFP A and associated PMON, insert/extract and tributary SPI-4 B, PFP B and associated PMON, insert/extract) and for common (main SPI-4, clock generator, GPIO and chip version) as shown in Table 18.

Indirect Registers Map

Module Base Address	Block Base Name	Block Base Address	Register Offset	Indirect Register Address 0x	Register Description
M:0x8000	CLK_GEN	0x0a00	0x00	M: 08a00	MCLK Divider Sticky Register (p. 104)
M:0x8000	CLK_GEN	0x0a00	0x01	M: 08a01	Clock Control Input Status Register (p. 104)
A:0x0000 B:0x2000 M:0x8000	LP2LID_MAP	0x0000	0x00-0xFF	A: 00000 - 000FF B: 02000 - 020FF M:08000 - 080FF	SPI-4 Ingress LP to LID Mapping Table (p. 105)
A:0x0000 B:0x2000 M:0x8000	INGRESS_CAL0	0x0100	0x00-0xFF	A: 00100 - 0013F B: 02100 - 0213F M:08100 - 0817F	SPI-4 Ingress Calendar 0 Table (p. 105)
A:0x0000 B:0x2000 M:0x8000	INGRESS_CAL1	0x0200	0x00-0xFF	A: 00200 - 0023F B: 02200 - 0223F M:08200 - 0827F	SPI-4 Ingress Calendar 1 Table (p. 105)
SPI-4 Ingress Register group					
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x00	A: 00300 B: 02300 M:08300	SPI-4 Interface Enable Register (p. 106)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x01	A: 00301 B: 02301 M:08301	SPI-4 Ingress Configuration Register (p. 106)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x02	A: 00302 B: 02302 M:08302	SPI-4 Ingress Training Parameter Register (p. 107)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x03	A: 00303 B: 02303 M:08303	SPI-4 Ingress Calendar 0 Configuration Register. (p. 107)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x04	A: 00304 B: 02304 M:08304	SPI-4 Ingress Calendar 1 Configuration Register (p. 108)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x05	A: 00305 B: 02305 M:08305	SPI-4 Ingress Status Register (p. 108)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x06	A: 00306 B: 02306 M:08306	SPI-4 Ingress Diagnostics Register (p. 109)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x07	A: 00307 B: 02307 M:08307	SPI-4 Ingress Automatic Alignment Control Register (p. 109)

Table 18 Indirect Registers Map (Part 1 of 8)

Module Base Address	Block Base Name	Block Base Address	Register Offset	Indirect Register Address 0x	Register Description
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x08	A: 00308 B: 02308 M:08308	SPI4 Ingress Calendar Switch Control Register (p. 109)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x0B-0x0C	A: 0030B B: 0230B M: 0830B - 0830C	SPI-4 Ingress Fill Level Register (p. 110)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x0D-0x0E	A: 0030D B: 0230D M:0830D - 0830E	SPI-4 Ingress Max Fill Level Register (p. 110)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x0F-0x10	A: 0030F B: 0230F M:0830F - 08310	SPI-4 Ingress WATERMARK Register (p. 111)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x13	A: 00313 B: 02313 M:08313	SPI-4 Ingress Training to out of sync threshold Register (p. 111)
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x14	A: 00314 B: 02314 M:08314	Reserved
A:0x0000 B:0x2000 M:0x8000	INGRESS_REG	0x0300	0x15-0x24	Reserved	Reserved
A:0x0000 B:0x2000 M:0x8000	LID2LP_MAP	0x0400	0x00-0x7F or 0x00-0x3F	A: 00400- 0043F B: 02400 - 0243F M:08400 - 0847F	SPI-4 Ingress Training to out of sync threshold Register (p. 111)
A:0x0000 B:0x2000 M:0x8000	EGRESS_CAL0	0x0500	0x00	A: 00500-0053F B: 02500-0253F M:08500-0857F	SPI-4 Egress Calendar 0 Table (p. 111)
A:0x0000 B:0x2000 M:0x8000	EGRESS_CAL1	0x0600	0x00	A: 00600-0063F B: 02600-0263F M:08600-0867F	SPI-4 Egress Calendar 1 Table. (p. 112)
SPI-4 Egress Register group					
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG	0x0800	0x01	A: 00801 B: 02801 M:08801	SPI-4 Egress Configuration Register (p. 113)
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG	0x0800	0x02	A: 00802 B: 02802 M:08802	SPI-4 Egress Training Parameter Register (p. 113)
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG	0x0800	0x03	A: 00803 B: 02803 M:08803	SPI-4 Egress Calendar 0 Configuration Register (p. 114)

Table 18 Indirect Registers Map (Part 2 of 8)

Module Base Address	Block Base Name	Block Base Address	Register Offset	Indirect Register Address 0x	Register Description
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG	0x0800	0x04	A: 00804 B: 02804 M:08804	SPI-4 Egress Calendar 1 Configuration Register (p. 114)
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG	0x0800	0x05	A: 00805 B: 02805 M:08805	SPI-4 Egress Status Register (p. 115)
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG	0x0800	0x06	A: 00806 B: 02806 M:08806	SPI-4 Egress Diagnostics Register (p. 115)
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG	0x0800	0x07	A: 00807 B: 02807 M:08807	SPI-4 Egress Automatic Alignment Control Register (p. 115)
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG,	0x0800	0x08	A: 00808 B: 02808 M:08808	SPI-4 Egress Calendar Switch Control Register (p. 116)
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG	0x0800	0x0B-0x0C	A: 0080B B: 0280B M:0880B- 0880C	SPI-4 Egress Fill Level Register (p. 116)
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG	0x0800	0x0D-0x0E	A: 0080D B: 0280D M:0880D - 0880E	SPI-4 Egress Max Fill Level Register (p. 116)
A:0x0000 B:0x2000 M:0x8000	EGRESS_REG,	0x0800	0x0F	A: 0080F B: 0280F M:0880F	Reserved
A:0x0000 B:0x2000 M:0x8000	SPI_TIMING	0x0900	0x00	A: 00900 B: 02900 M:08900	SPI-4 Histogram Measure Launch Register (p. 117)
A:0x0000 B:0x2000 M:0x8000	SPI_TIMING	0x0900	0x01	A: 00901 B: 02901 M:08901	SPI-4 Histogram Measure Status Register (p. 117)
A:0x0000 B:0x2000 M:0x8000	SPI_TIMING	0x0900	0x02-0x0B	A: 00902 - 0090B B: 02902 - 0290B M:08902 - 0890B	SPI-4 Histogram Counter Register (p. 117)
A:0x0000 B:0x2000 M:0x8000	SPI_TIMING	0x0900	0x0C-0x1E	A: 0090C - 0091E B: 0290C - 0291E M:0890C - 0891E	SPI-4 Bit Alignment Result Register (p. 118)
A:0x0000 B:0x2000 M:0x8000	SPI_TIMING	0x0900	0x2A	A: 0092A B: 0292A M:0892A	SPI-4 Egress Data Lane Timing Register (p. 118)
A:0x0000 B:0x2000 M:0x8000	SPI_TIMING	0x0900	0x2B	A: 0092B B: 0292B M:0892B	SPI-4 Egress Data Control Lane Timing Register (p. 118)

Table 18 Indirect Registers Map (Part 3 of 8)

Module Base Address	Block Base Name	Block Base Address	Register Offset	Indirect Register Address 0x	Register Description
A:0x0000 B:0x2000 M:0x8000	SPI_TIMING	0x0900	0x2C	A: 0092C B: 0292C M:0892C	SPI-4 Egress Data Clock Timing Register (p. 119)
A:0x0000 B:0x2000 M:0x8000	SPI_TIMING	0x0900	0x2D	A: 0092D B: 0292D M:0892D	SPI-4 Egress Status Timing Register (p. 119)
A:0x0000 B:0x2000 M:0x8000	SPI_TIMING	0x0900	0x2E	A: 0092E B: 0292E M:0892E	SPI-4 Egress Status Clock Timing Register (p. 120)
A (TM) B (TM) A (MT) B (MT)	BUFFER_ ASSIGN	TM - 0x1000 MT - 0x1800	0x00-0x3F	TM A: 01000 - 0103F B: 03000 - 0303F MT A: 01800 - 0183F B: 03800 - 0383F	PFP Buffer Segment Assign Table (p. 120)
A (TM) B (TM) A (MT) B (MT)	PACKET_ LEN	TM - 0x1100 MT - 0x1900	0x00-0x3F	TM A: 01100 - 0113F B: 03100 - 0313F MT A: 01900 - 0193F B: 03900 - 0393F	PFP Packet Length Thresholds (p. 121)
A (TM) B (TM) A (MT) B (MT)	QUEUE_ DIAGNOSE	TM - 0x1200 MT - 0x1A00	0x00-0x3F	TM A: 01200 - 0123F B: 03200 - 0323F MT A: 01A00 - 01A3F B: 03A00 - 03A3F	PFP Queue Diagnose Table (p. 121)
A (TM) B (TM) A (MT) B (MT)	PACKET_ DIAGNOSE	TM - 0x1300 MT - 0x1B00	0x00-0x3F	TM A: 01300 - 0133F B: 03300 - 0333F MT A: 01B00 - 01B3F B: 03B00 - 03B3F	PFP Packet Diagnose Table (p. 121)
A (TM) B (TM) A (MT) B (MT)	BURST_SIZE	TM - 0x1400 MT - 0x1C00	0x00-0x3F	TM A: 01400 - 0143F B: 03400 - 0343F MT A: 01C00 - 01C3F B: 03C00 - 03C3F	PFP Egress Burst Size Table (p. 122)
A (TM) B (TM) A (MT) B (MT)	DIRECTION	TM - 0x1500 MT - 0x1D00	0x00-0x3F	TM A: 01500 - 0153F B: 03500 - 0353F MT A: 01D00 - 01D3F B: 03D00 - 03D3F	PFP Egress Weight And Direction Register (p. 122)

Table 18 Indirect Registers Map (Part 4 of 8)

Module Base Address	Block Base Name	Block Base Address	Register Offset	Indirect Register Address 0x	Register Description
A (TM) B (TM) A (MT) B (MT)	PACKET_ MODE	TM - 0x1600 MT - 0x1E00	0x00-0x3F	TM A: 01600 - 0163F B: 03600 - 0363F MT A: 01E00 - 01E3F B: 03E00 - 03E3F	PFP Egress Packet Mode Control Registers (p. 123)
PFP TM Control Register group - 0x1700 **PFP MT Control Register group - 0x1F00**					
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x00	TM A: 01700 B: 03700 MT A: 01F00 B: 03F00	PFP Link Number Configuration Register (p. 123)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x01	TM A: 01701 B: 03701 MT A: 01F01 B: 03F01	PFP Buffer Management Configuration Register (p. 123)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x02	TM A: 01702 B: 03702 MT A: 01F02 B: 03F02	PFP Queue Weighting Enable Register (p. 124)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x03	TM A: 01703 B: 03703 MT A: 01F03 B: 03F03	PFP Flow Control Register (p. 125)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x04	TM A: 01704 B: 03704 MT A: 01F04 B: 03F04	PFP Test Register (p. 125)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x05	TM A: 01705 B: 03705 MT A: 01F05 B: 03F05	PFP Ingress Status Monitor Register - 1 (p. 126)

Table 18 Indirect Registers Map (Part 5 of 8)

Module Base Address	Block Base Name	Block Base Address	Register Offset	Indirect Register Address 0x	Register Description
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x06	TM A: 01706 B: 03706 MT A: 01F06 B: 03F06	PFP Ingress Status Monitor Register - 2 (p. 126)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x07	TM A: 01707 B: 03707 MT A: 01F07 B: 03F07	PFP Ingress Status Monitor Register - 3 (p. 126)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x08	TM A: 01708 B: 03708 MT A: 01F08 B: 03F08	PFP Ingress Status Monitor Register - 4 (p. 126)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x09	TM A: 01709 B: 03709 MT A: 01F09 B: 03F09	PFP Egress Status Monitor Register - 1 (p. 127)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x0A	TM A: 0170A B: 0370A MT A: 01F0A B: 03F0A	PFP Egress Status Monitor Register - 2 (p. 127)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x0B	TM A: 0170B B: 0370B MT A: 01F0B B: 03F0B	PFP Egress Status Monitor Register - 3 (p. 127)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x0C	TM A: 0170C B: 0370C MT A: 01F0C B: 03F0C	PFP Egress Status Monitor Register - 4 (p. 127)
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x0D	TM A: 0170D B: 0370D MT A: 01F0D B: 03F0D	PFP Internal Parity Error Indication Register (p. 127)

Table 18 Indirect Registers Map (Part 6 of 8)

Module Base Address	Block Base Name	Block Base Address	Register Offset	Indirect Register Address 0x	Register Description
A (TM) B (TM) A (MT) B (MT)	TM_PFP_REG MT_PFP_REG	TM - 0x1700 MT - 0x1F00	0x0E	TM A: 0170E B: 0370E MT A: 01F0E B: 03F0E	PFP Maximum Packet Length Register (p. 128)
B: 0x2000	AUXILIARY	0x0A00	0x00	B: 02A00	Auxiliary Interface Enable Register (p. 129)
B: 0x2000	AUXILIARY	0x0A00	0x01	B: 02A01	Auxiliary Interface Configuration Register (p. 129)
B: 0x2000	AUXILIARY	0x0A00	0x02	B: 02A02	Auxiliary Extension Buffer Configuration Register (p. 129)
B: 0x2000	AUXILIARY	0x0A00	0x03	B: 02A03	Auxiliary Clock Monitor Status Register) (p. 130)
B: 0x2000	AUXILIARY	0x0A00	0x04	B: 02A04	External Memory Test Control Register (p. 130)
B: 0x2000	AUXILIARY	0x0A00	0x05	B: 02A05	External Memory Test Results Register (p. 131)
B: 0x2000	AUXILIARY	0x0A00	0x07	B: 02A07	Auxiliary Early Backpressure Threshold Register (p. 131)
B: 0x2000	AUXILIARY	0x0A00	0x08	B: 02A08	Auxiliary Packet Mode Configuration Register (p. 131)
B: 0x2000	AUXILIARY	0x0A00	0x0E	B: 02A0E	HSTL Test Register (p. 131)
B: 0x2000	AUXILIARY	0x0A00	0x0F	B: 02A0F	Auxiliary Automatic Impedance Matching Control Register (p. 132)
B: 0x2000	AUXILIARY	0x0A00	0x12	B: 02A12	Auxiliary Synchronization Status Register (p. 132)
B: 0x2000	AUXILIARY	0x0A00	0x13	B: 02A13	Auxiliary Initialization Control Register (p. 133)
B: 0x2000	PRGD	0x0B00	0x00	A: 00B00	Enable Control Register (p. 133)
B: 0x2000	PRGD	0x0B00	0x01	A: 00B01	Feedback Configuration Register (p. 133)
B: 0x2000	PRGD	0x0B00	0x02	A: 00B02	Bandwidth Control Register (p. 133)
B: 0x2000	PRGD	0x0B00	0x03	A: 00B03 B: 02B03	Packet Length Register (p. 134)
B: 0x2000	PRGD	0x0B00	0x04	A: 00B04 B: 02B04	Burst Size Register (p. 134)
B: 0x2000	PRGD	0x0B00	0x05	A: 00B05 B: 02B05	Random Control Register (p. 134)
B: 0x2000	PRGD	0x0B00	0x06	A: 00B06 B: 02B06	LID Register (p. 135)
B: 0x2000	PRGD	0x0B00	0x07	A: 00B07 B: 02B07	Synchronization Register (p. 135)
B: 0x2000	PRGD	0x0B00	0x08	A: 00B08 B: 02B08	Bit Error Insertion Register (p. 135)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x00	A: 00F00 B: 02F00	PMON Event Interrupt Indication Register (p. 136)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x01	A: 00F01 B: 02F01	PMON Event Interrupt Enable Register (p. 139)

Table 18 Indirect Registers Map (Part 7 of 8)

Module Base Address	Block Base Name	Block Base Address	Register Offset	Indirect Register Address 0x	Register Description
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x02-0x03	A: 00F02 - 00F03 B: 02F02 - 02F03	PMON Buffer T-M Overflow Indication Register (p. 140)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x04-0x05	A: 00F04 - 00F05 B: 02F04 - 02F05	PMON Buffer M-T Overflow Indication Register (p. 141)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x06-0x07	A: 00F06 - 00F07 B: 02F06 - 02F07	PMON Buffer T-M Overflow Interrupt Control Register (p. 141)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x08-0x09	A: 00F08 - 00F09 B: 02F08 - 02F09	PMON Buffer M-T Overflow Interrupt Control Register (p. 141)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x0A	A: 00F0A B: 02F0A	PMON Buffer Overflow Source Register (p. 142)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x0B	A: 00F0B B: 02F0B	PMON T-M Inactive Transfer LP Field Register (p. 142)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x0C	A: 00F0C B: 02F0C	PMON M-T Inactive Transfer LP Field Register (p. 142)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x0D	A: 00F0D B: 02F0D	PMON T-M Illegal SOP Event LID Field Register (p. 142)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x0E	A: 00F0E B: 02F0E	PMON T-M Illegal EOP Event LID Field Register (p. 142)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x0F	A: 00F0F B: 02F0F	PMON M-T Illegal SOP Event LID Field Register (p. 143)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x10	A: 00F10 B: 02F10	PMON M-T Illegal EOP Event LID Field Register (p. 143)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x11	A: 00F11 B: 02F11	PMON T-M Packet Cut-Down LID Field Register (p. 143)
A: 0x0000 B: 0x2000	PMON_EVENT	0x0F00	0x12	A: 00F12 B: 02F12	PMON M-T Packet Cut-Down LID Field Register (p. 143)
A: 0x0000 B: 0x2000	PMON_LID_CNT	0x0C00	0x00-0x17F	A: 00C00 - 00C17 B: 02C00 - 02C17	PMON Per LID Counter Table (p. 144)
A: 0x0000 B: 0x2000	PMON_MODULE_CNT	0x0E00	0x00-0x10	A: 00E00 - 00E10 B: 02E00 - 02E10	PMON Per Module/Interface Counter Table (p. 144)
M: 0x8000	MISC	0x0B00	0x00	M: 08B00	Miscellaneous Registers (p. 145)
M: 0x8000	MISC	0x0B00	0x01	M: 08B01	PMON 1ms Timer Register (p. 145)
M: 0x8000	MISC	0x0B00	0x10-0x12	M: 08B10 - 08B12	GPIO Direction Register (p. 145)
M: 0x8000	MISC	0x0B00	0x13-0x15	M: 08B13 - 08B15	GPIO Level Register (p. 146)
M: 0x8000	MISC	0x0B00	0x16-0x18	M: 08B16 - 08B18	GPIO Link Table (p. 146)
M: 0x8000	MISC	0x0B00	0x30	M: 08B30	Version Number Register (p. 146)
M: 0x8000	MISC	0x0B00	0x32	M: 08B32	Software Version Register (p. 146)

Table 18 Indirect Registers Map (Part 8 of 8)

Direct Registers Description

Note: (1) All direct registers are 8 bits wide.

(2) Unused bits are reserved bits.

(3) A READ to unused/reserved bits returns 0 while a WRITE is ignored.

Miscellaneous Registers

Global Software Reset Register

Field	Read / Write	Bits	Length	Reset State	Description
RST	R/W	0:0	1	0	This field resets the IDT88K8483. Reset automatically runs initialization on both software and hardware. Read 0: Initial state after reset. Write 1: Reset the chip.
Note: Clocks generated by the IDT88K8483 are **not** affected by a software reset.					

Table 19 Global Software Reset Register (Register Offset=0x22)

Microprocessor Registers

Microprocessor Mailbox Input FIFO Data Register

Field	Read / Write	Bits	Length	Reset State	Description
Data	R/W	0:0 - 0:7	8	0	Data is written/downloaded to this field, which is a 32 byte IFIFO, by the host CPU and read by the chip.

Table 20 Microprocessor Mailbox Input FIFO Data Register (Register Offset=0x10)

Microprocessor Mailbox Input FIFO Length Register

Field	Read / Write	Bits	Length	Reset State	Description
Length	R/W	0:0 - 0:5	6	0	This field indicates the number of data bytes that is written to the “data” field in Microprocessor Mailbox Input FIFO Data Register (p. 90) by the host CPU.

Table 21 Microprocessor Mailbox Input FIFO Length Register (Register Offset=0x11)

Microprocessor Mailbox Input FIFO Status Register

Field	Read / Write	Bits	Length	Reset State	Description
IFIFO_STATUS	R	0:0	1	0	This field indicates whether the host CPU (WRITE side) or the IDT88K8483 (READ side) has control of the mailbox input IFIFO. 0:Host CPU (WRITE side) has control of IFIFO. Also indicates that the mailbox input FIFO is empty and data can be written to the FIFO by the host. 1:IDT88K8483 (READ side) has control of IFIFO.

Table 22 Microprocessor Mailbox Input FIFO Status Register (Register Offset=0x14)

Microprocessor Mailbox Output FIFO Data Register

Field	Read / Write	Bits	Length	Reset State	Description
Data	R/W	0:0 - 0:7	8	0	Data is written/downloaded to this field, which is a 32 byte OFIFO, by the IDT88K8483 and read by the host CPU.

Table 23 Microprocessor Mailbox Output FIFO Data Register (Register Offset=0x12)

Microprocessor Mailbox Output FIFO Length Register

Field	Read / Write	Bits	Length	Reset State	Description
Length	R/W	0:0 - 0:5	6	0	The number of data bytes written to the "data" field in the Microprocessor Mailbox Output FIFO Data Register (p. 91), by the IDT88K8483.

Table 24 Microprocessor Mailbox Output FIFO Length Register (Register Offset=0x13)

Microprocessor Mailbox Output FIFO Status Register

Field	Read / Write	Bits	Length	Reset State	Description
OFIFO_STATUS	R	0:0	1	0	Indicates whether the host CPU(READ side) or IDT88K8483 (WRITE side) has control of OFIFO. 0: IDT88K8483 (WRITE side) has control of IFIFO. 1: Host CPU(READ side) has control of IFIFO.

Table 25 Microprocessor Mailbox Input FIFO Status Register (Register Offset=0x15)

Embedded Processor State Register

Field	Read / Write	Bits	Length	Reset State	Description
EP_READY	R	0:0	1	0	This flag indicates whether the chip is ready to download the firmware binary file from the host CPU. This flag is checked before the host CPU downloads to the IDT88K8483. This bit is cleared by reset and will go high after the chip is initialized. 0:Not ready for download. 1:Ready for application s/w download.
EP_RUNNING	R	0:1	1	0	This flag indicates whether the downloading procedure is finished. 0:Download taking place. 1:Download finished.
CHIP_READY	R	0:2	1	0	This bit indicates that the downloaded software has initiated the chip and user can access it. This bit is set by downloaded software and is cleared by reset. 0:Chip not yet ready. 1:Chip is ready to be used.

Table 26 Embedded Processor State Register (Register Offset=0x16)

External Microprocessor Registers

Microprocessor Indirect Access Control Register

Field	Read / Write	Bits	Length	Reset State	Description
ERROR	R	0:0 - 0:5	6	0	Indicates the error code of a READ or WRITE operation. 0: No error.Operation performed successfully Error code- see Table 28 below for description of error codes.
RWN	R/W	0:6	1	0	Indicates the initiation of a read or write operation by the OBC. 0: A write operation is initiated by the OBC. 1: A read operation is initiated by the OBC.
BUSY	R	0:7	1	0	Gives a busy indication if an indirect READ or WRITE is initiated. The flag is set until the operation is completed. 0: Not busy. 1: Busy indication.

Table 27 Microprocessor Indirect Access Control Register (Register Offset=0x1A)

Error Code	Error
1	Reconfiguration attempted without device reset, configuration is allowed only once after reset for this register
2	Multiple LPs mapped to the same LID
3	Multiple LIDs mapped to the same LP
4	Buffer segment assigned exceeds total available segments
5	Buffer segment assigned exceeds total number of queue entries available
6	Configuration modified while link active
7	Undefined address
8	Channel limit exceeded
9 to 0x3C	Reserved
0x3D	Version mismatch
0x3E	Protected register
0x3F	Internal timeout

Table 28 Microprocessor Indirect Access Error Codes

Microprocessor Indirect Access Data Register - 1

Field	Read / Write	Bits	Length	Reset State	Description
DATA[0:7]	R/W	0:0 - 0:7	8	0	This register contains the first byte of the 4 byte data that is to be written to or read from the indirect register.

Table 29 Microprocessor Indirect Access Data Register -1 (Register Offset=0x1B)

Microprocessor Indirect Access Data Register - 2

Field	Read / Write	Bits	Length	Reset State	Description
DATA[8:15]	R/W	0:0 - 0:7	8	0	This register contains the second byte of the 4 byte data that is to be written to or read from the indirect register.

Table 30 Microprocessor Indirect Access Data Register - 2 (Register Offset=0x1C)

Microprocessor Indirect Access Data Register - 3

Field	Read / Write	Bits	Length	Reset State	Description
DATA[16:23]	R/W	0:0 - 0:7	8	0	This register contains the third byte of the 4 byte data that is to be written to or read from the indirect register.

Table 31 Microprocessor Indirect Access Data Register - 3 (Register Offset=0x1D)

Microprocessor Indirect Access Data Register - 4

Field	Read / Write	Bits	Length	Reset State	Description
DATA[24:31]	R/W	0:0 - 0:7	8	0	This register contains the fourth byte of the 4 byte data that is to be written to or read from the indirect register.

Table 32 Microprocessor Indirect Access Data Register - 4 (Register Offset=0x1E)

Microprocessor Indirect Access Address Register - 1

Field	Read / Write	Bits	Length	Reset State	Description
ADDRESS[0:7]	R/W	0:0 - 0:7	8	0	This register contains the first byte of the 2 byte address of the indirect register.

Table 33 Microprocessor Indirect Access Address Register - 1 (Register Offset=0x1F)

Microprocessor Indirect Access Address Register - 2

Field	Read / Write	Bits	Length	Reset State	Description
ADDRESS[8:15]	R/W	0:0 - 0:7	8	0	This register contains the second byte of the 2 byte address of the indirect register.

Table 34 Microprocessor Indirect Access Address Register - 2 (Register Offset=0x20)

Microprocessor Indirect Access Address Register - 3

Field	Read / Write	Bits	Length	Reset State	Description
ADDRESS[16:19]	R/W	0:0 - 0:3	4	0	Reserved. This byte should always be 0x00.

Table 35 Microprocessor Indirect Access Address Register - 3 (Register Offset=0x21)

PFP Insert/extract registers

Note: The PFP insert/extract is controlled by OBC (On Board Controller). Data is inserted into the insert FIFO by the OBC and extracted from the extract FIFO by the OBC.

PFP T-M insert control register for module A

Field	Read/ Write	Bits	Length	Reset State	Description
DATA_AVAILABLE	R/W	0:0	1	0	This field indicates the availability of insert FIFO for T-M insertion. Read 0: FIFO is available Read 1: FIFO not available Write 1: Launch data after writing transfer and overhead into the FIFO.
Note: The DATA_AVAILABLE flag will self clear if FIFO is emptied by PFP. This event will be forwarded to interrupt module.					

Table 36 PFP T-M insert control register (Register Offset=0x0)

PFP T-M insert data register for module A

Field	Read/ Write	Bits	Length	Reset State	Description
DATA	W	0:0-0:7	8	0	This field holds the data to be written into the insert FIFO.

Table 37 PFP T-M insert data register(Register Offset=0x1)

PFP T-M extract control register for module A

Field	Read/ Write	Bits	Length	Reset State	Description
DATA_AVAILABLE	R/W	0:0	1	0	This bit indicates the availability of data in the extract FIFO. If data is available, then it is extracted from the FIFO. Read 0: Data is not available in the FIFO. Read 1: Data is available in the FIFO. Write 0: Clears the extract FIFO.
Note: After data is extracted from the FIFO, a transfer extract event will be forwarded to the interrupt module.					

Table 38 PFP T-M extract control register (Register Offset=0x2)

PFP T-M extract data register for module A

Field	Read/ Write	Bits	Length	Reset State	Description
DATA	R	0:0-0:7	8	0	This field holds the content read from the FIFO.

Table 39 PFP T-M extract data register (Register Offset=0x3)

PFP M-T insert control register for module A

Field	Read/ Write	Bits	Length	Reset State	Description
DATA_AVAILABLE	R/W	0:0	1	0	This field indicates the availability of insert FIFO for M-T insertion. Read 0: FIFO is available Read 1: FIFO not available Write 1: Launch data after writing transfer and overhead into the FIFO.
Note: The DATA_AVAILABLE flag will self clear if FIFO is emptied by PFP. This event will be forwarded to interrupt module.					

Table 40 PFP M-T insert control register (Register Offset=0x4)

PFP M-T insert data register for module A

Field	Read/ Write	Bits	Length	Reset State	Description
DATA	W	0:0-0:7	8	0	The content to be inserted into the insert FIFO is written into this field.

Table 41 PFP M-T insert data register (Register Offset=0x5)

PFP M-T extract control register for module A

Field	Read/ Write	Bits	Length	Reset State	Description
DATA_AVAILABLE	R/W	0:0	1	0	This bit indicates the availability of data in the extract FIFO. If data is available, then it is extracted from the FIFO. Read 0: Data is not available in the FIFO. Read 1: Data is available in the FIFO. Write 0: Clears the FIFO.
Note: After data is extracted from the FIFO, a transfer extract event will be forwarded to the interrupt module.					

Table 42 PFP M-T extract control register (Register Offset=0x6)

PFP M-T extract data register for module A

Field	Read/ Write	Bits	Length	Reset State	Description
DATA	R	0:0-0:7	8	0	This field holds the content extracted from the FIFO.

Table 43 PFP M-T extract data register (Register Offset=0x7)

Interrupt Registers

Primary Interrupt Indication Register

Field	Read / Write	Bits	Length	Reset State	Description
MODULE_A	R/W	0:0	1	0	This field capture events in module A. Read 0: Normal operation of module A. Read 1: An event is captured in module A. Write 1: This field is cleared.
MODULE_B	R/W	0:1	1	0	This field capture events in module B. Read 0: Normal operation of module B. Read 1: An event is captured in module B. Write 1: This field is cleared.
COMMON	R/W	0:2	1	0	This field capture events in module M. Read 0: Normal operation of module M. Read 1: An event is captured in module M. Write 1: This field is cleared.

Table 44 Primary Interrupt Indication Register (Register Offset=0x08)

Primary Interrupt Enable Register

Field	Read / Write	Bits	Length	Reset State	Description
MODULE_A_EN	R/W	0:0	1	0	This field enables an interrupt to be generated if an event is captured in MODULE_A field in Primary Interrupt Indication Register (p. 98). 0: Disable. 1: Enable.
MODULE_B_EN	R/W	0:1	1	0	This field enables an interrupt to be generated if an event is captured in MODULE_B field in Primary Interrupt Indication Register (p. 98). 0: Disable. 1: Enable.
COMMON_EN	R/W	0:2	1	0	This field enables an interrupt to be generated if an event is captured in COMMON field in Primary Interrupt Indication Register (p. 98). 0: Disable. 1: Enable.

Table 45 Primary Interrupt Enable Register (Register Offset=0x09)

Note: Please refer to Interrupt Scheme (p. 64) for an explanation of the interrupt scheme.

Secondary Interrupt Module A Indication Register

Field	Read / Write	Bits	Length	Reset State	Description
SPI-MT EXTRACT	R/W	0:0	1	0	This bit indicates when a PFP M-T extraction event takes place in module A. Read 0: No extraction. Read 1: An extraction event has occurred in the PFP M-T locker in module A. Write 1: Clear this field.
SPI-TM EXTRACT	R/W	0:1	1	0	This bit indicates when a PFP T-M extraction event takes place in module A. Read 0: No extraction. Read 1: An extraction event has occurred in the PFP T-M locker in module A. Write 1: Clear this field.
SPI-TM INSERT	R/W	0:2	1	0	This bit indicates when a PFP T-M insertion event takes place in module A. Read 0: No extraction. Read 1: An insertion event has occurred in the PFP T-M locker in module A. Write 1: Clear this field.
SPI-MTINSERT	R/W	0:3	1	0	This bit indicates when a PFP M-T insertion event takes place in module A. Read 0: No extraction. Read 1: An insertion event has occurred in the PFP M-T locker in module A. Write 1: Clear this field
PMON	R	0:4	1	0	Indicates if a PMON event has occurred.

Table 46 Secondary Module Indication Register (Register Offset=0x0A.)

Secondary Interrupt Module A Enable Register

Field	Read / Write	Bits	Length	Reset State	Description
SPI-MTEXTRACT_EN	R/W	0:0	1	0	This field enables an interrupt to be generated if an event is captured in "SPI-MT EXTRACT" field in the Secondary Interrupt Module A Indication Register (p. 100) 0: Disable. 1: Enable.
SPI-TMEXTRACT_EN	R/W	0:1	1	0	This field enables an interrupt to be generated if an event is captured in "SPI-TM EXTRACT" field in the Secondary Interrupt Module A Indication Register (p. 100). 0: Disable. 1: Enable.
SPI-TMINSERT_EN	R/W	0:2	1	0	This field enables an interrupt to be generated if an event is captured in "SPI-TM INSERT" field in the Secondary Interrupt Module A Indication Register (p. 100). 0: Disable. 1: Enable.
SPI-MTINSERT_EN	R/W	0:3	1	0	This field enables an interrupt to be generated if an event is captured in "SPI-MT INSERT" field in the Secondary Interrupt Module A Indication Register (p. 100). 0: Disable. 1: Enable.
PMON_EN	R/W	0:4	1	0	This field enables an interrupt to be generated if an event is captured in PMON field in Secondary Interrupt Module A Indication Register (p. 100). 0: Disable. 1: Enable.
Note: Writing a 1 to any field in this register, causes an interrupt to be generated based on the occurrence of that particular event indicated in the corresponding field in Table 46. The interrupt appears as an active low on the **INTB** pin in the microprocessor interface.					

Table 47 Secondary Module Enable Register (Register Offset=0x0B)

Secondary Interrupt Module B Indication Register

Field	Read / Write	Bits	Length	Reset State	Description
Reserved		0:0 - 0:4			
PMON	R	0:4	1	0	Indicates if a PMON event has occurred.

Table 48 Secondary interrupt module B Indication register(Register Offset=0xC)

Secondary Interrupt Module B Enable Register

Field	Read / Write	Bits	Length	Reset State	Description
Reserved		0:0 - 0:3	4		
PMON_EN	R	0:4	1	0	This field enables an interrupt to be generated if an event is captured in PMON field in Secondary Interrupt Module B Indication Register (p. 101). 0: Disable. 1: Enable.

Table 49 Secondary Interrupt module B enable register (Register Offset=0xD)

Secondary Interrupt COMMON Indication Register

Field	Read / Write	Bits	Length	Reset State	Description
TIMEBASE	R/W	0:0	1	0	This field indicates an event captured in the timebase. Read 0: No event is generated. Read 1: An event is generated by a timebase trigger. Write 1: Clear the field.
INDIRECT_ACC	R/W	0:1	1	0	This field indicates an event captured in the indirect access. Read 0: No event is generated. Read 1: An event is generated due to an invalid indirect access sequence. Write 1: Clear the field.
I_FIFO_READY	R/W	0:2	1	1	This field indicates when the embedded processor is ready to accept data through the I_FIFO Read 0: I_FIFO not ready to accept data. Read 1: I_FIFO ready to accept data. Write 1: Resets the field.
I_FIFO_OFLOW	R/W	0:3	1	0	This field indicates if the mailbox I_FIFO is oveflowed. Read 0: No overflow in mailbox I_FIFO. Read 1: Overflow in mailbox I_FIFO. An attempt to write more than 32 bytes generates this interrupt. Write 1: Clears this field.
O_FIFO_MSG	R/W	0:4	1	0	This field indicates when the embedded processor has data in its mailbox O_FIFO Read 0: No data in present in O_FIFO. Read 1: Data is present in O_FIFO. Write 1: Resets the bit.
SOC	R/W	0:5	1	0	SOC trigger
10ms	R/W	0:6	1	0	This field generates a 10ms timer event based on the 1ms timer. Read 0: 10ms timer event is not generated. Read 1: 10ms timer event is generated. Write 1: Resets the field.

Table 50 Interrupt secondary COMMON indication register (Register Offset=0xe)

Secondary Interrupt COMMON Enable Register

Field	Read / Write	Bits	Length	Reset State	Description
TIMEBASE_EN	R/W	0:0	1	0	This field enables an interrupt to be generated if an event is captured in "TIMEBASE" field in the Secondary Interrupt COMMON Indication Register (p. 102).The interrupt appears as an active low on the INTB pin in the microprocessor interface. 0: Disable. 1: Enable.
INDIRECT_ACC_EN	R/W	0:1	1	0	This field enables an interrupt to be generated if an event is captured in "INDIRECT_ACC" field in the Secondary Interrupt COMMON Indication Register (p. 102).The interrupt appears as an active low on the INTB pin in the microprocessor interface. 0: Disable. 1: Enable.
I_FIFO_READY_EN	R/W	0:2	1	0	This field enables an interrupt to be generated if an event is captured in "I_FIFO_READY" field in the Secondary Interrupt COMMON Indication Register (p. 102).The interrupt appears as an active low on the INTB pin in the microprocessor interface. 0: Disable. 1: Enable.
I_FIFO_OFLOW_EN	R/W	0:3	1	0	This field enables an interrupt to be generated if an event is captured in "I_FIFO_OFLOW" field in the Secondary Interrupt COMMON Indication Register (p. 102).The interrupt appears as an active low on the INTB pin in the microprocessor interface. 0: Disable. 1: Enable.
O_FIFO_MSG_EN	R/W	0:4	1	0	This field enables an interrupt to be generated if an event is captured in O_FIFO_MSG field in the Secondary Interrupt COMMON Indication Register (p. 102).The interrupt appears as an active low on the INTB pin in the microprocessor interface. 0: Disable. 1: Enable.
SOC_EN	R/W	0:5	1	0	This field enables an interrupt to be generated if an event is captured in "SOC" field in the Secondary Interrupt COMMON Indication Register (p. 102).The interrupt appears as an active low on the INTB pin in the microprocessor interface. 0: Disable. 1: Enable.
10ms_EN	R/W	0:6	1	0	This field enables an interrupt to be generated if an event is captured in "10ms" field in the Secondary Interrupt COMMON Indication Register (p. 102).The interrupt appears as an active low on the INTB pin in the microprocessor interface. 0: Disable. 1: Enable.
Note: Writing a 1 to any field in this register, causes an interrupt to be generated based on the occurrence of that particular event indicated in the corresponding field in Table 50. The interrupt appears as an active low on the **INTB** pin in the microprocessor interface.					

Table 51 Interrupt Secondary COMMON Enable Register (register_offset=0xf)

Indirect Registers Description

Note: (1) All indirect registers are 32 bits wide.

(2) Treat unused bits as reserved bits.

(3) A READ to unused/reserved bits returns 0 while a WRITE is ignored.

Clock Registers

MCLK Divider Sticky Register

Field	Read / Write	Bits	Length	Reset State	Description
N	R/W	0:0-0:1	2	11	Selects the frequency of the MCLK. 00: F/2. 01: F/3. 10: F/4. 11: F/5.
Note: (1) "Sticky" means that the register value does not change during software reset. (2) MCLK is generated by the clock generator type M and is used for generic interface, the PFP block and the PMON block.Please refer to Figure 36 Clock Generator Type M p.70"Clock Generator Type M" on page 70 for MCLK discussion.					

Table 52 MCLK Divider Sticky Register (Block Base=0x0a00, Register Offset=0x00)

Clock Control Input Status Register

Field	Read / Write	Bits	Length	Reset State	Description
DIV_FOUR	R	0:0	1	Pin input	Reflects the state of the external configuration signal DIV4. This signal selects the prescaler frequency to divide by 1 or 4. 0: Configures the prescaler frequency to divide by 1. Full rate. 1: Configures the prescaler frequency to divide by 4. Quarter rate.
CK_SEL_A	R	0:1	1	Pin input	Reflects the value of the external configuration signal SPI4A_CLK_SEL. This signal configures the divider1 frequency to divide by 2 or 8. 0: Divide by 2. 1: Divide by 8.
CK_SEL_B	R	0:2	1	Pin input	Reflects the value of the external configuration signal SPI4B_CLK_SEL. This signal configures the divider1 frequency to divide by 2 or 8. 0: Divide by 2. 1: Divide by 8.
CK_SEL_M	R	0:3	1	Pin input	Reflects the value of the external configuration signal SPI4M_CLK_SEL. This signal configures the divider1 frequency to divide by 2 or 8. 0: Divide by 2. 1: Divide by 8.
Note: Please refer to CLK_SEL signals configuration (p. 69) and Figure 36 Clock Generator Type M p.70 for clock description.					

Table 53 Clock Control Input Status Register (Block Base=0x0a00, Register Offset=0x01)

SPI-4 Registers

SPI-4 Ingress LP to LID Mapping Table

Field	Read / Write	Bits	Length	Reset State	Description
N	R/W	0:0 - 0:5	6	0	LID number.This field maps the LP to the LID in the PFP and can take any 1 of 64 possible LID values. The LP number is the register offset. Refer to Figure 3 and Figure 4 for LID information.
P	R/W	0:6	1	0	Selects module A or module B ingress, valid for main. 0:Module A. 1:Module B.
Reserved	R	0: 7	1	0	Reserved bit.
ENABLE	R/W	1:0	1	0	Enables or disables this LP connection to the LID. 0:Disable. 1:Enable.

Table 54 SPI-4 Ingress LP to LID Mapping Table (Block Base=0x0000, Register Offset=0x00-0xff)

SPI-4 Ingress Calendar 0 Table

Field	Read / Write	Bits	Length	Reset State	Description
LP	R/W	0:7	8	0xFF	The LP value programmed schedules a status channel update according to the calendar sequence.
Note: (1)There are 128 table entries for SPI-4 main interface and 64 table entries for SPI-4 tributary interface. (2)The IDT88K8483 and the attached device must have identical calendars for ingress and the attached egress device.					

Table 55 SPI-4 Ingress Calendar 0 Table (Block Base=0x0100, Register Offset=0x00-0x3f/0x7f)

SPI-4 Ingress Calendar 1 Table

Field	Read / Write	Bits	Length	Reset State	Description
LP	R/W	0:7	8	0xFF	The LP value programmed schedules a status channel update according to the calendar sequence.
Note: (1)There are 128 table entries for SPI-4 main interface and 64 table entries for SPI-4 tributary interface. (2)The IDT88K8483 and the attached device must have identical calendars for ingress and the attached egress device.					

Table 56 Ingress Calendar 1 Table (Block Base=0x0200, Register Offset=0x00-0x3f/0x7f)

SPI-4 Interface Enable Register

Field	Read / Write	Bits	Length	Reset State	Description
SPI4_EN	R/W	0:0	1	0	This bit enables/disables the SPI-4 interface ingress path. The SPI-4 ingress path is disabled during reset and while configuring the port and is then enabled for normal use. 0: Disable. 1: Enable.
SPI4_PDN	R/W	0:1	1	0	SPI4 interface power down mode. 0:Power up. 1:Power down or disable the SPI4 LVDS I/O, except the clock.
Note:	(1) The SPI4 interface has to be configured before enabling the interface				

Table 57 SPI-4 Interface Enable Register (Block Base= 0x0300, Register Offset=0x00)

SPI-4 Ingress Configuration Register

Field	Read / Write	Bits	Length	Reset State	Description
I_INSYNC_THR	R/W	0:0-0:4	5	0x1F	The number of consecutive error free DIP-4 that need to be detected before the SPI-4 ingress data channel is synchronized. The actual number of error free DIP 4 that need to be detected is I_INSYNC_THR+1.
I_CLK_EDGE	R/W	0:5	1	1	Indicates the active edge of the status clock in LVTTL mode. 0:The status information is output at the rising edge of the status clock. 1:The status information is output at the falling edge of the status clock.
I_LOW	R/W	0:6	1	1	This bit should be set to '0' or '1'depending on the frequency of the ingress status clock output when the status channel is selected to run in LVDS mode (LVDS_STA bit inTable 62 indicates a '1') 0: ISCLK clock is higher than or equal to 200 MHz. 1: ISCLK clock is lower than 200 MHz.
Reserved	R	0:7	1	0	Reserved bits.
I_OUTSYNC_THR	R/W	1:0-1:3	4	0xF	Indicates the number of consecutive DIP4 errors that need to be detected before the ingress data channel changes from in sync state to out of sync state
Note: Please refer to Figure 16 for an illustration of out of sync and in sync state.					

Table 58 SPI-4 Ingress Configuration Register (Block Base=0x0300, Register Offset=0x01)

SPI-4 Ingress Training Parameter Register

Field	Read / Write	Bits	Length	Reset State	Description
FIFO_MAX_T	R/W	0:0-2:7	24	0	The SPI-4 ingress FIFO_MAX_T field is the maximum time interval between scheduling of training sequences on the FIFO status path interface. The units are in 2^8 SPI-4 data cycles.
ALPHA_FIFO	R/W	3:0-3:7	8	0	The SPI-4 ingress ALPHA_FIFO field is the number of repetitions of the status training sequence that must be scheduled every FIFO_MAX_T cycles. The value for alpha used is actually one more than the ALPHA_FIFO value programmed into the ALPHA_FIFO field.
Note: The purpose of the FIFO status path training sequence is for the deskew of bit arrival times on the FIFO status and control lines.					

Table 59 SPI-4 Ingress Training Parameter Register (Block base=0x0300, Register Offset=0x02)

SPI-4 Ingress Calendar 0 Configuration Register.

Field	Read / Write	Bits	Length	Reset State	Description
I_CAL_M	R/W	0:0-0:7	8	0x01	The I_CAL_M value programmed defines the number of times the calendar 0 sequence is repeated before a DIP-2 parity and "1 1" framing words are inserted[1]. The actual CALENDAR_M[3] value used is one more than the value programmed into the I_CAL_M field.
I_CAL_LEN	R/W	1:0-1:6	7	0x7	Indicates the length of the ingress calendar 0[2].The actual calendar length CALENDAR_LEN[3] is I_CAL_LEN+1. In LVTTL mode, the I_CAL_LEN can be programmed with any value. In LVDS mode, the I_CAL_LEN should be programmed with 4n-1, where n is an integer.
Note: [1]If the I_CSW_EN bit in SPI4 Ingress Calendar Switch Control Register (p. 109) is set to 1,then the I_CAL_M value defines the number of times the calendar sequence is repeated before a DIP2 parity,'1 1' framing word and calendar selection word are inserted. [2]The calendar length CALENDAR_M must be at least as large as the number of active SPI-4 ingress LPs. CALENDAR_M must match the number of entries in the SPI-4 Ingress Calendar 0 Table (p. 105) [3]CALENDAR_LEN and CALENDAR_M are described in the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1).					

Table 60 SPI-4 Ingress Calendar 0 Configuration Register (Block Base=0x0300, Register Offset=0x03)

SPI-4 Ingress Calendar 1 Configuration Register

Field	Read / Write	Bits	Length	Reset State	Description
I_CAL_M	R/W	0:0-0:7	8	0x01	The I_CAL_M value programmed defines the number of times the calendar 1 sequence is repeated before a DIP-2 parity and "1 1" framing words are inserted[1]. The actual CALENDAR_M[3] value used is one more than the value programmed into the I_CAL_M field.
I_CAL_LEN	R/W	1:0-1:6	7	0x7	Indicates the length of the ingress calendar 1[2]. The actual calendar length CALENDAR_LEN[3] is I_CAL_LEN+1. In LVTTL mode, the I_CAL_LEN can be programmed with any value. In LVDS mode, the I_CAL_LEN should be programmed with 4n-1, where n is an integer.

Note:
[1]If the I_CSW_EN bit in SPI4 Ingress Calendar Switch Control Register (p. 109) is set to 1,then the I_CAL_M value defines the number of times the calendar sequence is repeated before a DIP2 parity,'1 1' framing word and calendar selection word are inserted.
[2]The calendar length CALENDAR_M must be at least as large as the number of active SPI-4 ingress LPs. CALENDAR_M must match the number of entries in the SPI-4 Ingress Calendar 1 Table (p. 105)
[3]CALENDAR_LEN and CALENDAR_M are described in the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1).

Table 61 SPI-4 Ingress Calendar 1 Configuration Register (Block base=0x0300, Register Offset=0x04)

SPI-4 Ingress Status Register

Field	Read / Write	Bits	Length	Reset State	Description
I_SYNCV	R	0:0	1	0	Describes the synchronization state of the SPI-4 ingress data path. Refer to Figure 16 SPI-4 Ingress State Machine p.44 for an illustration of out of sync and in sync state. 0:SPI-4 ingress data path is out of synchronization 1:SPI-4 ingress data path is in synchronization
I_DSK_OOR	R	0:1	1	0	Indicates the state of the de-skew block in the ingress datapath.Refer to Figure 15 SPI-4 Ingress Block Diagram p.43 for de-skew overview. 0: SPI-4 ingress data path de-skew is within range. 1: SPI-4 ingress data path de-skew is out of range.
DCLK_AV	R	0:2	1	0	Describes the availability state of the SPI-4 ingress data clock. 0:SPI-4 ingress data clock is not available. 1:SPI-4 ingress data clock is available.
LVDS_STA	R	0:3	1	X	The SPI-4 ingress status channel mode (LVDS/LVTTL) is configured by LVDSSTA pin and this pin's level is indicated in the LVDS_STA field. 0:LVTTL mode. 1:LVDS mode.

Table 62 SPI-4 Ingress Status Register (Block base=0x0300, Register Offset=0x05)

SPI-4 Ingress Diagnostics Register

Field	Read / Write	Bits	Length	Reset State	Description
I_FORCE_TRAIN	R/W	0:0	1	0	This field is used to force continuous training on the SPI-4 ingress status interface. 0:Normal status channel operation. 1:Force continuous training on the SPI-4 ingress status interface.
I_ERR_INS	R/W	0:1	1	0	This field is used to insert the number of DIP-2 errors on the SPI-4 ingress status interface programmed into the I_DIP_NUM field. After the DIP-2 errors are inserted, the I_ERR_INS field will clear itself. 0:Normal status channel operation. 1:Insert DIP-2 errors on the SPI-4 ingress status interface.
I_DIP_NUM	R/W	0:2-0:5	4	0	This field is used to program the number of DIP-2 errors to be inserted when the field I_ERR_INS is set to '1'. The number programmed should be less than 16.
Note: The purpose of the status channel training sequence is for the deskew of status and clock signals and for the alignment between the 2 status signals.					

Table 63 SPI-4 Ingress Diagnostics Register (Block base=0x0300, Register Offset=0x06)

SPI-4 Ingress Automatic Alignment Control Register

Field	Read / Write	Bits	Length	Reset State	Description
AUTO_ALIGN	R/W	0:0	1	0	This field enables or disables automatic alignment for the incoming LVDS data bits in the data path. This register is used for test purposes. 0:Auto alignment is used for test mode. 1:Auto alignment is automatic.

Table 64 SPI-4 Ingress Automatic Alignment Control Register (Block base=0x0300, Register Offset=0x07)

SPI4 Ingress Calendar Switch Control Register

Field	Read / Write	Bits	Length	Reset State	Description
I_CSW_EN	R/W	0:0	1	0	The I_CSW_EN field is used to enable the switching of active calendars and works together with CAL_SEL.Refer to Table 66 for calendar selection.
CAL_SEL	R/W	0:1	1	0	This field is used to select calendar_0 or calendar_1. This bit is valid only if I_CSW_EN is set to 1. Refer to Table 66 for calendar selection.
I_DIP_CSW	R/W	0:2	1	1	This field describes the DIP-2 computation method based on the setting of I_CSW_EN.Please refer toTable 67 for bit setting.
Note: Refer to the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1) for more details about calendar implementation.					

Table 65 SPI-4 Ingress Calendar Switch Control Register (Block base=0x0300, Register Offset=0x08)

CAL_SEL	I_CSW_EN	Description
0	1	Selects Calendar 0.Calendar selection word is fixed to 01b and is placed after framing pattern.
1	1	Selects Calendar 1.Calendar selection word is fixed to 10b and is placed after framing pattern.
X	0	Selects Calendar 0.

Table 66 Ingress Calendar Switch Register: Bit CAL_SEL

I_DIP_CSW	I_CSW_EN	Description
X	0	DIP2 is computed over all preceding status indications after last '11' framing pattern.
1	1	DIP2 is computed over all preceding status indications after last '11' framing pattern, including the calendar selection word, which is fixed at 10b.
0	1	DIP2 is computed over all preceding status indications after last '11' framing pattern, excluding the calendar selection word.

Table 67 Ingress calendar Switch Register: Bit I_DIP_CSW

SPI-4 Ingress Fill Level Register

Field	Read / Write	Bits	Length	Reset State	Description
FILL_CUR	R	0:0-0:5	6	0x0	Indicates the current fill level of the ingress locker. Since this is a real-time register, the value read from it will change rapidly and is used for internal diagnostics only.

Table 68 SPI-4 Ingress Fill Level Register (Block base=0x0300, Register offset=0x0B-0x0C)

There are 2 registers for SPI-4 main interface.

SPI-4 Ingress Max Fill Level Register

Field	Read / Write	Bits	Length	Reset State	Description
FILL_MAX	R/Clear	0:0-0:5	6	0x0	Indicates the maximum fill level of the ingress locker since the time of the last read of this register. This register is cleared after reading.

Table 69 SPI-4 Ingress Max Fill Level Register (Block Base=0x0300, Register Offset=0x0D-0x0E

There are 2 registers for SPI-4 main interface.

SPI-4 Ingress WATERMARK Register

Field	Read / Write	Bits	Length	Reset State	Description
WATERMARK	R/W	0:0-0:4	5	0x0d	Sets the watermark value per PFP.This indicates that if "WATERMARK" number of ingress lockers are full, then backpressure will be initiated for all LIDs on a SPI-4 ingress interface.
Note:(1) 0x1F is the highest watermark that can be set, meaning that the ingress buffer will be full before backpressure will be initiated on a SPI-4 ingress inter face PFP. A WATERMARK field value of 0x0F is used to set a watermark for a half-full ingress buffer before tripping backpressure. (2) Per LID backpressure is set in fields THR_STARV and THR_HUNG in the PFP Buffer Segment Assign Table (p. 120)					

Table 70 SPI-4 Ingress Watermark Register (Block Base=0x0300, Register Offset=0x0F-0x10)

There are 2 registers for SPI-4 main interface.

SPI-4 Ingress Training to out of sync threshold Register

Field	Read / Write	Bits	Length	Reset State	Description
STRT_TRAIN	R/W	0:0-0:7	8	0	!=0: If this field is not equal to zero, then the ingress interface goes out of sync if more than STRT_TRAIN times consecutive training pattern is received on its data channel.

Table 71 Ingress Training to out of sync threshold Registe(Block Base=0x0300,Register Offset=0x13)

SPI-4 Egress LID To LP Mapping Table

Field	Read / Write	Bits	Length	Reset State	Description
LP	R/W	0:0-0:7	8	0	LP number. LID to LP map is used to map a LID used internally to a SPI-4 egress logical port.
EN	R/W	1:0	1	0	The EN bit is used to enable or disable the connection of a LID to an LP. 0=LP is disabled 1=LP is enabled
Note: The LID number is equal to the register offset.					

Table 72 SPI-4 Egress LID To LP Mapping Table (Block Base=0x0400, Register Offset=0x00-0x3F/0x7F)

There are 128 table entries for SPI-4 main interface and 64 table entries for SPI-4 tributary interface.

SPI-4 Egress Calendar 0 Table

Field	Read / Write	Bits	Length	Reset State	Description
LP	R/W	0:0-0:7	8	0xFF	The Logical Port value programmed in this field, schedules a status channel update according to the calendar sequence.

Table 73 SPI-4 Egress Calendar 0 Table (Block Base=0x0500, Register Offset=0x00-0x3F/0x7F)

There are 128 table entries for SPI-4 main egress and 64 table entries for SPI-4 tributary egress calendar_0 to schedule the updating of the status channel LPs to the attached device

SPI-4 Egress Calendar 1 Table.

Field	Read / Write	Bits	Length	Reset State	Description
LP	R/W	0:0-0:7	8	0xFF	The Logical Port value programmed in this field schedules a status channel update according to the calendar sequence.

Table 74 SPI-4 Egress Calendar 1 Table (Block Base=0x0600, Register Offset=0x00-0x3F/0x7F)

There are 128 table entries for SPI-4 main egress and 64 table entries for SPI-4 tributary egress calendar_1 to schedule the updating of the status channel LPs to the attached device

SPI-4 Egress Configuration Register

Field	Read / Write	Bits	Length	Reset State	Description
E_INSYNC_THR	R/W	0:0-0:4	5	0x1F	The number of consecutive error free DIP 2 required to make the egress status channel state machine transition from out of sync to in sync.The actual number of error free DIP 2 that need to be detected is E_OUTSYNC_THR+1.
E_CLK_EDGE	R/W	0:5	1	0	This field controls the edge of the status clock in LVTTL mode, at which the status information will be sampled. 0:Sampling is done at rising edge. 1:Sampling is done at falling edge.
E_LOW	R/W	0:6	1	1	For optimum device performance, this bit should be set to '0' or '1' depending on the SPI-4 egress data clock frequency. 0: EDCLK is higher than or equal to 200 MHz. 1: EDCLK is lower than 200 MHz.
NOSTAT	R/W	0:7	1	0	The NOSTAT bit enables the no status channel option. Once NOSTAT is set, the status channel is ignored. There is no DIP-2 error checking, and no status channel updating. The received status is fixed to starving. The data channel is put into the in sync state. 0:Normal status channel operation. 1:No status channel option is selected.
E_OUTSYNC_THR	R/W	1:0-1:3	4	0xF	The number of consecutive DIP 2 errors needed for the egress state to transition from in sync to out of sync.The actual number of DIP 2 errors that need to be detected is E_INSYNC_THR+1.
Note: Please refer to SPI-4 Ingress State Machine (p. 44) for an illustration of out of sync and in sync state.					

Table 75 SPI-4 Egress Configuration Register (Block Base=0x0800, Register Offset=0x01)

SPI-4 Egress Training Parameter Register

Field	Read / Write	Bits	Length	Reset State	Description
DATA_MAX_T	R/W	0:0-2:7	24	0	The SPI-4 egress DATA_MAX_T field is the maximum time interval between scheduling of training sequences on the egress data path interface. The unit is in 2^8 SPI-4 data cycles.
ALPHA	R/W	3:0-3:7	8	0	The SPI-4 egress ALPHA field is the number of repetitions of the data training sequence that must be scheduled every DATA_MAX_T cycles. The value for alpha used is actually one more than the ALPHA value programmed into the ALPHA field.
Note: The purpose of the data path training sequence is for the deskew of bit arrival times on the data and control lines.					

Table 76 SPI-4 Egress Training Parameter Register (Block Base=0x0800, Register Offset=0x02)

SPI-4 Egress Calendar 0 Configuration Register

Field	Read / Write	Bits	Length	Reset State	Description
E_CAL_M	R/W	0:0-0:7	8	0x01	The E_CAL_M value programmed defines the number of times the calendar sequence is repeated before a DIP-2 parity and "1 1" framing words are inserted[1]. The actual CALENDAR_M value used is one more than the value programmed into the E_CAL_M field.
E_CAL_LEN	R/W	1:0-1:6	7	0x07	This field specifies the egress calendar 0 length. In LVTTL mode, the E_CAL_LEN can be programmed with any value. In LVDS mode, it should be programmed with 4n-1, where n is an integer.Indicates the length of the egress calendar 0[2]. The actual calendar length CALENDAR_LEN[3] is E_CAL_LEN+1.

Note:
[1]If the E_CSW_EN bit in SPI-4 Egress Calendar Switch Control Register (p. 116) is set to 1,then the E_CAL_M value defines the number of times the calendar sequence is repeated before a DIP2 parity,'1 1' framing word and calendar selection word are inserted.
[2]The calendar length CALENDAR_M must be at least as large as the number of active SPI-4 egress LPs. CALENDAR_M must match the number of entries in the SPI-4 Egress Calendar 0 Table (p. 111)
[3]CALENDAR_LEN and CALENDAR_M are described in the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1).

Table 77 SPI-4 Egress Calendar 0 Configuration Register (Block Base=0x0800, Register Offset=0x03)

SPI-4 Egress Calendar 1 Configuration Register

Field	Read / Write	Bits	Length	Reset State	Description
E_CAL_M	R/W	0:0-0:7	8	0x01	The E_CAL_M value programmed defines the number of times the calendar sequence is repeated before a DIP-2 parity and "1 1" framing words are inserted[1]. The actual CALENDAR_M value used is one more than the value programmed into the E_CAL_M field.
E_CAL_LEN	R/W	1:0-1:6	7	0x07	This field specifies the egress calendar 1 length. In LVTTL mode, the E_CAL_LEN can be programmed with any value. In LVDS mode, it should be programmed with 4n-1, where n is an integer. Indicates the length of the egress calendar 1[2]. The actual calendar length CALENDAR_LEN[3] is E_CAL_LEN+1.

Note:
[1]If the E_CSW_EN bit in SPI-4 Egress Calendar Switch Control Register (p. 116) is set to 1,then the E_CAL_M value defines the number of times the calendar sequence is repeated before a DIP2 parity,'1 1' framing word and calendar selection word are inserted.
[2]The calendar length CALENDAR_M must be at least as large as the number of active SPI-4 ingress LPs. CALENDAR_M must match the number of entries in the SPI-4 Egress Calendar 1 Configuration Register (p. 114)
[3]CALENDAR_LEN and CALENDAR_M are described in the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1).

Table 78 SPI-4 Egress Calendar 1 Configuration Register (Block Base=0x0800, Register Offset=0x04)

SPI-4 Egress Status Register

Field	Read / Write	Bits	Length	Reset State	Description
E_SYNCV	R	0:0	1	0	Describes the synchronization state of the egress status channel state machine. 0:SPI-4 egress status channel is out of synchronization. 1:SPI-4 egress status channel is in synchronization.
E_DSK_OOR	R	0:1	1	0	Indicates the state of the de-skew block in the egress status path.Refer to Figure 17 for de-skew overview. 0:SPI-4 egress status path de-skew is within range. 1:SPI-4 egress status path de-skew is out of range.
SCLK_AV	R	0:2	1	0	Describes the availability state of the SPI-4 egress status channel clock.This field is cleared if there is no status clock available on LVDS or LVTTL input on a 2048 MCLK hopping window. 0:SPI-4 egress status channel clock not available. 1:SPI-4 egress status channel clock is available.

Table 79 SPI-4 Egress Status Register (Block Base=0x0800, Register Offset=0x05)

SPI-4 Egress Diagnostics Register

Field	Read / Write	Bits	Length	Reset State	Description
E_FORCE_TRAIN	R/W	0:0	1	0	This field is used to force continuous training on the SPI-4 egress datapath. 0:Normal datapath operation. 1:Force continuous training on the SPI-4 egress datapath.
E_ERR_INS	R/W	0:1	1	0	Inserts consecutive DIP-4 error on egress datapath based on the number programmed in the E_DIP_NUM field. After the DIP-4 errors are inserted, the E_ERR_INS field will clear itself. 0: Normal datapath operation. 1: Insert DIP-4 error on the SPI-4 egress datapath.
E_DIP_NUM	R/W	0:2-0:5	4	0	This field is used to program the number of DIP-4 errors to be inserted when the field E_ERR_INS is set to '1'. This number should be less than 16.
BIT_DELAY	R/W	0:6-0:7	2	0	The BIT_DELAY field is used to delay SPI-4 egress data bit line 0 by the number of bits programmed into the BIT_DELAY field. This may be used for diagnostics.
Note: The purpose of the data path training sequence is for the deskew of data and clock signals and for the alignment between the 16 data signals.					

Table 80 SPI-4 Egress Diagnostics Register (Block Base=0x0800, Register Offset=0x06)

SPI-4 Egress Automatic Alignment Control Register

Field	Read / Write	Bits	Length	Reset State	Description
AUTO_ALIGN	R/W	0:0	1	0	This field enables or disables automatic alignment for the incoming LVDS data bits in the status path.This register is used for test purposes. 0:Auto alignment is disabled. 1: Alignment is automatic.

Table 81 SPI-4 Egress Automatic Alignment Control Register (Block Base=0x0800, Register Offset=0x07)

SPI-4 Egress Calendar Switch Control Register

Field	Read / Write	Bits	Length	Reset State	Description
E_CSW_EN	R/W	0:0	1	0	The engress calendar switch enable bit is used to enable the switching of the active calendars following the reception of the calendar selection word on the status channel. 0:Egress calendar switch is disabled. Only SPI-4 egress calendar 0 is used. 1:Egress calendar switch is enabled. Calendar 0 or calendar 1 will automatically be selected depending on the value of the received calendar selection words.
CAL_ID	R	0:1	1	0	MSB of calendar ID word
E_DIP_CSW	R/W	0:2	1	1	This field describes the DIP-2 computation method of the received DIP-2 on the status channel. It is based on the selection of calendar 0 or calendar 1.Refer to Table 67 page 110 for a detailed explanation.
Note: Refer to the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1) for more details about calendar implementation.					

Table 82 SPI-4 Egress Calendar Switch Control Register (Block Base = 0x0800, Register Offset=0x08)

SPI-4 Egress Fill Level Register

Field	Read / Write	Bits	Length	Reset State	Description
FILL_CUR	R	0:0-0:3	4	0	Indicates the current fill level of the egress locker. Since this is a real-time register, the value read from it will change rapidly and is used for internal diagnostics only

Table 83 SPI-4 Egress Fill Level Register (Block Base=0x0800, Register Offset = 0x0B and 0x0C)

There are two registers for SPI-4 main interface.

SPI-4 Egress Max Fill Level Register

Field	Read / Write	Bits	Length	Reset State	Description
FILL_MAX	R/C	0:0-0:3	4	0	Indicates the maximum fill level of the egress locker since the time of the last read of this register. This register is cleared after reading.

Table 84 SPI-4 Egress Max Fill Level Register (Block Base =0x0800, Register Offset = 0x0D and 0x0E)

There are two registers for SPI-4 main interface.

SPI-4 Histogram Measure Launch Register

Field	Read / Write	Bits	Length	Reset State	Description
LANE	R/W	0:0-0:4	5	0	LANE field selects the SPI-4 ingress datapath lanes, control lane or SPI-4 egress associated status channel lanes that will use manual bit alignment. 0:SPI-4 ingress DATA0 lane selected for measurement. x:SPI-4 ingress DATAx lane selected for measurement. 15:SPI-4 ingress DATA15 lane selected for measurement. 16:SPI-4 ingress CTL selected for measurement. 17:SPI-4 egress status 0 lane selected for measurement. 18:SPI-4 egress status 1 lane selected for measurement.
Note: The manual bit alignment is a edge transition histogram measure process. Please refer to Figure 15(Ingress block diagram) and subsequent description for histogram overview. In normal operation bit alignment is automatic and these registers are not used.					

Table 85 SPI-4 Histogram Measure Launch Register (Block Base=0x0900 Register Offset=0x00)

SPI-4 Histogram Measure Status Register

Field	Read / Write	Bits	Length	Reset State	Description
BUSY	R	0:0	1	0	This field is used to observe when the LANE process in Table 85 is busy for manual lane assignment procedures and is self cleared when the process completes.The BUSY field is intended for diagnostics only and is not needed for normal operation. 0:Lane process is complete. 1:Lane process is busy.
ERROR	R	0:1	1	0	This field indicates the result after the manual bit alignment (LANE process) is completed. 0:Successful measure. This field is auto cleared when a new measure is launched. 1:Aborted indication.

Table 86 SPI-4 Histogram Measure Status Register (Block Base=0x0900 Register Offset=0x01)

SPI-4 Histogram Counter Register

Field	Read / Write	Bits	Length	Reset State	Description
C[n]	R	0:0-1:1	10	0	This register holds the histogram measured value. There are 10 registers which keep the statistic value of a HISTOGRAM measure for a particular lane until a new measure is launched. These values indicate the eye opening and jitter for each measured lane.The counter value is used to select the TAP inTable 88.

Table 87 SPI-4 Histogram Counter Register (Block Base=0x0900 Register Offset=0x02-0x0B)

SPI-4 Bit Alignment Result Register

Field	Read / Write	Bits	Length	Reset State	Description
TAP[7:0]	R/W	0:0-0:7	8	0	TAP[3:0] covers the range of taps from 0 to 8. TAP[7:4] covers the range of taps from 5 to 14. The value selected from the counter register field C[n] Table 87, is written into the TAP field. This is used to select the received bit stream from the 10 samples after the HISTOGRAM measure is launched.There are 19 registers in total.
Note: Please refer to SPI-4 Ingress Block Diagram (p. 43) and SPI-4 Egress State Block Diagram (p. 46) for bit alignment overview.					

Table 88 SPI-4 Bit Alignment Result Register (Block Base=0x0900 Register Offset=0x0C-0x1E)

SPI-4 Egress Data Lane Timing Register

Field	Read / Write	Bits	Length	Reset State	Description
DTC0[1:0]	R/W	0:0-0:1	2	0	This register is used to manually align the phase of data lane n by adding between 0.1 and 0.3 clock cycles of delay. DTCn [1:0] is used for adding 0.1 clock cycle units of output delay to the SPI-4 egress data lane n. DTCn[1:0]=0=No added delay. DTCn[1:0]=1=Add 0.1 clock cycle of delay to data lane n. DTCn[1:0]=2=Add 0.2 clock cycles of delay to data lane n. DTCn[1:0]=3=Add 0.3 clock cycles of delay to data lane n.
DTC1[1:0]	R/W	0:2-0:3	2	0	
.	R/W		2	0	
DTC15[1:0]	R/W	3:6-3:7	2	0	

Table 89 SPI-4 Egress Data Lane Timing Control (Block Base=0x0900, Register Offset=0x2A)

SPI-4 Egress Data Control Lane Timing Register

Field	Read / Write	Bits	Length	Reset State	Description
CTLTC[1:0]	R/W	0:0-0:1	2	0	This register is used to manually align the phase of the control lane by adding between 0.1 clock cycle and 0.3 clock cycles of delay. CTLTC [1:0] Used for adding 0.1 clock cycle units of output delay to the SPI-4 egress control output. CTLTC[1:0]=0=No added delay. CTLTC[1:0]=1=Add 0.1 clock cycle of delay to the control output. CTLTC[1:0]=2=Add 0.2 clock cycles of delay to the control output. CTLTC[1:0]=3=Add 0.3 clock cycles of delay to the control output.

Table 90 SPI-4 Egress Data Control Lane Timing Control (Block Base=0x0900, Register Offset=0x2B)

SPI-4 Egress Data Clock Timing Register

Field	Read / Write	Bits	Length	Reset State	Description
DCTC[0:3]	R/W	0:0-0:3	4	0	This register is used to manually align the phase of the SPI-4 egress data clock to the data and control lanes by adding from 0.1 clock cycle to 0.9 clock cycles of delay to the data clock output. Note that the clock delay value is not monotonically related to the value encoded in the bit field [3:0]. **DCTC [3:0]** Used for adding 0.1 clock cycle units of output delay to the SPI-4 egress data clock. [3:0]=0=No added delay [3:0]=1=Add 0.1 clock cycle of delay to the SPI-4 egress data clock. [3:0]=3=Add 0.2 clock cycles of delay to the SPI-4 egress data clock. [3:0]=2=Add 0.3 clock cycles of delay to the SPI-4 egress data clock. [3:0]=7=Add 0.4 clock cycles of delay to the SPI-4 egress data clock. [3:0]=6=Add 0.5 clock cycles of delay to the SPI-4 egress data clock. [3:0]=4=Add 0.6 clock cycles of delay to the SPI-4 egress data clock. [3:0]=5=Add 0.7 clock cycles of delay to the SPI-4 egress data clock. [3:0]=F=Add 0.8 clock cycles of delay to the SPI-4 egress data clock. [3:0]=E=Add 0.9 clock cycles of delay to the SPI-4 egress data clock.

Table 91 SPI-4 Egress Data Clock Timing Control (BlockBase=0x0900, Register Offset=0x2C)

SPI-4 Egress Status Timing Register

Field	Read / Write	Bits	Length	Reset State	Description
STC0[0:1]	R/W	0:0-0:1	2	0	This register is used to manually align the phase of the status lane n by adding from 0.1 clock cycle to 0.3 clock cycles of delay. The STC0[1:0] and STC0[1:0] fields are valid only for LVDS status and are not used for LVTTL status. STCn [1:0] Used for adding 0.1 clock cycle units of output delay to SPI-4 egress status lane n. [1:0]=0=No added delay. [1:0]=1=Add 0.1 clock cycle of delay to status lane n. [1:0]=2=Add 0.2 clock cycles of delay to status lane n. [1:0]=3=Add 0.3 clock cycles of delay to status lane n.
STC1[0:1]	R/W	0:2-0:3	2	0	

Table 92 SPI-4 Egress Status Timing Control (Block Base=0x0900, Register Offset=0x2D)

SPI-4 Egress Status Clock Timing Register

Field	Read / Write	Bits	Length	Reset State	Description
SCTC[0:3]	R/W	0:0-0:3	4	0	This register is used to manually align the phase of the SPI-4 egress status clock to the status outputs by adding from 0.1 clock cycle to 0.9 clock cycles of delay to the status clock output. Note that the clock delay value is not monotonically related to the value encoded in the bit field [3:0]. The SCTC[3:0] field is valid only for LVDS status, not for LVTTL status. SCTC [3:0] Used for adding 0.1 unit intervals of output delay to the SPI-4 egress status clock output. [3:0]=0=No added delay [3:0]=1=Add 0.1 clock cycle of delay t o the SPI-4 egress status clock [3:0]=3=Add 0.2 clock cycles of delay to the SPI-4 egress status clock [3:0]=2=Add 0.3 clock cycles of delay to the SPI-4 egress status clock [3:0]=7=Add 0.4 clock cycles of delay to the SPI-4 egress status clock [3:0]=6=Add 0.5 clock cycles of delay to the SPI-4 egress status clock [3:0]=4=Add 0.6 clock cycles of delay to the SPI-4 egress status clock [3:0]=5=Add 0.7 clock cycles of delay to the SPI-4 egress status clock [3:0]=F=Add 0.8 clock cycles of delay to the SPI-4 egress status clock [3:0]=E=Add 0.9 clock cycles of delay to the SPI-4 egress status clock

Table 93 SPI-4 Egress Status Clock Timing Control (Block Base=0x0900, Register Offset=0x2E)

Packet Fragment Processor (PFP) Registers

PFP Buffer Segment Assign Table

Field	Read / Write	Bits	Length	Reset State	Description
M	R/W	0:0-1:0	9	0	Maximum number of data buffer segments per LID of the available 508 segments in the PFP.
Reserved	R	1:1-1:7	7		
THR_STARV	R/W	2:0-2:7	8	0	Indicates the starving threshold. Status is set to starving if the number of free segments in the data buffer is more than or equal to the starving threshold
THR_HUNG	R/W	3:0-3:7	8	0	Indicates the hungry threshold. Status is set to hungry if the number of free segments in the data buffer is less than or equal to the starving thresholds but greater than or equal to the hungry threshold. Status is set to satisfied if the number of free segments in the data buffer is greater than the hungry threshold.

Table 94 PFP Buffer Segment Assign Table (Block Base=0x01000/0x1800, Register Offset=0x00-0x3F)

There are 64 registers in this table, one for each LID.

PFP Packet Length Thresholds

Field	Read / Write	Bits	Length	Reset State	Description
LEN_MIN	R/W	0:0-0:7	8	0x40	Used to configure the minimum packet length that the PFP is expected to receive. If the packet length is less than LEN_MIN, then the event is detected by the PFP and forwarded to PMON. The value in LEN_MIN does not affect the behavior of the data path and is only intended for diagnostics purposes.
Reserved	R/W	1:0-1:7	8	0	
LEN_MAX	R/W	2:0-3:5	14	0x5EE	Used to configure the maximum packet length that the PFP is expected to receive. If the packet length is greater than LEN_MAX, then the event is detected by PFP and forwarded to PMON. The value in LEN_MAX does not affect the behavior of the data path and is only intended for diagnostics purposes.

Table 95 PFP Packet Length Thresholds (Block Base=0x1100/0x1900, Register Offset=0x00-03F)

There are 64 registers in this table, one for each LID.

PFP Queue Diagnose Table

Field	Read / Write	Bits	Length	Reset State	Description
UNIT	R/W	0:0-1:1	10	0	The number of units waiting in the PFP queue for transfer to the egress interface. A unit corresponds to a packet or packet fragment, depending on the value of PRT_MODE in Table 101
Reserved	R	1:2-2:3	10	0	
READ_POINTER	R/W	2:4-3:7	12	0	The value in this field indicates the circular queue read pointer position.

Table 96 PFP Queue Diagnose Table (Block Base=0x1200/0x1A00, Register Offset=0x00-0x3F)

There are 64 registers in this table, one for each LP.

PFP Packet Diagnose Table

Field	Read / Write	Bits	Length	Reset State	Description
PKT_NUM	R/W	0:0-1:1	10	0	Indicates the number of packets stored in the PFP segmented buffer.

Table 97 PFP Packet Diagnose Table (Block Base=0x1300/0x1B00, Register Offset=0x00-03F)

There are 64 registers in this table, one for each LID.

PFP Egress Burst Size Table

Field	Read / Write	Bits	Length	Reset State	Description
MAX_BURST_S	R/W	0:0-0:3	4	0xF	The maximum data burst size transferred to the egress interface when a starving status signal is received. The actual burst size is equal to (MAX_BURST_S+1)*16 bytes
MAX_BURST_H	R/W	0:4-0:7	4	0xF	The maximum data burst size transferred to the egress interface when a hungry status signal is received. The actual burst size is equal to (MAX_BURST_H+1)*16 bytes.
Note: The MAX_BURST_H and MAX_BURST_S values relate to MaxBurst2 and MaxBurst1 parameters in the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1).					

Table 98 PFP Egress Burst Size Table (Block Base=0x1400/0x1C00, Register Offset=0x00-0x3F)

There are 64 registers in this table, one for each LID.

PFP Egress Weight And Direction Register

Field	Read / Write	Bits	Length	Reset State	Description
DIR[1:0]	R/W	0:0-0:1	2	11	Indicates the PFP LID direction. Each LID has 4 directions. T-M PFP / M-T PFP 00: Main SPI-4 / Tributary SPI-4 01: Redirect / Loopback 10: Extract (OBC for A) (PRBS for B) / Extract (OBC for A) (Auxiliary for B) 11: Discard / Discard
WEIGHT	R/W	0:2	1	0	This field sets the priority mode of the LIDs. This weight is used by the egress server scheduler to service the LIDs when the WEIGHT_EN field in PFP Queue Weighting Enable Register (p. 124) is set to 1. 0: Low priority for this LID, denoted by the register offset. 1:High priority for this LID, denoted by the register offset.
Note: Please refer to page 52 for a detailed explanation of PFP weighing and scheduling.					

Table 99 PFP Egress Weight And Direction Register (Block Base=0x1500/0x1D00, Register Offset=0x00-03F)

There are 64 registers in this table, one for each LID.

PFP Egress Packet Mode Control Registers

Field	Read / Write	Bits	Length	Reset State	Description
PKT_MODE	R/W	0:0	1	0	This field is used to program the PFP egress to interleaved mode or packet mode. 0: Interleaved mode. The LID is eligible to be served by the egress scheduler if there is one or more packet fragment in the queue.The transfer unit is one packet fragment. 1: Packet mode. The LID is eligible to be served by the egress scheduler if there are one or more packets in the data memory.The transfer unit is one packet.
EBP_EN	R/W	0:1	1	0	This control bit enables early backpressure propagation. 0: Normal backpressure. 1:Enable early backpressure propagation.

Table 100 PFP Egress Packet Mode Control Register (Block Base=0x1600/0x1E00, Register Offset=0x00-0x3F)

There are 64 registers, one for each LID.

PFP Link Number Configuration Register

Field	Read / Write	Bits	Length	Reset State	Description
NR_LID	R/W	0:0-0:2	3	0	Link Identifier (LID) number configuration. Configures the maximum number of LIDs that the application will use for this PFP data buffer. Once configured this value should not be changed without resetting the IDT88K8483. NR_LID Maximum number of LIDs 000 1 001 4 010 8 011 16 100 32 101 64

Table 101 PFP Link Number Configuration Register (Block Base=0x1700/0x1F00, Register Offset=0x00)

PFP Buffer Management Configuration Register

Field	Read / Write	Bits	Length	Reset State	Description
BUF_THR	R/W	0:0-1:0	9	0x1c0	Indicates the global threshold for segmented data buffer at which the backpressure is initiated. This field must be configured before the overbooking mode is enabled (OVBK_EN = 1). Unit is the number of LIDs.
OVBK_EN	R/W	1:1	1	0	This indicates the manner in which the 508 data buffer segments in the PFP are managed. 0: Non-overbooking mode.This means that the number of data buffer segments allocated to each LID is limited by the M field in PFP Buffer Segment Assign Table (p. 120). 1:Enable overbooking mode. This means that data buffer segments can now be shared between LIDs up to 8 times the value of M if free segments are available.

Table 102 PFP Buffer Management Configuration Register (Block Base=0x1700/0x1F00, Register Offset=0x01)

PFP Queue Weighting Enable Register

Field	Read / Write	Bits	Length	Reset State	Description
WEIGHT_EN	R/W	0:0	1	0	This field selects which LID data needs to be transmitted first according to its priority set in the field WEIGHT in PFP Egress Weight And Direction Register (p. 122), when non-satisfied status information is received in the FIFO status channel. 0: The egress server scheduler schedules the LIDs in the calendar to be serviced in a two-priority round robin according to the starving, hungry and satisfied status of each LID. A starving status sets the LID priority high, a hungry status sets the priority low. 1: The egress server schedules the LIDs with hungry or starving status to be serviced in a two-priority round robin scheme mode according to a fixed priority scheme. The status values of hungry and starving received in the egress status calendar are merged into a single non-satisfied status. The priority of the LID can be set in the WEIGHT field in the "PFP Egress Weight And Direction Register" on page 122.
Note: Please refer to page 52 for a detailed explanation of PFP priority and scheduling.					

Table 103 PFP Queue Weighting Enable Register (Block Base=0x1700/0x1F00, Register Offset=0x02)

PFP Flow Control Register

Field	Read / Write	Bits	Length	Reset State	Description
CREDIT_EN	R/W	0:0	1	0	This field enables the information received over the FIFO status channel to be interpreted as credit rather than status. 0:Status mode. In status mode the SPI-4 egress state used to schedule each LID remains the same until the received calendar status credit entry for the LID changes value. If the status is hungry or starving, transfers will continue until the status changes to satisfied even if fewer credits have been received than egress transfers. 1:Credit enable. In this mode, the SPI-4 egress will issue one credit's worth data burst for the LID and then wait for another credit from the status channel before issuing another credit burst for that LID.
BURST_EN	R/W	0:1	1	0	This field enables bursts consisting of multiple transfers for the same LID to be made to the egress port buffers. This burst mode modifies the round-robin egress scheduler to prioritize those LIDs having multiple packet fragments or complete packets waiting for transfer. 0: Burst not enabled. The SPI-4 egress can transfer only one fragment of data for the scheduled LID to the egress port buffer. 1: Burst enabled.The SPI-4 egress can transfer more than one data segment to the egress port buffer.

Table 104 PFP Flow Control Register (Block Base=0x1700/0x1F00, Register Offset=0x03)

PFP Test Register

Field	Read / Write	Bits	Length	Reset State	Description
REPEAT	R/W	0:0	1	0	0: Entries in the queue, corresponding to packets or packet fragments stored in the data buffer are deleted once they are processed by the egress server. 1: Entries in the queue are not deleted after they processed by the egress server.
SINGLE_REP	R/W	0:1	1	0	0: Indicates that all 64 LIDs will be repeated. 1: Indicates that only a single LID in field LID_REPEAT will be repeated.
LID_REPEAT	R/W	0:2-0:7	6	0	0: Indicates the repeat operation is valid for all 64 LIDs. LID number: Indicates the repeat operation is valid for a single LID.
STOP	R/W	1:0	1	0	0: Normal operation. 1: Disables the service operation by stopping the egress server.
SINGLE _STOP	R/W	1:1	1	0	0: Stops service operation of all LIDs. 1: Stops service operation of a single LID indicated by LID_STOP.
LID_STOP	R/W	1:2-1:7	6	0	0: Indicates the stop operation is valid for all 64 LIDs. LID number: Indicates the stop operation is valid for a single LID.

Table 105 PFP Test Register (Block Base=0x1700/0x1F00, Register Offset=0x04)

PFP Ingress Status Monitor Register - 1

Field	Read / Write	Bits	Length	Reset State	Description
STATUS[0]	R	0:0-0:1	2	0	Indicates status for LID 0
STATUS[1:15]	R	0:2-3:7	30	0	Indicates status for LIDs 1-15

Note: (1) The status has the same definition as described in the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1)

[MSB, LSB]	Status
10	Satisfied
01	Hungry
00	Starving
11	Reserved

(2) The ingress status reflects the status based on the data buffer fill level.

Table 106 PFP Ingress Status Monitor Register - 1 (Block Base=0x1700/0x1F00, Register Offset=0x05)

PFP Ingress Status Monitor Register - 2

Field	Read / Write	Bits	Length	Reset State	Description
STATUS[16:31]	R	0:0-3:7	32	0x00	Indicates status for LID 16-31

Table 107 PFP Ingress Status Monitor Register - 2 (Block Base=0x1700/0x1F00, Register Offset=0x06)

PFP Ingress Status Monitor Register - 3

Field	Read / Write	Bits	Length	Reset State	Description
STATUS[32:47]	R	0:0-3:7	32	0x00	Indicates status for LID 32-47

Table 108 PFP Ingress Status Monitor Register - 3 (Block Base=0x1700/0x1F00, Register Offset=0x07)

PFP Ingress Status Monitor Register - 4

Field	Read / Write	Bits	Length	Reset State	Description
STATUS[48:63]	R	0:0-3:7	32	0x00	Indicates status for LID 48-63

Table 109 PFP Ingress Status Monitor Register - 4 (Block Base=0x1700/0x1F00, Register Offset=0x08)

PFP Egress Status Monitor Register - 1

Field	Read / Write	Bits	Length	Reset State	Description
STATUS[0:15]	R	0:0-3:7	32	0x00	Indicates status for lid 0-15
Note: (1) The egress status has the same definition as described in the OIF SPI-4 implementation agreement (OIF-SPI-4-02.1) and is shown in PFP Ingress Status Monitor Register - 1 (p. 126) (2) The egress status reflects the status received from the status channel.					

Table 110 PFP Egress Status Monitor Register - 1 (Block Base=0x1700/0x1F00, Register Offset=0x09)

PFP Egress Status Monitor Register - 2

Field	Read / Write	Bits	Length	Reset State	Description
STATUS[16:31]	R	0:0-3:7	32	0x00	Indicates status for lid 16-31

Table 111 PFP Egress Status Monitor Register - 2 (Block Base=0x1700/0x1F00, Register Offset=0x0A)

PFP Egress Status Monitor Register - 3

Field	Read / Write	Bits	Length	Reset State	Description
STATUS[32:47]	R	0:0-3:7	32	0x00	Indicates status for lid 32-47

Table 112 PFP Egress Status Monitor Register - 3 (Block Base=0x1700/0x1F00, Register Offset=0x0B)

PFP Egress Status Monitor Register - 4

Field	Read / Write	Bits	Length	Reset State	Description
STATUS[48:63]	R	0:0-3:7	32	0x00	Indicates status for lid 48-63.

Table 113 PFP Egress Status Monitor Register - 4 (Block Base=0x1700/0x1F00, Register Offset=0x0C)

PFP Internal Parity Error Indication Register

Field	Read / Write	Bits	Length	Reset State	Description
P_ERROR_I	R/W	0:0	1	0	0: Internal memory parity error did not occur. 1:Internal memory parity error occurred. Write 1: Clear the field.
P_ERROR_INS	R/WC	0:1	1	0	Writing 1 generates a single parity error, self clear.

Table 114 PFP Internal Parity Error Indication Register (Block Base=0x1700/0x1F00, Register Offset=0x0D)

PFP Maximum Packet Length Register

Field	Read / Write	Bits	Length	Reset State	Description
MAX_LEN	R/W	0:0-0:5	6	6	This indicates the maximum packet length of the PFP. If maximum packet length is greater than or equal to MAX_LEN*256 bytes, the ingress server will truncate the packet, add SOP/EOP, add error tag accordingly and send cut-down event to PMON. The highest value that MAX_LEN can be set to is 15, 872 bytes.

Table 115 PFP Maximum Packet Length Register (Block Base=0x1700/0x1F00, Register Offset=0x0E)

Auxiliary Registers

Auxiliary Interface Enable Register

Field	Read / Write	Bits	Length	Reset State	Description
AUX_EN	R/W	0:0	1	0	This field enables the auxiliary interface[1]. 0:Disable the auxiliary interface. 1:Enable the auxiliary interface.
AUX_PDN	R/W	0:1	1	0	This field powers down the auxiliary outputs except for the clock. 0:Power up the auxiliary interface. 1:Power down the auxiliary interface.

Note: [1]The interface has to be configured before enabling it.This is done in Auxiliary Interface Configuration Register (p. 129)

[2]The interface has to be powered down before configuring it to the QDR-II interface mode or the generic interface mode

Table 116 Auxiliary Interface Enable Register (Block Base=0x0A00, Register Offset=0x00)

Auxiliary Interface Configuration Register

Field	Read / Write	Bits	Length	Reset State	Description
MEM	R/W	0:0	1	0	This bit configures the auxiliary interface to QDR-II mode or generic mode[1]. 0: Generic interface mode. 1: QDR-II interface mode.
LIDMDF	R/W	0:1	1	0	This bit defines the manner in which the LID in the PFP is mapped to the FIFOs in the QDR-II, for both status channel and data channel. 0: PFP LID x status channel is mapped to FIFO x status channel in the external QDR-II SRAM. FIFO x data channel in the QDR-II SRAM is mapped to the PFP LID x data channel. This setting is used when all PFP LID channels are mapped to QDR-II FIFOs. 1: PFP LID x status channel is mapped to the (FIFO x - LID_offset) status channel in the external QDR-II SRAM. FIFO x data channel in the QDR-II SRAM is mapped to the PFP (LID x+ LID_offset) data channel. This setting is used when some LIDs are mapped to the QDR-II FIFOs and other LIDs are mapped to the egress interface.

Note: [1]The interface has to be powered down before configuring it to the QDR II interface mode or the generic interface mode

Table 117 Auxiliary Interface Configuration Register (Block Base=0x0A00, Register Offset=0x01)

Auxiliary Extension Buffer Configuration Register

Field	Read / Write	Bits	Length	Reset State	Description
EBC[2:0]	R/W	0:2	3	0	Determines the number of FIFOs that are configured in the external QDR-II SRAM. Please refer to Table 119 for more information.

Table 118 Auxiliary Extension Buffer Configuration Register (Block Base=0x0A00, Register Offset=0x02)

EBC[2:0]	Number of FIFO's
3b'000	1
3b'001	4
3b'010	8
3b'011	16
3b'100	32
3b'101	64
3b'110	Reserved
3b'111	Reserved

Table 119 External Memory Segmentation

Auxiliary Clock Monitor Status Register)

Field	Read / Write	Bits	Length	Reset State	Description
NCLKAV	R	0:0	1	0	This field monitors the availability of the QDR-II synchronous negative input clock, CQB. 0: Clock not available. 1: Clock available.
PCLKAV	R	0:1	1	0	This field monitors the availability of the QDR-II synchronous positive input clock, CQ. 0: Clock not available. 1: Clock available.
Note: Refer to Table 2 "Pin Description" on page 28 for a brief description of the QDR-II clocks.					

Table 120 Auxiliary Clock Monitor Status Register (Block Base=0x0A00, Register Offset=0x03)

External Memory Test Control Register

Field	Read / Write	Bits	Length	Reset State	Description
TEST	R/W	0:0	1	0	This field triggers the external QDR-II SRAM test. 0: Testing is not triggered. 1: Testing is triggered.

Table 121 External Memory Test Control Register (Block Base=0x0A00, Register Offset=0x04)

External Memory Test Results Register

Field	Read / Write	Bits	Length	Reset State	Description
TEST_DONE	R	0:0	1	1	This field indicates the status of the external QDR-II SRAM built-in self test. 0: Test in progress. This bit is set to 0 when the test is triggered by writing 1 to the field TEST in Table 121. 1: Test finished.
ERROR	R	0:1	1	0	This field indicates the result of the external QDR-II SRAM test. 0: No error. 1: Some error with memory BIST.

Table 122 External Memory Test Results Register (Block Base=0x0A00, Register Offset=0x05)

Auxiliary Early Backpressure Threshold Register

Field	Read / Write	Bits	Length	Reset State	Description
EBP_THR	R/W	0:0-1:5	14	0x40	In the PFP to QDR-II path, this field programs the threshold in the QDR-II FIFO at which backpressure will be generated. If free space in the FIFO is less than this threshold, backpressure is initiated towards the PFP egress by setting the FIFO status to satisfied. This threshold is a global setting that is used by all FIFOs in the QDR-II SRAM.

Table 123 Auxiliary Early Backpressure Threshold Register (Block Base=0x0A00, Register Offset=0x07)

Auxiliary Packet Mode Configuration Register

Field	Read / Write	Bits	Length	Reset State	Description
PKT_MODE	R/W	0:0	1	0	This bit controls the mode of transfer from QDR-II to PFP ingress. 0: Cut through mode. In this mode, contiguous transfers from the QDR-II SRAM to the PFP may contain interleaved packets. 1: Packet mode.In this mode, whole packets are transferred from the QDR-II SRAM to PFP.

Table 124 Auxiliary Packet Mode Configuration Register (Block Base=0x0A00, Register Offset=0x08)

HSTL Test Register

Field	Read / Write	Bits	Length	Reset State	Description
HSTL_RX_TEST	R/W	0:0	1	0	Controls an internal test function in the HSTL receiver. 0: Normal operation 1: Reserved for internal IDT test

Table 125 Auxiliary HSTL Receiver Test Control Register (Block Base=0x0A00, Register Offset=0x0E)

Auxiliary Automatic Impedance Matching Control Register

Field	Read / Write	Bits	Length	Reset State	Description
AUTO_MEASURE	R/W	0:0	1	0	Writing 1 to this register will enable an automatic impedance measurement. Set to 0 for normal operation.
Note: This register is used for diagnostic purpose only.					

Table 126 Auxiliary Automatic Impedance Matching Control Register (Block Base=0x0A00, Register Offset=0x0F)

Auxiliary Synchronization Status Register

Field	Read / Write	Bits	Length	Reset State	Description
INIT_DONE	R/W	0:0	1	0	This field indicates the initialization status. 0: Auxiliary interface not initialized. 1: Auxiliary interface initialized.
ALARM	R/W	0:1	1	0	This field indicates the clock is not usable due to instability or excessive jitter. 0:No alarm, indicates that the clock is stable. 1:Alarm due to an unstable clock or excessive jitter.

Table 127 Auxiliary Synchronization Status Register (Block Base=0x0A00, Register Offset=0x12)

Auxiliary Initialization Control Register

Field	Read / Write	Bits	Length	Reset State	Description
INIT_TRIG	R/W	0:0	1	0	Write 1 to initialize synchronization of the auxiliary interface.
AUTO_SYNCH	R/W	0:1	1	1	0:Test mode, 1:Embedded software controls initialization of the synchronization.

Table 128 Auxiliary Initialization Control Register (Block Base=0x0A00, Register Offset=0x013)

PRGD Registers

Enable Control Register

Field	Read/ Write	Bits	Length	Reset state	Description
GEN	R/W	0:0	1	0	This bit enables or disables the PRBS generator. 0: Disable PRBS generator. 1: Enable PRBS generator.
DEN	R/W	0:1	1	0	This bit enables or disables the PRBS detector. 0: Disable PRBS detector.The received PRBS is not detected and the payload is discarded. 1: Enables PRBS detector to detect the received PRBS.

Table 129 Enable Control Register (Block Base=0x0B00, Register Offset=0x00)

Feedback Configuration Register

Field	Read/ Write	Bits	Length	Reset State	Description
FBC	R/W	0:0 - 0:7	8	0	This field defines the feedback function for generating the PRBS sequence.
FBC	R/W	1:0 - 1:7	8	0xC0	This field defines the feedback function for generating the PRBS sequence.
FBC	R/W	2:0 - 2:7	8	0	This field defines the feedback function for generating the PRBS sequence.
FBC	R/W	3:0 - 3:7	8	0	This field defines the feedback function for generating the PRBS sequence.

Table 130 Feedback Configuration Register (Block Base=0x0B00, Register Offset=0x01)

Bandwidth Control Register

Field	Read/ Write	Bits	Length	Reset State	Description
BW	R/W	0:0 - 0:1	2	11	This field defines the bandwidth level for the PRBS generator and checker as shown in Table 126.

Table 131 Bandwidth Control Register (Block Base=0x0B00, Register Offset=0x02)

BW	Bandwidth Level
00	MCLK
01	1/2 MCLK
10	1/4 MCLK
11	1/8 MCLK

Table 132 Bandwidth level as per field BW.

Packet Length Register

Field	Read/ Write	Bits	Length	Reset State	Description
P_LEN	R/W	0:0 - 1:5	14	0xFF	This field determines the packet length to be generated using the PRBS pattern. The actual packet length to be transmitted is P_LEN + 1.

Table 133 Packet Length Register (Block Base=0x0B00, Register Offset=0x03)

Burst Size Register

Field	Read/Write	Bits	Length	Reset State	Description
BURST_S	R/W	0:0 - 0:3	4	0xF	This field determines the burst size of the packets generated by the PSBR packet generator. The packets can be transmitted in a random or a fixed burst as determined by the BURST_RAND field in the Random Control Register (p. 134)

Table 134 Burst Size Register (Block Base=0x0B00, Register Offset=0x04)

Random Control Register

Field	Read/Write	Bits	Length	Reset State	Description
PLEN_RAND	R/W	0:0	1	0	This bit determines if the packet length of the packets generated by the PSBR packet generator is random or fixed. 0: Enable fixed packet length. It is fixed to P_LEN + 1. P_LEN is defined in Packet Length Register (p. 134). 1: Enable random packet length. The packet length can be from 1 to P_LEN + 1.
BURST_RAND	R/W	0:1	1	0	This bit determines if the burst size of the packets to be transmitted is random or fixed. 0: Enable fixed burst size. It is fixed to (BURST_S+1)*16 bytes. BURST_S is defined in Burst Size Register (p. 134). 1: Enable random burst size. The burst size can vary from 16 bytes to (BURST_S+1)*16 bytes.

Table 135 Random Control Register (Block Base=0x0B00, Register Offset=0x05)

LID Register

Field	Read/ Write	Bits	Length	Reset State	Description
LID	R/W	0:0 - 0:5	6	0	This field indicates the LID which is selected to transfer the PRBS packet burst.

Table 136 LID Register (Block Base=0x0B00, Register Offset=0x06)

Synchronization Register

Field	Read/ Write	Bits	Length	Reset State	Description
SYNCV	R/W	0:0	1	0	This field indicates the synchronization status of the PRBS detector. 0: Out of sync. 1: In sync.
SYNCI	R/W	0:1	1	0	This field captures any transaction in the field SYNCV. 0: No change. 1: Change in state from out of sync to in sync or vice-versa. Write 1: Clear
Note: (1)The out of sync status can be due to any one of 3 reasons. a) Resetting the device. b) If field "DEN" in Enable Control Register (p. 133) is 0. c) If excessive errors between regenerated sequence from the received data and received sequence. (2) A transition from out of sync to in sync is caused by 48 consecutive error free bits. (3) In the in sync state, each mismatched bit will generate a bit error event and will be forwarded to PMON.					

Table 137 Synchronization Register (Block Base=0x0B00, Register Offset=0x07)

Bit Error Insertion Register

Field	Read/ Write	Bits	Length	Reset State	Description
ERROR_INS	R/W	0:0	1	0	This field is used to insert a single bit error into the PRBS generator. 0: Bit error is not inserted. 1: 1 bit error is inserted After the error is inserted, it auto clears.

Table 138 Bit Error Insertion Register (Block Base=0x0B00, Register Offset=0x08)

PMON Registers

PMON Event Interrupt Indication Register

Field	Read / Write	Bits	Length	Reset State	Description
T_INACT_I	R/W	0:0	1	0	Tributary ingress inactive LP event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
M_INACT_I	R/W	0:1	1	0	Main ingress inactive LP event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
TM_ISOP_I	R/W	0:2	1	0	T-M illegal SOP event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
TM_IEOP_I	R/W	0:3	1	0	T-M illegal EOP event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
MT_ISOP_I	R/W	0:4	1	0	M-T illegal SOP event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
MT_IEOP_I	R/W	0:5	1	0	M-T illegal EOP event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
TM_PKTCD_I	R/W	0:6	1	0	T-M packet cut down event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
MT_PKTCD_I	R/W	0:7	1	0	M-T packet cut down event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
T_LOCKUN_I	R/W	1:0	1	0	Tributary SPI4 ingress locker unavailable event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
M_LOCKUN_I	R/W	1:1	1	0	Main SPI4 ingress locker unavailable event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
T_DCLKLOS_I	R/W	1:2	1	0	Tributary ingress data clock loss event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.

Table 139 PMON Event Interrupt Indication Register (Block Base=0x0F00, Register Offset=0x00)

Field	Read / Write	Bits	Length	Reset State	Description
T_SCLKLOS_I	R/W	1:3	1	1	Tributary egress status clock loss event. Read 1: Indicates that the event has not occurred. Read 0: Indicates occurrence of the event. Write 1: Clear the bit.
M_DCLKLOS_I	R/W	1:4	1	0	Main ingress data clock loss event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
M_SCLKLOS_I	R/W	1:5	1	0	Main egress status clock loss event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
T_DIP2_I	R/W	1:6	1	0	Tributary SPI4 DIP-2 event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
T_DIP4_I	R/W	1:7	1	0	Tributary SPI4 DIP-4 event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
T_BUSERR_I	R/W	2:0	1	0	Tributary SPI4 bus error event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
T_ISYNC_I	R/W	2:1	1	0	Tributary ingress synch status change event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
T_ESYNC_I	R/W	2:2	1	0	Tributary Egress synch status change event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
M_DIP2_I	R/W	2:3	1	0	Main SPI4 DIP-2 event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
M_DIP4_I	R/W	2:4	1	0	Main SPI4 DIP-4 event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.

Table 139 PMON Event Interrupt Indication Register (Block Base=0x0F00, Register Offset=0x00)

Field	Read / Write	Bits	Length	Reset State	Description
M_BUSERR_I	R/W	2:5	1	0	Main SPI4 bus error event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
M_ISYNC_I	R/W	2:6	1	0	Main ingress synch status change event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.
M_ESYNC_I	R/W	2:7	1	0	Main Egress synch status change event. Read 1: Indicates occurrence of the event. Read 0: Indicates that the event has not occurred. Write 1: Clear the bit.

Table 139 PMON Event Interrupt Indication Register (Block Base=0x0F00, Register Offset=0x00)

PMON Event Interrupt Enable Register

Field	Read / Write	Bits	Length	Reset State	Description
T_INACT_EN	R/W	0:0	1	0	Tributary ingress inactive LP. 0: Disables the interrupt. 1: Enables the interrupt.
M_INACT_EN	R/W	0:1	1	0	Main ingress inactive LP. 0: Disables the interrupt. 1: Enables the interrupt.
TM_ISOP_EN	R/W	0:2	1	0	T-M illegal SOP. 0: Disables the interrupt. 1: Enables the interrupt.
TM_IEOP_EN	R/W	0:3	1	0	T-M illegal EOP. 0: Disables the interrupt. 1: Enables the interrupt.
MT_ISOP_EN	R/W	0:4	1	0	M-T illegal SOP. 0: Disables the interrupt. 1: Enables the interrupt.
MT_IEOP_EN	R/W	0:5	1	0	M-T illegal EOP. 0: Disables the interrupt. 1: Enables the interrupt.
TM_PKTCD_EN	R/W	0:6	1	0	T-M packet cut down. 0: Disables the interrupt. 1: Enables the interrupt.
MT_PKTCD_EN	R/W	0:7	1	0	M-T packet cut down. 0: Disables the interrupt. 1: Enables the interrupt.
T_LOCKUN_EN	R/W	1:0	1	0	Tributary SPI4 ingress locker unavailable. 0: Disables the interrupt. 1: Enables the interrupt.
M_LOCKUN_EN	R/W	1:1	1	0	Main SPI4 ingress locker unavailable. 0: Disables the interrupt. 1: Enables the interrupt.
T_DCLKLOS_EN	R/W	1:2	1	0	Tributary ingress data clock lost. 0: Disables the interrupt. 1: Enables the interrupt.
T_SCLKLOS_EN	R/W	1:3	1	0	Tributary egress status clock lost. 0: Disables the interrupt. 1: Enables the interrupt.
M_DCLKLOS_EN	R/W	1:4	1	0	Main ingress data clock lost. 0: Disables the interrupt. 1: Enables the interrupt.
M_SCLKLOS_EN	R/W	1:5	1	0	Main egress status clock lost. 0: Disables the interrupt. 1: Enables the interrupt.
T_DIP2_EN	R/W	1:6	1	0	Tributary SPI4 DIP-2. 0: Disables the interrupt. 1: Enables the interrupt.

Table 140 PMON Event Interrupt Enable Register (Block Base=0x0F00, Register Offset=0x01)

Field	Read / Write	Bits	Length	Reset State	Description
T_DIP4_EN	R/W	1:7	1	0	Tributary SPI4 DIP-4. 0: Disables the interrupt. 1: Enables the interrupt.
T_BUSERR_EN	R/W	2:0	1	0	Tributary SPI4 bus error. 0: Disables the interrupt. 1: Enables the interrupt.
T_ISYNC_EN	R/W	2:1	1	0	Tributary ingress synch status change. 0: Disables the interrupt. 1: Enables the interrupt.
T_ESYNC_EN	R/W	2:2	1	0	Tributary Egress synch status change. 0: Disables the interrupt. 1: Enables the interrupt.
M_DIP2_EN	R/W	2:3	1	0	Main SPI4 DIP-2. 0: Disables the interrupt. 1: Enables the interrupt.
M_DIP4_EN	R/W	2:4	1	0	Main SPI4 DIP-4. 0: Disables the interrupt. 1: Enables the interrupt.
M_BUSERR_EN	R/W	2:5	1	0	Main SPI4 bus error. 0: Disables the interrupt. 1: Enables the interrupt.
M_ISYNC_EN	R/W	2:6	1	0	Main ingress synch status change. 0: Disables the interrupt. 1: Enables the interrupt.
M_ESYNC_EN	R/W	2:7	1	0	Main Egress synch status change. 0: Disables the interrupt. 1: Enables the interrupt.
Note: Writing a 1 to any field in this register, causes an interrupt to be generated based on the occurrence of that particular event indicated in the corresponding field in Table 139. The interrupt appears as an active low on the INTB pin in the microprocessor interface.					

Table 140 PMON Event Interrupt Enable Register (Block Base=0x0F00, Register Offset=0x01)

PMON Buffer T-M Overflow Indication Register

Field	Read / Write	Bits	Length	Reset State	Description
OVFERFLOW[31:0]	R/W	0:0-3:7	32	0	This register indicates the overflow on a per LID basis from the tributary to main SPI-4 interface. Bit 0 of register with offset 0x02 indicates overflow for LID 0, bit 3 for LID 3, bit 0 of 2nd register with offset 0x03 indicates overflow for LID 32 and so on. Read 1: Indicates overflow for that LID. Read 0: Indicates no overflow for that LID. Write 1: Clears the bit.

Table 141 PMON Buffer T-M Overflow Indication Register (Block Base=0x0F00, Register Offset=0x02-0x03)

There are 2 registers.

PMON Buffer M-T Overflow Indication Register

Field	Read / Write	Bits	Length	Reset State	Description
OVERFLOW[31:0]	R/W	0:0-3:7	32	0	This register indicates the overflow on a per LID basis from the main to tributary SPI-4 interface. Bit 0 of register with offset 0x04 indicates overflow for LID 0, bit 3 for LID 3, bit 0 of 2nd register with offset 0x05 indicates overflow for LID 32 and so on. Read 1: Indicates overflow for that LID. Read 0: Indicates no overflow for that LID. Write 1: Clears the bit.

Table 142 PMON Buffer M-T Overflow Indication Register (Block Base=0x0F00, Register Offset=0x04-0x05)

There are 2 registers.

PMON Buffer T-M Overflow Interrupt Control Register

Field	Read / Write	Bits	Length	Reset State	Description
OVF_EN[31:0]	R/W	0:0-3:7	32	0	This register enables or disables the overflow indication for the LIDs which is indicated in registers in Table 141.Bit 0 of register with offset 0x06 is for LID 0 and bit 0 of register with offset 0x07 is for LID 32 and so on. 0: Disables overflow indication in PMON buffer T-M overflow indication register. 1: Enables overflow indication in PMON buffer T-M overflow indication register.

Table 143 PMON Buffer T-M Overflow Interrupt Control Register (Block Base=0x0F00, Register Offset=0x06-0x07)

There are 2 registers.

PMON Buffer M-T Overflow Interrupt Control Register

Field	Read / Write	Bits	Length	Reset State	Description
OVF_EN	R/W	0:0-3:7	32	0	This register enables or disables the overflow indication for the LIDs which is indicated in registers in Table 142.Bit 0 of register with offset 0x08 is for LID 0 and bit 0 of register with offset 0x09 is for LID 32 and so on. 0: Disables overflow indication in PMON buffer M-T overflow indication register. 1: Enables overflow indication in PMON buffer M-T overflow indication register.

Table 144 PMON Buffer M-T Overflow Interrupt Control Register (Block Base=0x0F00, Register Offset=0x08-0x09)

There are 2 registers.

PMON Buffer Overflow Source Register

Field	Read / Write	Bits	Length	Reset State	Description
TM_OVF	R	0:0	1	0	This is a field associated critical event. When there is an overflow in the 64 T-M LIDs, this event is generated. It is the OR result of 64 LIDs.
MT_OVF	R	0:1	1	0	This is a field associated critical event. When there is an overflow in the 64 T-M LIDs, this event is generated. It is the OR result of 64 LIDs.

Table 145 PMON Buffer Overflow Source Register (Block Base=0x0F00, Register Offset=0x0A)

PMON T-M Inactive Transfer LP Field Register

Field	Read / Write	Bits	Length	Reset State	Description
LP	R	0:0-0:7	8	0	In the T-M direction, when a control word carries an inactive LP information, then this event is generated and this register indicates the LP connected to the event.

Table 146 PMON T-M Inactive Transfer LP Field Register (Block Base=0x0F00, Register Offset=0x0B)

PMON M-T Inactive Transfer LP Field Register

Field	Read / Write	Bits	Length	Reset State	Description
LP	R	0:0-0:7	8	0	In the M-T direction, when a control word carries an inactive LP information, then this event is generated and this register indicates the LP connected to the event.

Table 147 PMON M-T Inactive Transfer LP Field Register (Block Base=0x0F00, Register Offset=0x0C)

PMON T-M Illegal SOP Event LID Field Register

Field	Read / Write	Bits	Length	Reset State	Description
LID	R	0:0-0:5	6	0	This event is generated when consecutive SOPs are received at the tributary SPI4 interface. The LID connected with the event is indicated in the register.

Table 148 PMON T-M Illegal SOP Event Field Register (Block Base=0x0F00, Register Offset=0x0D)

PMON T-M Illegal EOP Event LID Field Register

Field	Read / Write	Bits	Length	Reset State	Description
LID	R	0:0-0:5	6	0	This event is generated when consecutive EOPs are received at the tributary SPI4 interface. The LID connected with the event is indicated in the register

Table 149 PMON T-M Illegal EOP Event Field Register (Block Base=0x0F00, Register Offset=0x0E)

PMON M-T Illegal SOP Event LID Field Register

Field	Read / Write	Bits	Length	Reset State	Description
LID	R	0:0-0:5	6	0	This event is generated when consecutive SOPs are received at the main SPI4 interface. The LID connected with the event is indicated in the register.

Table 150 PMON M-T Illegal SOP Event Field Register (Block Base=0x0F00, Register Offset=0x0F)

PMON M-T Illegal EOP Event LID Field Register

Field	Read / Write	Bits	Length	Reset State	Description
LID	R	0:0-0:5	6	0	This event is generated when consecutive EOPs are received at the main SPI4 interface. The LID connected with the event is indicated in the register

Table 151 PMON M-T Illegal EOP Event Field Register (Block Base=0x0F00, Register Offset=0x10)

PMON T-M Packet Cut-Down LID Field Register

Field	Read / Write	Bits	Length	Reset State	Description
LID	R	0:0-0:5	6	0	When the packet arriving at the tributary SPI-4 interface is larger than the storage capability of the LID, this event is raised and the LID associated with the event is indicated.

Table 152 PMON T-M Packet Cut-Down LID Field Register (Block Base=0x0F00, Register Offset=0x11)

PMON M-T Packet Cut-Down LID Field Register

Field	Read / Write	Bits	Length	Reset State	Description
LID	R	0:0-0:5	6	0	When the packet arriving at the main is larger than the storage capability of the LID, this event is raised and the LID associated with the event is indicated.

Table 153 PMON M-T Packet Cut-Down LID Field Register (Block Base=0x0F00, Register Offset=0x12)

PMON Per LID Counter Table

Length	Register Offset	Measure Point	Reset State	Description
24	0x 6n	3,4	0	Tributary ingress good packet counter
24	0x 6n+1	3,4	0	Tributary ingress abort packet counter
24	0x6n+2	13,14	0	Main ingress good packet counter
24	0x6n+3	13,14	0	Main ingress abort packet counter
24	0x6n+4	18,19	0	Tributary egress packets counter
24	0x6n+5	8,9	0	Main egress packets counter
Note: (1) In the register offset column 'n' refers to the LID number, with n between 0 and 63. The register address of the counter for a particular LID is derived from the offset address using the equation shown in the register offset column and adding it to the block_base. (2) For the measure point, refer to Figure 33 PMON Measure Points p.67				

Table 154 PMON Per LID Counter Table (Block Base=0x0C00, Register Offset=0x00-0x17F)

Note: The counter tables are subject to accumulation of data from a point in time to another.

PMON Per Module/Interface Counter Table

Subject to accumulation	Length	Register Offset	Measure Point	Reset State	Description
	29	0x00	3,4	0	Tributary SPI-4 ingress byte
	26	0x01	1,2	0	Tributary SPI-4 ingress transfer
SPI4+insert+loop	8	0x02	6,7	0	T-M too long packet
	8	0x03	6,7	0	T-M too short packet
	16	0x04	21,22	0	Tributary SPI-4 DIP-2 error
	16	0x05	1,2	0	Tributary SPI-4 DIP-4 error
Individual for A/B	29	0x06	13,14	0	Main SPI-4 ingress byte
Module A	26	0x07	12	0	Main SPI-4 ingress transfer
	8	0x08	16,17	0	M-T too long packet
	8	0x09	16,17	0	M-T too short packet
Module A	16	0x0A	11	0	Main SPI-4 DIP-2 error
Module A	16	0x0B	12	0	Main SPI-4 DIP-4 error
Module B	30	0x0C	10	0	PRBS bit error
Module B	24	0x0D	5	0	Auxiliary ingress transfer counter
Module B	24	0x0E	20	0	Auxiliary egress transfer counter
Module B	24	0x0F	15	0	PRBS ingress transfer counter
Module B	24	0x10	10	0	PRBS egress transfer counter

Table 155 PMON Per Module/Interface Counter Table (Block Base=0x0E00 Register Offset=0x00-0x10

Note: The counter tables are subject to accumulation of data from a point in time to another based on the Timebase.

For the measure points please refer to Figure 33 PMON Measure Points p.67

Miscellaneous Registers

PMON Timebase Control Register

Field	Read / Write	Bits	Length	Reset State	Description
INTERNAL	R/W	0:0	1	0	Selects between the internal and external time base.Please refer to table 144.
TIMER	R/W	0:1	1	0	Selects the internal timer/OBC as the timebase timing source. Please refer to table 144.
MANUAL	R/WC	0:2	1	0	Manual time base trigger, self clear.

Table 156 PMON Timebase Control Register (Block Base=0x8B00, Register Offset=0x00)

Manual Bit 2	Timer Bit 1	Internal Bit 0	Timebase trigger Source
X	X	0	External.
X	1	1	Internal timer.
X	0	1	External OBC.

Table 157 Timebase source table.

PMON 1ms Timer Register

Field	Read / Write	Bits	Length	Reset State	Description
PERIOD	R/W	0:0-2:1	18	0x1E600	The timer register specifies the number of MCLK for generation of a 1ms time interval.

Table 158 PMON 1ms Timer Register (Block Base=0x8B00, Register Offset=0x01)

GPIO Direction Register

Field	Read / Write	Bits	Length	Reset State	Description
DIR_OUT	R/W	0:0	1	0	This field controls the direction of General Purpose IO pins. The direction can be input or output. 0: The GPIO pins act as input/read pins. 1: The GPIO pins act as output/write pins.

Table 159 GPIO Direction Register (Block Base=0x8B00, Register Offset=0x10-0x12)

There are 3 registers.Register offset 0x10 is for GPIO 0. Register offset 0x11 is for GPIO 1and register offset 0x12 is for GPIO 2.

GPIO Level Register

Field	Read / Write	Bits	Length	Reset State	Description
LEVEL	R/W	0:0	1	1	This field controls the logical level on the GPIO pins.It indicates a logical high or a logical low. 0: Logical low. 1: Logical high.

Table 160 GPIO Level Register (Block Base=0x8B00, Register Offset=0x13-0x15)

There are 3 registers.

GPIO Link Table

Field	Read / Write	Bits	Length	Reset State	Description
ADDRESS	R/W	0:0- 1:7	16	0	This field defines the address of the bit to be selected.
BIT	R/W	2:0- 2:4	5	0	This field defines which bit is to be selected at the address defined in the field ADDRESS.
REFLECT_EN	R/W	2:5	1	0	If this field is enabled, then the LEVEL field in Table 160 reflects the status of the bit which is selected from the indirect address space. 0: Disable. 1: Enable.

Table 161 GPIO Link Table (Block Base=0x8B00, Register Offset=0x16-0x18)

There are 3 registers.

Version Number Register

Field	Read / Write	Bits	Length	Reset State	Description
VER	R	0:0-0:7	8	0x01	This field indicates the version of the chip.
ID	R	1:0-1:7	8	0xff	This field indicates the chip ID.

Table 162 Version Number Register (Block Base=0x8B00, Register Offset=0x30)

Software Version Register

Field	Read / Write	Bits	Length	Reset State	Description
SW_VER	R	0:0-0:7	8	0x01	This field indicates the software version of the chip.

Table 163 Version Number Register (Block Base=0x8B00, Register Offset=0x32)

Electrical and Thermal Specification

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min[1]	Max	Unit
Core Digital Supply Voltage	V_{DDC12}	V_{SS}=0, T_j=25°C	-0.3	1.5	V
I/O Digital Supply Voltage for LVDS	V_{DDL12}		-0.3	1.5	V
I/O Digital Supply Voltage for HSTL	V_{DDH15}		-0.3	2.1	V
I/O Digital Supply Voltage for LVDS	V_{DDL25}		-0.3	3	V
I/O Digital Supply Voltage for HSTL	V_{DDH25}		-0.3	3	V
I/O Digital Supply Voltage for LVTTL	V_{DDT33}		-0.3	4.5	V
Analog Supply Voltage	V_{DDA25}		-0.3	4.5	V
I/O Input Voltage for LVTTL	Vin		-0.5	V_{DDT33}+0.5	V
I/O Input Voltage for LVDS	VinL		-0.5	V_{DDL25}+0.5	V
I/O Input Voltage for HSTL	VinL		-0.5	V_{DDH15}+0.5/ V_{DDH25}+0.5	V
Latch-up Current	Io		-	100	mA
ESD Performance (HBM)			-	2000	V
Lead Temperature, BR package	T_L		-	+250	°C
Lead Temperature, BL package	T_L			+245	°C
Ambient Operating Temperature	T_a (Industrial)		-40	+85	°C
Ambient Operating Temperature	T_a (Commercial)		0	+70	°C
Storage Temperature	T_s		-65	+150	°C

Table 164 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table Absolute Maximum Ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Core Digital Supply Voltage	V_{DDC12}	V_{SS}=0	1.08	1.2	1.32	V
I/O Digital Supply Voltage for LVDS	V_{DDL12}	V_{SS}=0	1.14	1.2	1.26	V
I/O Digital Supply Voltage for HSTL	V_{DDH15}	V_{SS}=0	1.4	1.5	1.6	V
I/O Digital Supply Voltage for LVDS	V_{DDL25}	V_{SS}=0	2.375	2.5	2625	V
I/O Digital Supply Voltage for HSTL	V_{DDH25}	V_{SS}=0	2.375	2.5	2.625	V
I/O Digital Supply Voltage for LVTTL	V_{DDT33}	V_{SS}=0	3.0	3.3	3.6	V
Analog Supply Voltage	V_{DDA25}	AV_{SS}=0	2.25	2.5	2.75	V

Table 165 Recommended Operating Conditions (Part 1 of 2)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference for Termination	V_{TT}	V_{SS}=0	0.7	V_{DDH15}/2	0.8	V
I/O Reference for LDVS	$V_{SPI4A/B/C\_VREF}$	V_{SS}=0	1.14	1.2	1.26	V
I/O Reference for HSTL	V_{QDR_IMP}/V_{G_IMP}	V_{SS}=0	0.68	V_{DDH15}/2	0.8	V

Table 165 Recommended Operating Conditions (Part 2 of 2)

Thermal Characteristics

Parameter	Symbol	Conditions	Value[1]
Maximum Power Dissipation total	P_T	Ta=25°C, F_{MCLK}=200 MHz	4.4W
Maximum Power Dissipation of core	P_{VDDC12}	Ta=25°C, F_{MCLK}=200 MHz	2W
Maximum Power Dissipation of each LVDS SPI-4 Interface I/O	P_{VDDL25}	Ta=25°C, F_{MCLK}=200 MHz	0.5W
Maximum Power Dissipation of HSTL I/O (Memory Interface)	$P_{VDDH15/VDDH25}$	Ta=25°C, F_{MCLK}=200 MHz	0.4W
Power Dissipation of LVTTL I/O	P_{VDDT33}	Ta=25°C, F_{MCLK}=200 MHz	0.33W
Maximum Power Dissipation of Analog circuits	P_{VDDA25}	Ta=25°C, F_{MCLK}=200 MHz	0.5W
Thermal Resistance (Junction to case)[2]	Θ_{JC}		0.3°C/W
Thermal Resistance (Ambient)[3]	Θ_{JA}	Air flow 0.0 m/s	12.6°C/W
		Air flow 1.0 m/s	8.7°C/W
		Air flow 2.0 m/s	7.2°C/W
		Air flow 3.0 m/s	6.5°C/W
		Air flow 4.0 m/s	6°C/W
		Air flow 5.0 m/s	5.8°C/W
Thermal Resistance (Junction to Board)[3]	Θ_{JB}		2.85°C/W

Table 166 Thermal Characteristics

1. Typical Power Dissipation for 3 SPI4 (LVDS) interfaces is 1.5W.

Typical Power Dissipation for 2 SPI4 (LVDS) interfaces is 1.1W.

Typical Power Dissipation for 1SPI4 (LVDS) interface is 0.7W.

Typical Power Dissipation for 1 Memory (HSTL) interface is 0.4W.

Typical Power Dissipation for 0 Memory (HSTL) interface is 0.08W.

2. Test Conditions follows standard test methods and procedures for measuring thermal impedance, per EIA/JEDEC51. Test board: 4 layers (2s/2p) - 101.6mmx114.6mmx1.6mm.

DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CMOS I/O						
Low-Level Input Voltage	V_{IL}		-	-	0.8	V
High-Level Input Voltage	V_{IH}		2.0	-	-	V
Low-Level Output Voltage	V_{OL}	Current=2mA	-	-	0.4	V
High-Level Output Voltage	V_{OH}	Current=2mA	2.4	-	-	V
Schmitt Trigger Input - Low-Level Voltage	V_{TL}		-	-	1.19	V
Schmitt Trigger Input - High-Level Voltage	V_{TH}		1.5	-	-	V
I/O Off State Leakage Current	I_{OZ}		-10	0	+10	µA
Pull-Up Resistor in Input/Bidirectional I/O	RPU		60	90	130	KΩ
Pull-Down Resistor in Input/Bidirectional I/O	RPD		50	85	160	KΩ
LVTTL I/O						
Low-Level Input Voltage	V_{IL}		-	-	0.8	V
High-Level Input Voltage	V_{IH}		2.0	-	-	V
Low-Level Output Voltage	V_{OL}	Current=2mA	-	-	0.4	V
High-Level Output Voltage	V_{OH}	Current=2mA	2.4	-	-	V
Schmitt Trigger Input - Low-Level Voltage	V_{TL}		-	-	1.19	V
Schmitt Trigger Input - High-Level Voltage	V_{TH}		1.5	-	-	V
I/O Off State Leakage Current	I_{OZ}		-10	0	+10	µA
Pull-Up Resistor in Input/Bidirectional I/O	RPU		60	90	130	KΩ
Pull-Down Resistor in Input/Bidirectional I/O	RPD		50	85	160	KΩ
LVDS I/O						
Input Differential Voltage	V_{IDTH}		-100	-	100	mV
Input Differential Impedance	R_{IN}		80	100	120	Ω
Low-Level Output Voltage	V_{OL}	R_{TERM}=100	0.925	-	-	V
High-Level Output Voltage	V_{OH}	R_{TERM}=100	-	-	1.475	V
Output Offset Voltage	V_{OS}		1125	-	1275	mV
Output Differential Voltage	$\|V_{OD}\|$	R_{TERM}=100	250	325	400	mV
Output Differential Impedance	R_O		80	100	120	Ω
Output Short Circuit Current	I_{OS}	Output shorted to GND	-	-	24	mA

Table 167 DC Characteristics (Part 1 of 2)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Output Short Circuit Current	I_{OSD}	+/- Outputs shorted together	-	-	12	mA
HSTL I/O						
Low-Level Input Voltage	V_{IL}		-0.3	-	V_{QDR_VREF}-0.1	V
High-Level Input Voltage	V_{IH}		V_{QDR_VREF}+0.1	-	V_{DDH25}+ 0.3	V
Low-Level Output Voltage	V_{OL}	Driver calibrated to 50Ω	-	-	0.4	V
High-Level Output Voltage	V_{OH}	Driver calibrated to 50Ω	V_{DDH25}- 0.4	-	-	V

Table 167 DC Characteristics (Part 2 of 2)

AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max[1]	Unit
Clock Interface.						
Reference clock (SPI4M_RCLK, SPI4B_RCLK, SPI4A_RCLK) frequency		DIV4=0	19.44		28.125	MHz
Reference clock Duty cycle		DIV4=0	30	50	70	%
Reference clock PPM		DIV4=0			30	PPM
Reference clock frequency		DIV4=1	77.76		112.5	MHz
Reference clock duty cycle		DIV4=1	30	50	70	%
Reference clock PPM		DIV4=1			30	PPM
MCLK internal clock frequency			124		200	MHz
SPI-4 Interface LVDS Input.						
DCLK clock frequency			77.76		450	MHz
SCLK clock frequency			77.76		450	MHz
DCLK clock duty cycle			45	50	55	%
SCLK clock duty cycle			45	50	55	%
Fall time (20%, 80%)		TIA/EIA-644	300		500	ps
Rise time (20%, 80%)		TIA/EIA-644	300		500	ps
Differential Skew (P to N)	T_{SKEW1}				50	ps
Clock jitter tolerance					0.44	UI
Data skew tolerance					2	UI
Input data jitter tolerance					0.13	UI
SPI-4 Interface LVDS Output. Figure TBD.						
DCLK clock frequency			77.76		450	MHz
SCLK clock frequency			77.76		450	MHz

Table 168 AC Characteristics (Part 1 of 4)

Parameter	Symbol	Conditions	Min	Typ	Max[1]	Unit
DCLK clock duty cycle			45	50	55	%
SCLK clock duty cycle			45	50	55	%
Fall time (20%, 80%)	I_{FALL}	TIA/EIA-644	300		500	ps
Rise time (20%, 80%)	I_{RISE}	TIA/EIA-644	300		500	ps
Differential Skew (P to N)	T_{SKEW1}				50	ps
DCLK and SCLK peak to peak Jitter					0.1	UI
DAT and CTL peak to peak Jitter					0.24	UI
Clock-to-Output Propagation delay. This value is programmable. [2]					0.6	UI
SPI-4 Interface LVTTL.						
SCLK clock frequency			19.44		112.5	MHz
SCLK clock duty cycle			40	50	60	%
Input Setup time			2			ns
Input hold time			0.5			ns
Clock-to-Output Propagation delay:				1	1.2	ns
Auxiliary Interface - QDR-II / Generic. Figure 46 Auxiliary Interface - QDR-II / Generic - Write Access p.154 and Figure 47.						
Auxiliary interface clock frequency	faux		133		200	MHz
Auxiliary interface clock period ($1/f_{aux}$)	T		7.51		5	ns
Auxiliary interface clock duty cycle			40		60	%
Clock to write valid	tKWV		0.2T		0.3T	"T" is in ns
Clock to address valid	tKAV		0.2T		0.3T	"T" is in ns
Clock to data valid	tKDV		0.2T		0.3T	"T" is in ns
Clock to read valid	tKRV		0.2T		0.3T	"T" is in ns
Echo clock to data setup	tQVD		-0.4			ns
Echo clock to data hold	tQHD		-0.4			ns
MCU Interface - Motorola mode - non multiplexed bus (MPM=0). Read Cycle. Figure 48 MCU Interface - Motorola Mode - Read Access p.155.						
Read cycle time	tRC		tDW+ tRecovery			ns
Valid DSB+CSB width	tDW		tPRD			ns
Delay from DSB to valid read signal	tRWV				2Tmax-2	ns
R/WB to DSB hold time	tRWH		4T			ns
Delay from DSB to Valid Address	tAV				2Tmax-2	ns
Address to DSB hold time	tADH		tRWH			ns
DSB to valid read data propagation delay	tPRD				6T	ns
Delay from read data active to high Z	tDAZ				10	ns
Recovery time from read cycle	tRecovery		5			ns

Table 168 AC Characteristics (Part 2 of 4)

Parameter	Symbol	Conditions	Min	Typ	Max[1]	Unit
MCU Interface - Motorola mode - non multiplexed bus (MPM=0). Write Cycle. Figure 49 MCU Interface - Motorola Mode - Write Access p.155.						
Internal master clock (MCLK) frequency (defined by the main clock generator)	F		124		200	MHz
Write cycle time	tWC		tDW+tRe-covery			ns
Valid DSB width	tDW		6T			ns
Delay from DSB to valid write signal	tRWV				2Tmax-2	ns
R/WB to DSB hold time	tRWH		6T			ns
Delay from DSB to Valid Address	tAV				2Tmax-2	ns
Address to DSB hold time	tAH		4T			ns
Delay from DSB to valid write data	tDV				tAV	ns
Write data to DSB hold time	tDHW		tAH			ns
Recovery time from write cycle	tRecovery		5			ns
MCU Interface - Intel mode - non multiplexed bus (MPM=1). Read Cycle. Figure 50 MCU Interface - Intel Mode - Read Access p.156.						
Internal master clock (MCLK) frequency (defined by main clock generator)	F		124		200	MHz
Read cycle time	tRC		tRDW+ tRecovery			ns
Valid RDB width	tRDW		tPRD			ns
Delay from RDB to Valid Address	tAV				2Tmax-2	ns
Address to RDB hold time	tAH		4T			ns
RDB to valid read data propagation delay	tPRD				6Tmax	ns
Delay from read data active to High Z	tDAZ				10	ns
Recovery time from read cycle	tRecovery		5			ns
MCU Interface - Intel mode - non multiplexed bus (MPM=1). Write Cycle. Figure 51 MCU Interface - Intel Mode - Write Access p.156.						
Internal master clock (MCLK) period (defined by clock_generator)	T		124		200	MHz
Write cycle time	tWC		tWRW+tR ecovery			ns
Valid WRB width	tWRW		6T			ns
Delay from WRB to Valid Address	tAV				2Tmax-2	ns
Address to WRB hold time	tAH		4T			ns
Delay from WRB to valid write data	tDV				tAV	ns
Write data to WRB hold time	tDHW		tAH			ns
Recovery time from write cycle	tRecovery		5			ns
Serial Peripheral Interface. Figure 53 Serial Peripheral Interface p.158.						

Table 168 AC Characteristics (Part 3 of 4)

Parameter	Symbol	Conditions	Min	Typ	Max[1]	Unit
SCLK Frequency	fOP				2.0	MHz
Min. /CS High Time	tCSH		100			ns
/CS Setup Time	tCSS		50			ns
/CS Hold Time	tCSD		100			ns
Clock Disable Time	tCLD		50			ns
Clock High Time	tCLH		205			ns
Clock Low Time	tCLL		205			ns
Data Setup Time	tDIS		50			ns
Data Hold Time	tDIH		150			ns
Output Delay	tPD				150	ns
Output Disable Time	tDF				50	ns
JTAG Interface. Figure 54 JTAG Interface p.158.						
TCK frequency					10	MHz
TCK duty cycle			40		60	%
TMS setup	tStms		20			ns
TMS hold	tHtms		20			ns
TDI setup	tSdti		20			ns
TDI hold	tHdti		20			ns
TCK low to TDO valid	tPtdo		2		50	ns

Table 168 AC Characteristics (Part 4 of 4)

1. Tmax = 1000/Fmin.

2. This value is programmable by

TCi[0:1] field in the SPI-4 Egress Data Lane Timing Register (p. 118)

CTLTC[0:1] field in the SPI-4 Egress Data Control Lane Timing Register (p. 118)

DCTC[0:1] field in the SPI-4 Egress Data Clock Timing Register (p. 119)

STCi[0:1] field in the SPI-4 Egress Status Timing Register (p. 119)

SCTC[0:3] field in the SPI-4 Egress Status Clock Timing Register (p. 120),

Timing Diagram

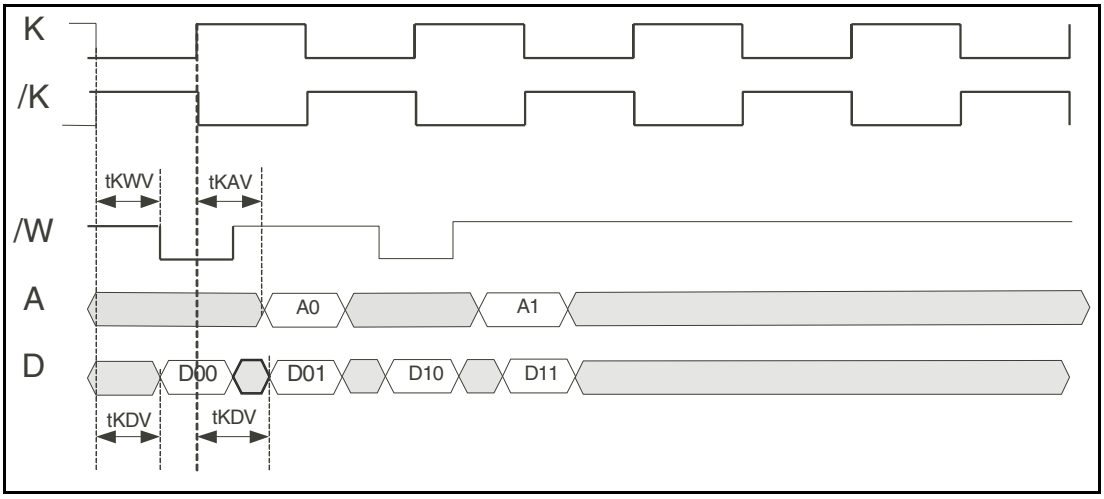


Figure 46 Auxiliary Interface - QDR-II / Generic - Write Access

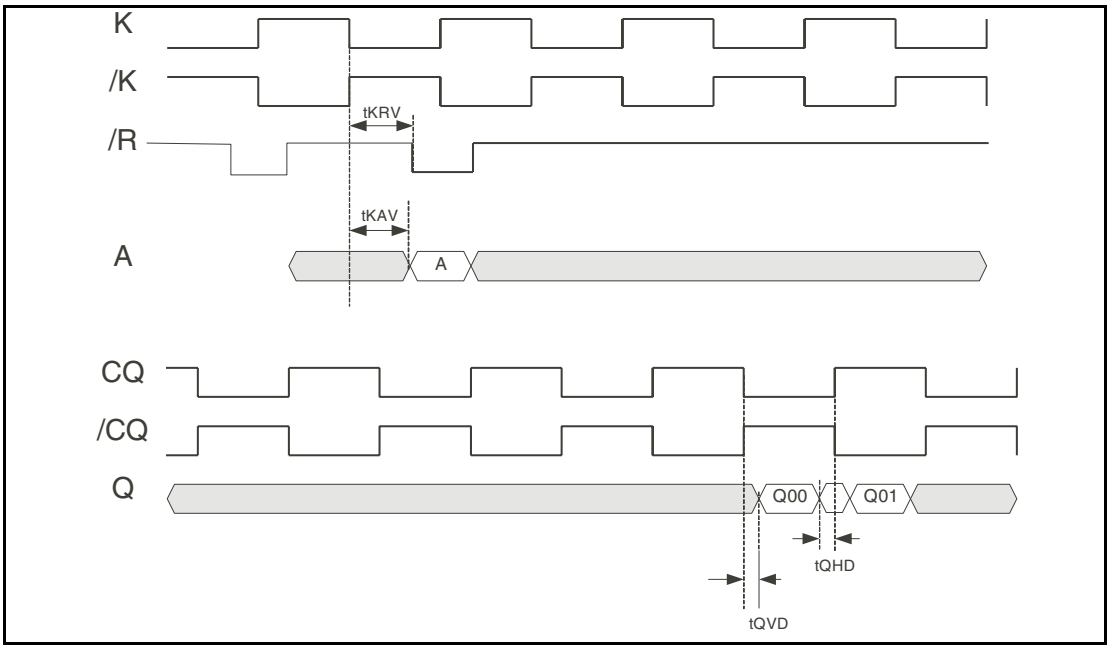


Figure 47 Auxiliary Interface - QDR-II / Generic - Read Access

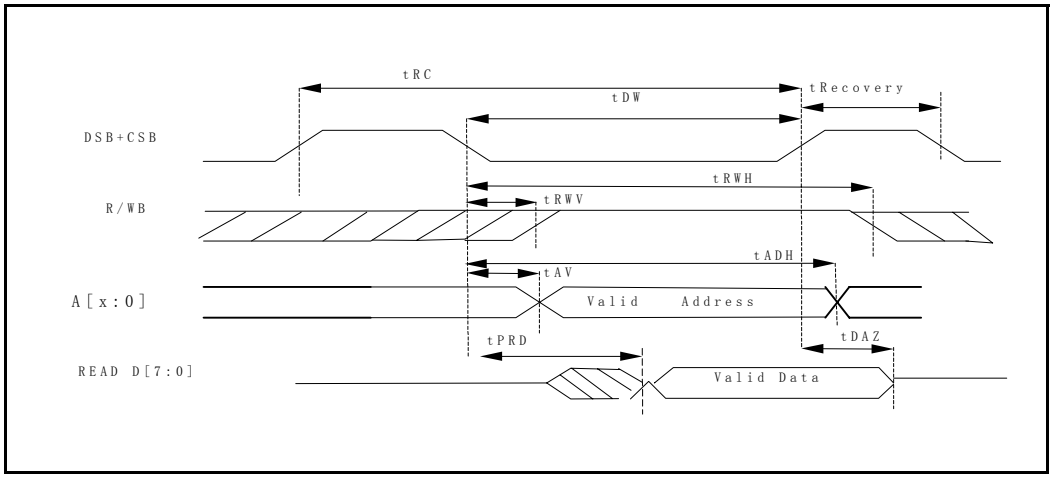


Figure 48 MCU Interface - Motorola Mode - Read Access

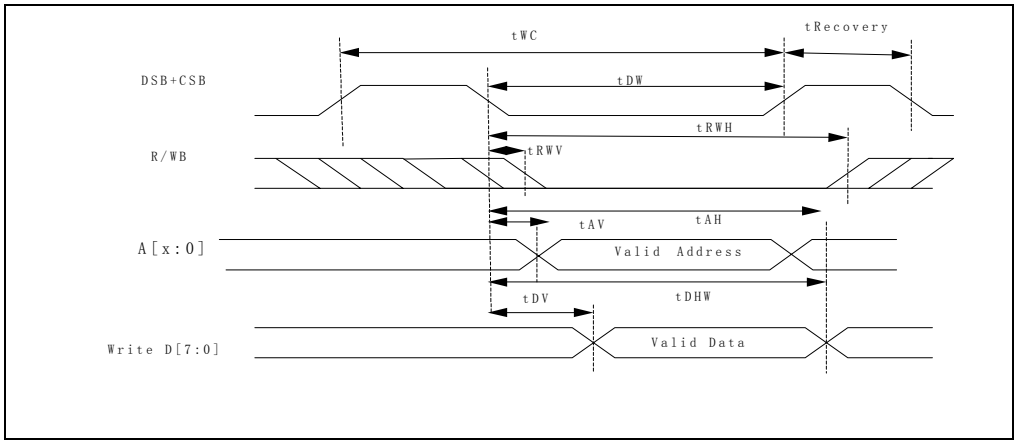


Figure 49 MCU Interface - Motorola Mode - Write Access

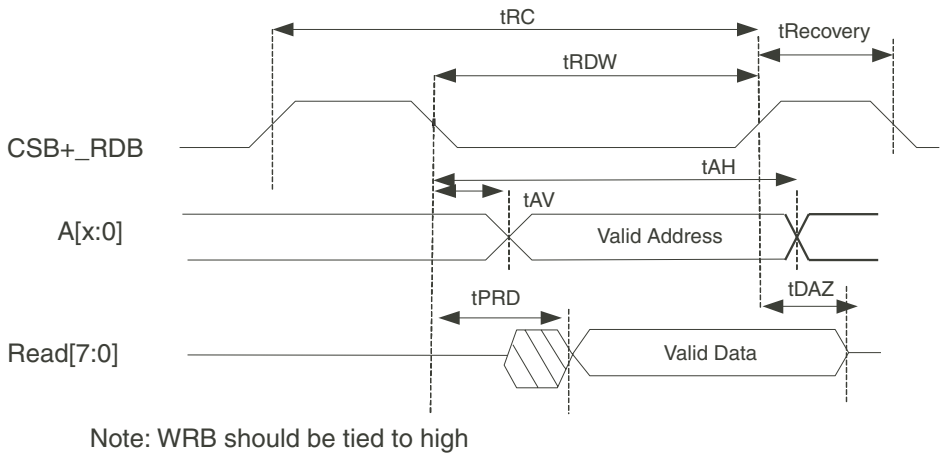


Figure 50 MCU Interface - Intel Mode - Read Access

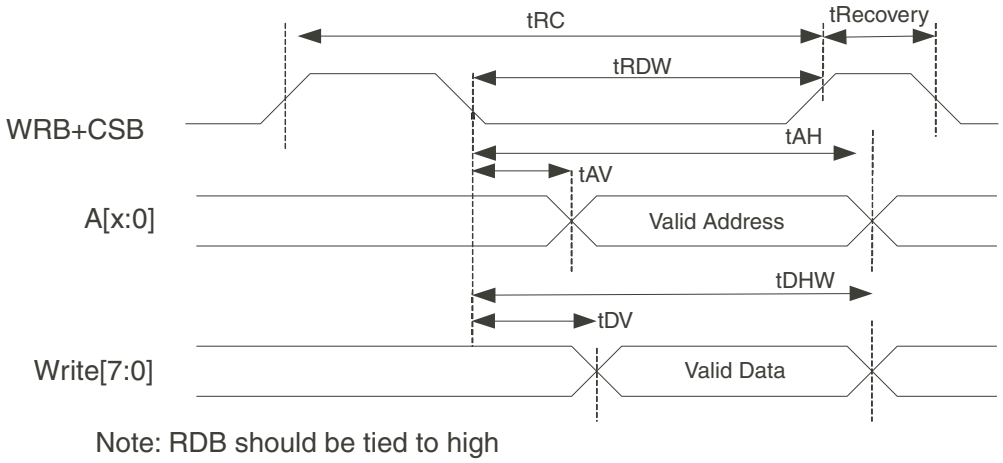


Figure 51 MCU Interface - Intel Mode - Write Access

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A		VDDT33	DAT2	DAT1	DAT0	A_ESCLK_L_P	A_ESCLK_L_N	A_ID_P[3]	A_ID_N[3]	A_ID_P[8]	A_ID_N[8]	ID[13]_P_A	ID[13]_N_A	A_IDCLK_P	A_IDCLK_N	A_ED_P[5]	A_ED_N[5]	A_ED_P[10]	A_ED_N[10]	EDCLK_P_A	EDCLK_N_A	A_ISCLK_L_P	A_ISCLK_L_N	A_BIAS	VDDT33		A
B	VSS	VSS	DAT3	ADR5	WRB	A_ESTA_L_P[1]	A_ESTA_L_N[1]	A_ID_P[2]	A_ID_N[2]	A_ID_P[7]	A_ID_N[7]	ID[12]_P_A	ID[12]_N_A	A_ID_P[15]	A_ID_N[15]	A_ED_P[4]	A_ED_N[4]	A_ED_P[9]	A_ED_N[9]	ED[15]_P_A	ED[15]_N_A	A_ISTA_L_P[1]	A_ISTA_L_N[1]	A_REF	VSS	VDDH15	B
C	DAT6	DAT5	DAT4	ADR3	RDB	A_ESTA_L_P[0]	A_ESTA_L_N[0]	A_ID_P[1]	A_ID_N[1]	A_ID_P[6]	A_ID_N[6]	ID[11]_P_A	ID[11]_N_A	A_ID_P[14]	A_ID_N[14]	A_ED_P[3]	A_ED_N[3]	A_ED_P[8]	A_ED_N[8]	ED[14]_P_A	ED[14]_N_A	A_ISTA_L_P[0]	A_ISTA_L_N[0]	A_ISCLK_T	QDR_Q0	QDR_Q8	C
D	DAT7	ADR2	ADR4	INTB	CSB	A_ESCLK_T	A_ESTA_T[1]	A_ID_P[0]	A_ID_N[0]	A_ID_P[5]	A_ID_N[5]	ID[10]_P_A	ID[10]_N_A	A_ECTL_P	A_ECTL_N	A_ED_P[2]	A_ED_N[2]	A_ED_P[7]	A_ED_N[7]	ED[12]_P_A	ED[12]_N_A	A_ED_N[13]	A_ISTA_T[0]	A_ISTA_T[1]	QDR_D0	QDR_D8	D
E	ADR0	ADR1	SPIEN	MPM	VSS	VSS	A_ESTA_T[0]	A_ICTL_P	A_ICTL_N	A_ID_P[4]	A_ID_N[4]	ID[9]_P_A	ID[9]_N_A	A_ED_P[0]	A_ED_N[0]	A_ED_P[1]	A_ED_N[1]	A_ED_P[6]	A_ED_N[6]	ED[11]_P_A	ED[11]_N_A	A_ED_P[13]	A_TRCLK	QDR_Q4	QDR_Q6	QDR_Q17	E
F	M_ESCLK_L_P	M_ESTA_L_P[1]	M_ESTA_L_P[0]	M_ESCLK_T	VSS	VSS	VSS	VDDL25	VDDL25	VDDA25	VSS	VDDL12	VDDL12	VDDL25	VSS	VSS	VDDA25	VDDL25	VSS	VSS	A_CLK_SEL	QDR_Q2	QDR_D2	QDR_D4	QDR_D6	QDR_D17	F
G	M_ESCLK_L_N	M_ESTA_L_N_M[1]	M_ESTA_L_N[0]	M_ESTA_T[1]	M_ESTA_T[0]	VSS	VSS	VDDL25	VDDL25	VDDA25	VSS	VDDL12	VDDL12	VDDL25	VSS	VSS	VDDA25	VDDL25	VDDH25	VTT075	A_LVDSTA	QDR_Q1	QDR_Q3	QDR_Q5	QDR_Q7	QDR_Q16	G
H	M_ID_P[3]	M_ID_P[2]	M_ID_P[1]	M_ID_P[0]	M_ICTL_P	VSS	VDDL25	VDDL25	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VTT075	TMS	QDR_D1	QDR_D3	QDR_D5	QDR_D7	QDR_D16	H
J	M_ID_N[3]	M_ID_N[2]	M_ID_N[1]	M_ID_N[0]	M_ICTL_N	VSS	VSS	VSS	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VTT075	TESTSE	QDR_Q9	QDR_Q10	QDR_Q11	QDR_Q12	QDR_Q15	J
K	M_ID_P[8]	M_ID_P[7]	M_ID_P[6]	M_ID_P[5]	M_ID_P[4]	VSS	VSS	VSS	VDDC12	VDDC12	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDC12	VDDC12	VSS	QDR_R	QDR_D9	QDR_D10	QDR_D11	QDR_D12	QDR_D15	K
L	M_ID_N[8]	M_ID_N[7]	M_ID_N[6]	M_ID_N[5]	M_ID_N[4]	VSS	VDDA25	VDDA25	VDDC12	VDDC12	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDC12	VDDC12	VSS	QDR_W	QDR_Q13	QDR_Q14	QDR_A0	QDR_NK	QDR_PK	L
M	M_ID_P[13]	M_ID_P[12]	M_ID_P[11]	M_ID_P[10]	M_ID_P[9]	TCK	VDDL12	VDDL12	VDDC12	VDDC12	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDC12	VDDC12	VDDH15	QDR_A17	QDR_D13	QDR_D14	QDR_A1	VSS	VDDH15	M
N	M_ID_N[13]	M_ID_N[12]	M_ID_N[11]	M_ID_N[10]	M_ID_N[9]	TDO	VDDL12	VDDL12	VDDC12	VDDC12	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDC12	VDDC12	VDDH15	QDR_A16	QDR_A4	QDR_A3	QDR_A2	QDR_NCQ	QDR_PCQ	N
P	M_IDCLK_P	M_ID_P[15]	M_ID_P[14]	M_ECTL_P	M_ED_P[0]	BOND1	VDDL25	VDDL25	VDDC12	VDDC12	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDC12	VDDC12	VSS	QDR_A15	QDR_A5	QDR_A6	QDR_A7	QDR_A8	QDR_A9	P
R	M_IDCLK_N	M_ID_N[15]	M_ID_N[14]	M_ECTL_N	M_ED_N[0]	BOND0	VSS	VSS	VDDC12	VDDC12	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDC12	VDDC12	VTT075	QDR_A14	QDR_A12	QDR_A11	QDR_A10	QDR_D18	QDR_Q18	R
T	M_ED_P[5]	M_ED[4]_P[4]	M_ED_P[3]	M_ED_P[2]	M_ED_P[1]	VSS	VSS	VSS	VDDC12	VDDC12	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDC12	VDDC12	VTT075	QDR_A13	QDR_Q26	QDR_Q25	QDR_Q23	QDR_Q21	QDR_Q19	T
U	M_ED_N[5]	M_ED_N[4]	M_ED_N[3]	M_ED_N[2]	M_ED_N[1]	VSS	VDDA25	VDDA25	VDDC12	VDDC12	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDC12	VDDC12	VTT075	VSS	QDR_D26	QDR_D25	QDR_D23	QDR_D21	QDR_D19	U
V	M_ED_P[10]	M_ED_P[9]	M_ED_P[8]	M_ED_P[7]	M_ED_P[6]	VSS	VDDL25	VDDL25	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDH15	TRSTB	QDR_Q35	QDR_Q34	QDR_Q24	QDR_Q22	QDR_Q20	V
W	M_ED_N[10]	M_ED_N[9]	M_ED_N[8]	M_ED_N[7]	M_ED_N[6]	VSS	VDDL25	VDDL25	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDC12	VDDH15	TDI	QDR_D35	QDR_D34	QDR_D24	QDR_D22	QDR_D20	W
Y	M_EDCLK_P	M_ED_P[15]	M_ED_P[14]	M_ED_P[12]	M_ED_P[11]	VSS	VSS	VDDL25	VDDL25	VDDA25	VSS	VDDL12	VDDL12	VDDL25	VSS	VSS	VDDA25	VDDL25	VDDH25	VDDH15	B_LVDSTA	QDR_Q33	QDR_Q32	QDR_D31	QDR_D30	QDR_Q28	Y
AA	M_EDCLK_N	M_ED_N[15]	M_ED_N[14]	M_ED_N[12]	M_ED_N[11]	VSS	VSS	VDDL25	VDDL25	VDDA25	VSS	VDDL12	VDDL12	VDDL25	VSS	VSS	VDDA25	VDDL25	VSS	VSS	B_CLK_SEL	QDR_D33	QDR_D32	QDR_Q31	QDR_Q30	QDR_D28	AA
AB	M_ISCLK_L_P	M_ISTA_L_P[1]	M_ISTA_L_P[0]	M_ED_N[13]	M_ED_P[13]	DIV4	B_ESTA_T[0]	B_ICTL_P	B_ICTL_N	B_ID_P[4]	B_ID_N[4]	B_ID_P[9]	B_ID_N[9]	B_ED_P[0]	B_ED_N[0]	B_ED_P[1]	B_ED_N[1]	B_ED_P[6]	B_ED_N[6]	B_ED_P[11]	B_ED_N[11]	B_ED_P[13]	B_TRCLK	VSS	QDR_Q29	QDR_Q27	AB
AC	M_ISCLK_L_N	M_ISTA_L_N[1]	M_ISTA_L_N[0]	M_ISTA_T[0]	GPIO2	B_ESCLK_T	B_ESTA_T[1]	B_ID_P[0]	B_ID_N[0]	B_ID_P[5]	B_ID_N[5]	B_ID_P[10]	B_ID_N[10]	B_ECTL_P	B_ECTL_N	B_ED_P[2]	B_ED_N[2]	B_ED_P[7]	B_ED_N[7]	B_ED_P[12]	B_ED_N[12]	B_ED_N[13]	B_ISTA_T[0]	B_ISTA_T[1]	QDR_D29	QDR_D27	AC
AD	M_BIAS	M_REF	M_ISCLK_T	M_ISTA_T[1]	GPIO1	B_ESTA_L_P[0]	B_ESTA_L_N[0]	B_ID_P[1]	B_ID_N[1]	B_ID_P[6]	B_ID_N[6]	B_ID_P[11]	B_ID_N[11]	B_ID_P[14]	B_ID_N[14]	B_ED_P[3]	B_ED_N[3]	B_ED_P[8]	B_ED_N[8]	B_ED_P[14]	B_ED_N[14]	B_ISTA_L_P[0]	B_ISTA_L_N[0]	B_ISCLK_T	QDR_IMP	QDR_REF	AD
AE	VSS	VSS	M_CLK_SEL	TIMEBASE	GPIO0	B_ESTA_L_P[1]	B_ESTA_L_N[1]	B_ID_P[2]	B_ID_N[2]	B_ID_P[7]	B_ID_N[7]	B_ID_P[12]	B_ID_N[12]	B_ID_P[15]	B_ID_N[15]	B_ED_P[4]	B_ED_N[4]	B_ED_P[9]	B_ED_N[9]	B_ED_P[15]	B_ED_N[15]	B_ISTA_L_P[1]	B_ISTA_L_N[1]	B_REF	VSS	VDDH15	AE
AF		VDDT33	MRCLK	RESETB	M_LVDSTA	B_ESCLK_L_P	B_ESCLK_L_N	B_ID_P[3]	B_ID_N[3]	B_ID_P[8]	B_ID_N[8]	B_ID_P[13]	B_ID_N[13]	B_IDCLK_P	B_IDCLK_N	B_ED_P[5]	B_ED_N[5]	B_ED_P[10]	B_ED_N[10]	B_EDCLK_P	B_EDCLK_N	B_ISCLK_L_P	B_ISCLK_L_N	B_BIAS	VDDT33		AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 52 88K8483 Top View Pinout

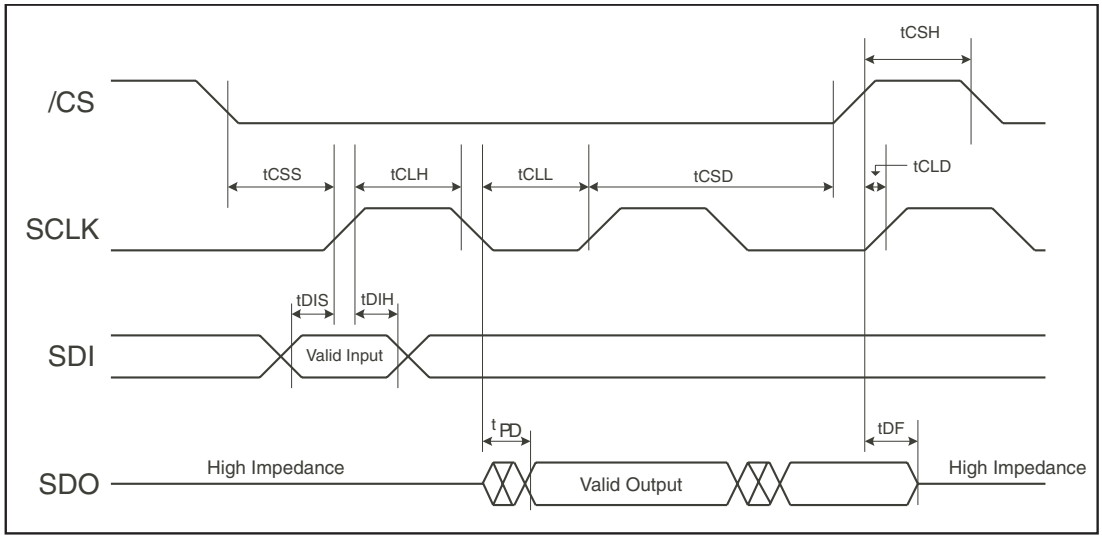


Figure 53 Serial Peripheral Interface

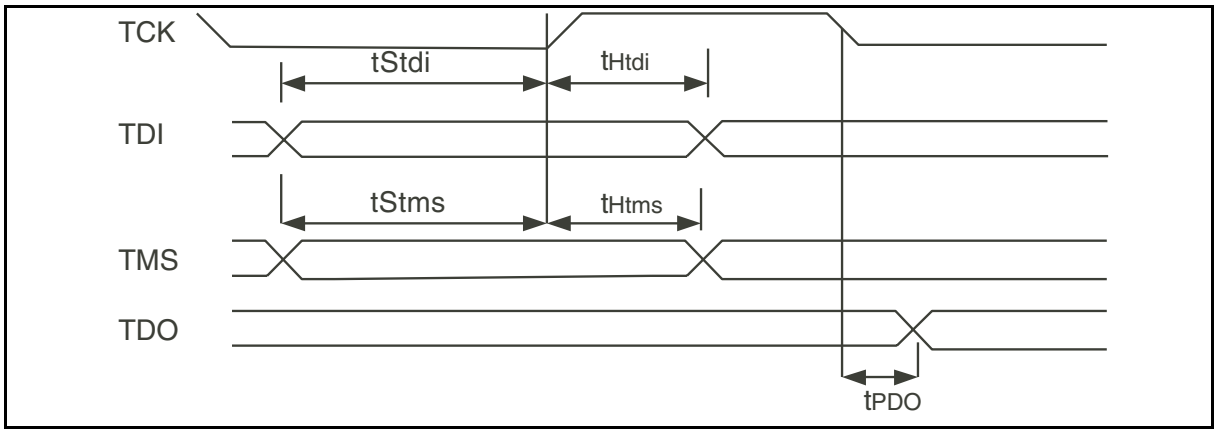


Figure 54 JTAG Interface

Mechanical data

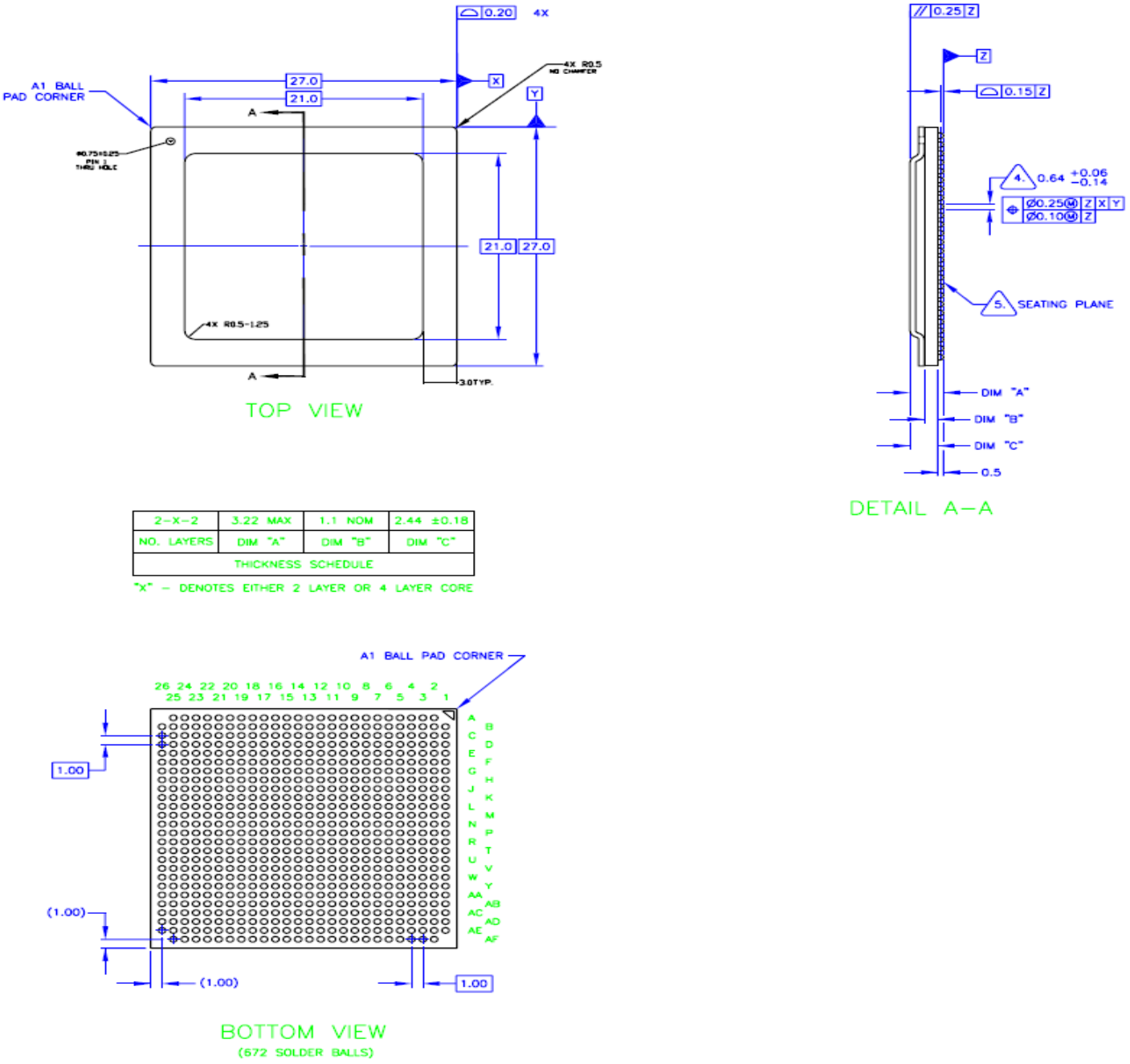


Figure 55 BR 672 FCBG Package Outline, RoHS compliant

Document Revision History

The document revision history is described in Table 169.

Issue	Date	Description
1.0	10/20/2006	General Release

Table 169 Document Revision History

Ordering Information

The ordering information is described in Table 170.

Device Code	Product
IDT88K8483BRI	IDT88K8483 SPI-4 Exchange, Industrial temperature, RoHS 6
IDT88K8483BLI	IDT88K8484 SPI-4 Exchange, Industrial temperature, RoHS 5

Table 170 Ordering Information

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