



16-BIT CMOS CASCADABLE ALU

IDT7381

FEATURES:

- High-performance 16-bit Arithmetic Logic Unit (ALU)
- 25ns to 55ns clocked ALU operations
- Ideal for radar, sonar or image processing applications
- 74S381 instruction set (8 functions)
- Replaces Gould S614381 or Logic Devices L4C381
- Cascadable with or without carry look-ahead
- Pipeline or flow-through modes
- Internal feedback path for accumulation
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CMOS technology
- Available in PLCC
- Speeds available: L/25/30/40/55

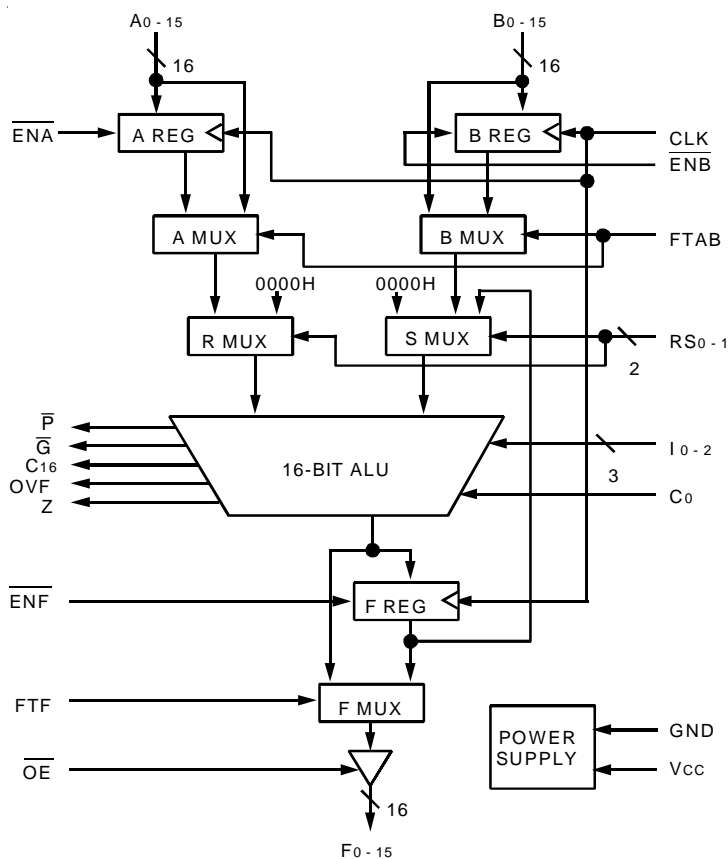
DESCRIPTION:

The IDT7381 is a high-speed cascadable Arithmetic Logic Unit (ALU). These three-bus devices have two input registers, an ultra-fast 16-bit ALU and 16-bit output register. With IDT's high-performance CMOS technology, the IDT7381 can do arithmetic or logic operations in 25ns. The IDT7381 functionally replaces four 54/74S381 four-bit ALUs in a 68-pin package.

The two input operands, A and B, can be clocked or fed through for flexible pipelining. The F output can also be set into clocked or flow-through mode. An output enable is provided for three-state control of the output port on a bus.

The IDT7381 has three function pins to select 1 of 8 arithmetic or logic operations. The two R and S selection pins determine whether A, B, F or 0 are fed into the ALU. This ALU has carry-out, propagate and generate outputs for cascading using carry look-ahead.

FUNCTIONAL BLOCK DIAGRAM

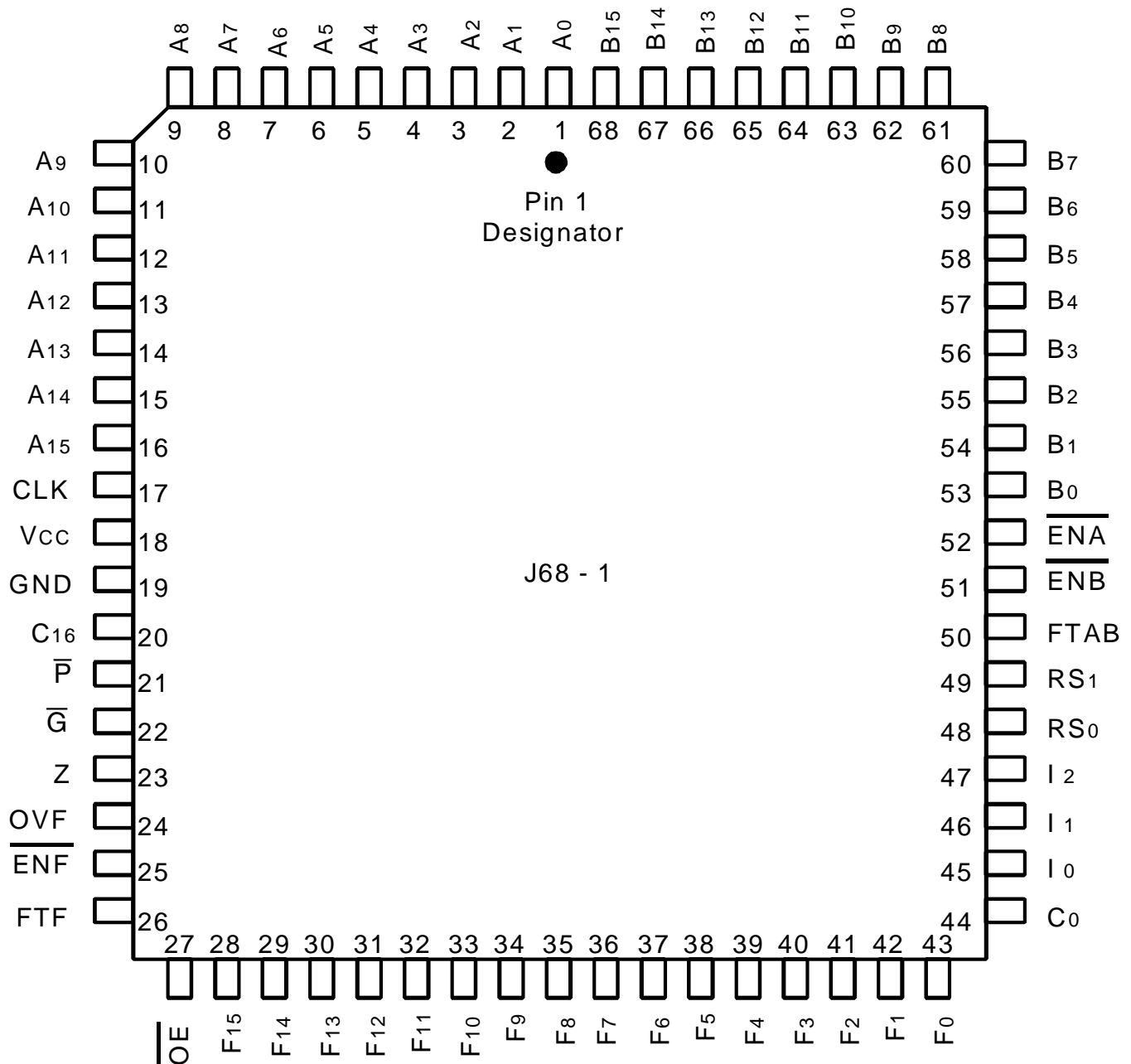


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COMMERCIAL TEMPERATURE RANGE

APRIL 2001

PIN CONFIGURATION



PLCC
TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Description
A0 - A15	I	Sixteen-bit data input port.
B0 - B15	I	Sixteen-bit data input port.
$\overline{\text{ENA}}$	I	Register enable for the A input port; active low pin.
$\overline{\text{ENB}}$	I	Register enable for the B input port; active low pin.
FTAB	I	Flow-through control pin. When this pin is high, both register A and B are transparent.
F0 - F15	O	Sixteen-bit data output port.
$\overline{\text{ENF}}$	I	Register enable for the F output port; active low pin.
FTF	I	Flow-through control pin. When this pin is high, the F register is transparent.
CLK	I	Clock input.
$\overline{\text{OE}}$	I	Output enable control pin. When this pin is high, the output port F is in a high impedance state. When low, the output port F is active.
C0	I	Carry input. This pin receives arithmetic carries from less significant ALU components in a cascade configuration.
C16	O	Carry output. This pin produces arithmetic carries to more significant ALU components in a cascaded configuration.
OVF	O	This pin indicates a two's complement arithmetic overflow, when high.
Z	O	This pin indicates a zero output result, when high.
RS0 - RS1	I	Two control pins used to select input operands for the R and S multiplexers.
I0 - I2	I	Three control pins to select the ALU function performed.
P	O	Indicates the carry propagate output state to the ALU.
$\overline{\text{G}}$	O	Indicates the carry generate output state to the ALU.
Vcc		Power supply pin, 5V.
GND		Ground pin, 0V.

R AND S MUX TABLE

RS1	RS0	R Mux	S Mux
0	0	A	F
0	1	A	0
1	0	0	B
1	1	A	B

ALU FUNCTION TABLE

I2	I1	I0	Function
0	0	0	$F = 0$
0	0	1	$F = \overline{R} + S + C_0$
0	1	0	$F = R + \overline{S} + C_0$
0	1	1	$F = R + S + C_0$
1	0	0	$F = R \text{ xor } S$
1	0	1	$F = R \text{ or } S$
1	1	0	$F = R \text{ and } S$
1	1	1	$F = \text{all } 1\text{'s}$

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM}	Terminal Voltage with Respect to Ground	-0.5 to V _{CC} + 0.5	V
V _{CC}	Power Supply Voltage	-0.5 to +7.0	V
T _{STG}	Storage Temperature	-55 to +125	°C
I _{OUT}	DC Output Current	50	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Under no circumstances should an input of an I/O Pin be greater than V_{CC} + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Pkg.	Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	PGA	10	pF
			PLCC	5	
C _{OUT}	Output Capacitance	V _{OUT} = 0V	PGA	12	pF
			PLCC	7	

NOTE:

- This parameter is sampled at initial characterization and is not production tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = 2.7V	—	—	10	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = 0.5V	—	—	-10	μA
I _{OS} ⁽³⁾	Short Circuit Current	V _{CC} = Max., V _{OUT} = GND	-20	—	-100	mA
I _{OZ}	Off State (High Impedance) Output Current	V _{CC} = Max.	—	-0.1	-20	μA
		V _O = 0.5V	—	-0.1	20	
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	2.4	—	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	—	—	0.5	V

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}	—	2	6	mA	
ΔI _{CC} ⁽³⁾	Quiescent Power Supply Current TTL Input HIGH	V _{CC} = Max. V _{IN} = 3.4V	—	0.5	1	mA/ input	
I _{CCD} ⁽⁴⁾	Dynamic Power Supply Current	V _{CC} = Max. Outputs disabled V _{IN} = GND or V _{CC} Mode: FTAB = FTF = 1	—	15	48	μA/ MHz	
I _{CCD1}	Dynamic Power Supply Current	V _{CC} = Max. Outputs Disabled All Data Inputs Disabled f _i = 10MHz, f _{CP} = 10MHz 50% Duty Cycle V _{IL} = GND, V _{IH} = V _{CC} Mode: FTAB = FTF = 1	—	20	33	mA	
I _{CCD2} ⁽⁶⁾	Dynamic Power Supply Current	V _{CC} = Max. Outputs Enabled. (CL = 50pF) All Data Inputs Switching f _i = 10MHz, f _{CP} = 10MHz 50% Duty Cycle V _{IL} = GND, V _{IH} = V _{CC} Mode: FTAB = FTF = 1	—	40	60	mA	
I _C ⁽⁷⁾	Total Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC} All Data Inputs Switching f _i = 10MHz, f _{CP} = 10MHz 50% Duty Cycle	Outputs Disabled	—	22	39	mA
			Outputs Enabled	—	42	76	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived from I_{CCD1} for use in Total Power Supply calculations.
- Total power supply current is calculated as follows:
 $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH_{NT} + I_{CCD} (f_{CP} + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 DH = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at DH
 I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.
- This parameter is not production tested but is an indicator of the power dissipated with outputs loaded.
- Values for these conditions are examples of the I_C formula in note 5 above. These are guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C)

Maximum Combinational Propagation Delays									
From Input	IDT7381L25				IDT7381L30				Unit
	F ₀₋₁₅	$\overline{P}, \overline{G}, N$	Z,OVF	C ₁₆	F ₀₋₁₅	$\overline{P}, \overline{G}, N$	Z,OVF	C ₁₆	
FTAB = 0, FTF = 0									
CLK	13	22	26	22	20	28	30	28	ns
C ₀	—	—	16	16	—	—	20	20	ns
I ₀₋₂ , RS ₀ , RS ₁	—	22	22	22	—	28	28	28	ns
FTAB = 0, FTF = 1									
CLK	27	22	26	22	33	28	30	28	ns
C ₀	22	—	16	16	28	—	20	20	ns
I ₀₋₂ , RS ₀ , RS ₁	22	22	22	22	28	28	28	28	ns
FTAB = 1, FTF = 0									
A _{0-A15} , B _{0-B15}	—	18	25	22	—	24	30	28	ns
CLK	13	—	—	—	19	—	—	—	ns
C ₀	—	—	16	16	—	—	20	20	ns
I ₀₋₂ , RS ₀ , RS ₁	—	22	22	22	—	28	28	28	ns
FTAB = 1, FTF = 1									
A _{0-A15} , B _{0-B15}	26	18	25	22	32	24	30	28	ns
C ₀	22	—	16	16	28	—	20	20	ns
I ₀₋₂ , RS ₀ , RS ₁	22	22	22	22	28	28	28	28	ns

Maximum Combinational Propagation Delays									
From Input	IDT7381L40				IDT7381L55				Unit
	F ₀₋₁₅	$\overline{P}, \overline{G}, N$	Z,OVF	C ₁₆	F ₀₋₁₅	$\overline{P}, \overline{G}, N$	Z,OVF	C ₁₆	
FTAB = 0, FTF = 0									
CLK	26	30	44	32	32	38	53	36	ns
C ₀	—	—	28	20	—	—	34	22	ns
I ₀₋₂ , RS ₀ , RS ₁	—	32	34	35	—	42	42	42	ns
FTAB = 0, FTF = 1									
CLK	46	30	44	32	56	38	53	36	ns
C ₀	30	—	28	20	37	—	34	22	ns
I ₀₋₂ , RS ₀ , RS ₁	40	32	34	35	55	42	42	42	ns
FTAB = 1, FTF = 0									
A _{0-A15} , B _{0-B15}	—	30	40	32	—	36	46	37	ns
CLK	26	—	—	—	32	—	—	—	ns
C ₀	—	—	28	20	—	—	34	22	ns
I ₀₋₂ , RS ₀ , RS ₁	—	32	34	35	—	42	42	42	ns
FTAB = 1, FTF = 1									
A _{0-A15} , B _{0-B15}	40	30	40	32	55	36	46	37	ns
C ₀	30	—	28	20	37	—	34	22	ns
I ₀₋₂ , RS ₀ , RS ₁	40	32	34	35	55	42	42	42	ns

NOTES:

1. Only for FTF = 0.
2. Minimum propagation delays are not production tested but guaranteed to be greater than or equal to 3ns.

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$) - (Cont'd.)

Minimum Set-up and Hold Times Relative to Clock (CLK)									
Input	IDT7381L25		IDT7381L30		IDT7381L40		IDT7381L55		Unit
	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	
FTAB = 0, FTF = X									
A0–A15, B0–B15	6	0	6	0	6	0	8	0	ns
C0 ⁽¹⁾	16	0	16	0	16	0	21	0	ns
I0–2, RS0, RS1 ⁽¹⁾	24	0	29	0	32	0	44	0	ns
EN \bar{A} , EN \bar{B} , EN \bar{F}	6	0	6	0	6	0	8	0	ns
FTAB = 1, FTF = 0									
A0–A15, B0–B15	16	0	25	0	28	0	35	0	ns
C0	16	0	16	0	16	0	21	0	ns
I0–2, RS0, RS1	24	0	29	0	32	0	44	0	ns
EN \bar{F}	6	0	6	0	6	0	8	0	ns

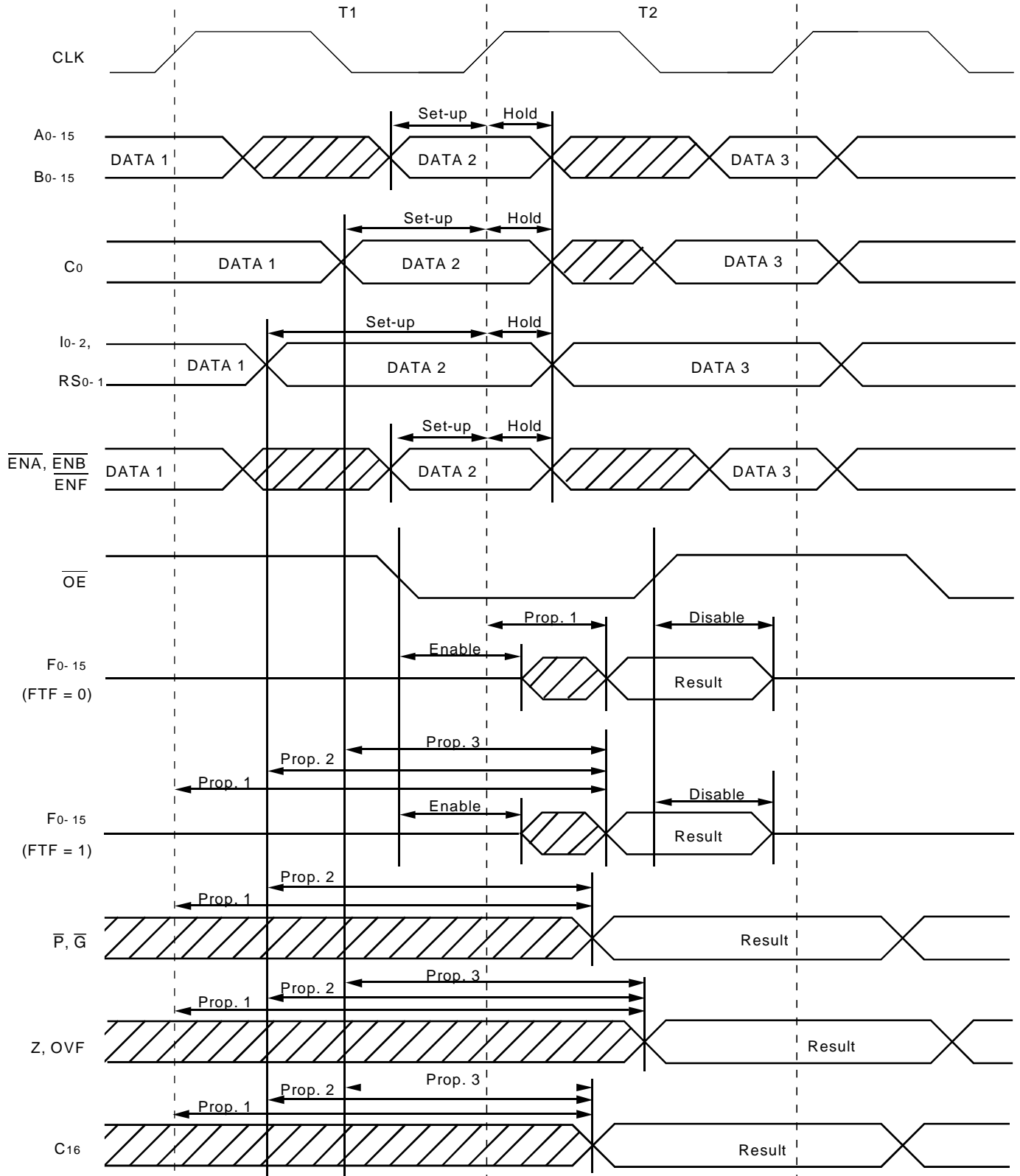
Minimum Clock Cycle Times and Pulse Widths					
Parameter	IDT7381L25	IDT7381L30	IDT7381L40	IDT7381L55	Unit
Clock LOW Time	6	8	10	14	ns
Clock HIGH Time	6	8	10	14	ns
Clock Period	20	25	34	43	ns

Maximum Output Enable/Disable Times					
Parameter	IDT7381L25	IDT7381L30	IDT7381L40	IDT7381L55	Unit
Enable Time	10	15	18	20	ns
Disable Time	10	15	18	20	ns

NOTES:

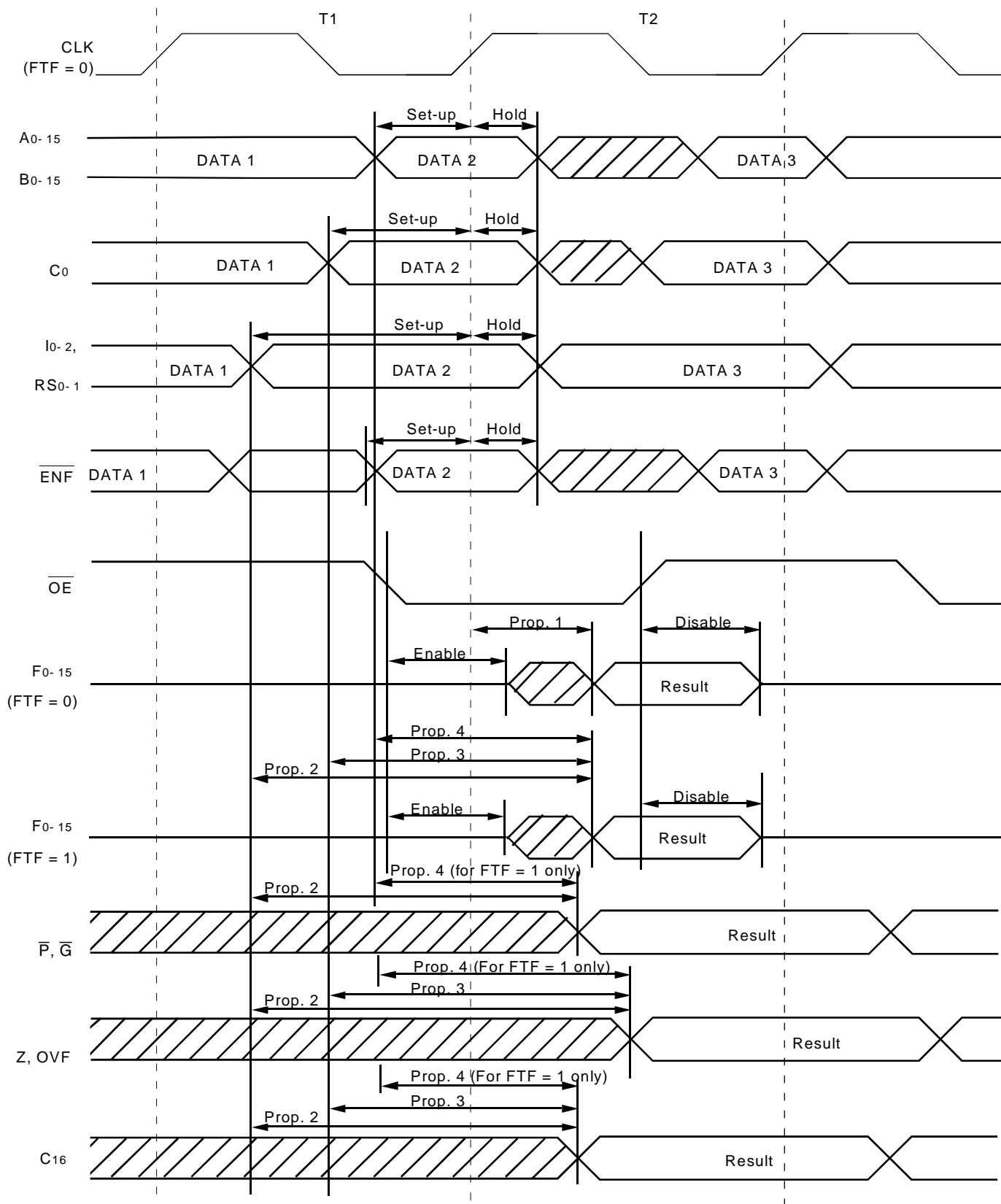
1. Only for FTF = 0.
2. Minimum propagation delays are not production tested but guaranteed to be greater than or equal to 3ns.

WAVEFORMS FOR FTAB = 0, FTF = X



- Prop. 1: Propagation delay with respect to the CLK.
- Prop. 2: Propagation delay with respect to I0-2, RS0-2.
- Prop. 3: Propagation delay with respect to C0.

WAVEFORMS FOR FTAB = 1, FTF = X



- Prop. 1: Propagation delay with respect to the CLK.
- Prop. 2: Propagation delay with respect to I0-2, RS0-2.
- Prop. 3: Propagation delay with respect to C0.
- Prop. 4: Propagation delay with respect to A, B.

PROPAGATION DELAY CALCULATIONS FOR TWO IDT7381S

From Input	To Output		To Set PUT Time Relative to Clock (CLK)
	F0-15	Flags ⁽¹⁾	
FTAB = 0, FTF = 0			
CLK	As in 16-bit case	(Clk → C16) + (C0 → flag)
C0	(C0 → C16) + (C0 → flag)	(C0 → C16) + (C0 set-up time)
I0-2, RS0-1	(I0-2, RS0-1 → C16) + (C0 → flag)	(I0-2, RS0-1 → C16) + (C0 set-up time)
A0-15, B0-15	As in 16-bit case
ENA, ENB, ENF	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	(Clk → C16) + (C0 → F0-15)	(Clk → C16) + (C0 → flag)
C0	(C0 → C16) + (C0 → F0-15)	(C0 → C16) + (C0 → flag)	(C0 → C16) + (C0 set-up time)
I0-2, RS0-1	(I0-2, RS0-1 → C16) + (C0 → F0-15)	(I0-2, RS0-1 → C16) + (C0 → flag)	(I0-2, RS0-1 → C16) + (C0 set-up time)
A0-15, B0-15	As in 16-bit case
ENA, ENB, ENF	As in 16-bit case
FTAB = 1, FTF = 0			
CLK	As in 16-bit case
C0	(C0 → C16) + (C0 → flag)	(C0 → C16) + (C0 set-up time)
I0-2, RS0-1	(I0-2, RS0-1 → C16) + (C0 → flag)	(I0-2, RS0-1 → C16) + (C0 set-up time)
A0-15, B0-15	(A0-15, B0-15 → C16) + (C0 → flag)	As in 16-bit case
ENA, ENB, ENF	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	Don't care condition	Don't care condition
C0	(C0 → C16) + (C0 → F0-15)	(C0 → C16) + (C0 → flag)
I0-2, RS0-1	(I0-2, RS0-1 → C16) + (C0 → F0-15)	(I0-2, RS0-1 → C16) + (C0 → flag)
A0-15, B0-15	(A0-15, B0-15 → C16) + (C0 → F0-15)	(A0-15, B0-15 → C16) + (C0 → flag)
ENA, ENB, ENF

NOTE:

1. Flags are \bar{P} , \bar{G} , OVF, Z and C16.

CASCADING THE IDT7381

Some applications require 32-bit or wider input operands. Cascading is the hardware solution. It provides a high speed alternative in handling more than 16-bit wide operands.

1. Cascading the IDT7381

Cascading to 32-bit wide operands takes only two IDT7381s and no external hardware. However, cascading to data widths greater than 32-bit can be done in two ways: without external hardware (slow method) or by using a carry look ahead generator.

- a) Cascading the IDT7381 without a carry-look-ahead generator: (Figures 1 and 2)
 1. Connect the C₁₆ output of the least significant device into the C₀ input of the next most significant device.
 2. Common lines to all devices are: RS₀₋₁, I₀₋₂, Clk, FTF, FTAB, \overline{ENA} , \overline{ENB} , \overline{ENF} .
 3. Take OVF, C₁₆, \overline{P} , \overline{G} of the most significant device as valid.
 4. The system's zero flag (Z) is obtained by ANDing all zero flag results.
- b) Cascading three or more IDT7381s with carry-look-ahead (CLA) generator: (Figure 3)
 1. Connect the \overline{P} and \overline{G} outputs of each device to the CLA generator's corresponding inputs.
 2. Take the CLA generator outputs into the C₀ inputs of each device (except for the least significant one).
 3. Common lines to all devices are: RS₀₋₁, I₀₋₂, Clk, FTF, FTAB, \overline{ENA} , \overline{ENB} , \overline{ENF} .
 4. Take OVF, C₁₆, \overline{P} , \overline{G} of the most significant device as valid.
 5. Carry-in to the system should be connected to the C₀ input of the least significant device and also to the CLA generator.

2. Time Delay Considerations

Once cascading has taken place, time delays may become critical in high performance systems. Our main interest here is focused on "propagation delays", i.e. calculating the time required for an input signal to propagate through several cascaded devices up to a specific output in another device within the cascaded system.

Propagation Delay

The propagation delay *for two devices* between the input and output of interest (input to output delay) is done as follows:

1. Calculate delay between the input and C₁₆ in the first device.
2. Calculate delay between C₀ and the output in the second device.
3. Add both results.

The following table is an example on how to build a propagation delay table for all inputs in a 32-bit IDT7381 cascaded system.

Propagation delay calculations can be extended to *n-cascaded* devices as the sum of the delays in all devices between the input and output of interest. That is:

$$(\text{Input})_1 \rightarrow (\text{C16})_1 = t_1$$

...

$$(\text{C0})_i \rightarrow (\text{C16})_i = t_i$$

$$(\text{C0})_{i+1} \rightarrow (\text{C16})_{i+1} = t_{i+1}$$

...

$$(\text{C0})_n \rightarrow (\text{Output})_n = t_n$$

Where the subscript *i* denotes the device number and the arrow (\rightarrow) represents the delay in between. Notice that *i + 1* is the immediate upper device from device *i*. Adding the delays *t_i* we get:

$$\text{Propagation delay} = t_1 + t_2 + \dots + t_i + t_{i+1} + \dots + t_n$$

Total Delay

As seen from Figure 8, the propagation delay is within the IDT7381 devices only. A complete analysis should also include the delay associated with the transmission line *L_i* (which depends on the line length and its impedance). This line delay should then be added to the propagation delay to obtain the total delay for the cascaded system:

$$\text{Total delay} = \text{Propagation delay} + \text{Transmission line delay}$$

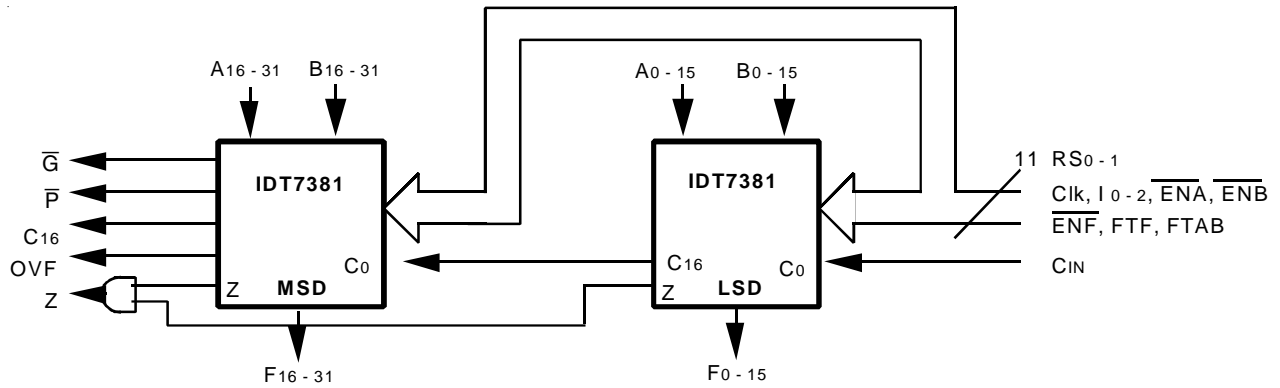


Figure 1. Cascading Two IDT7381s to 32 Bits

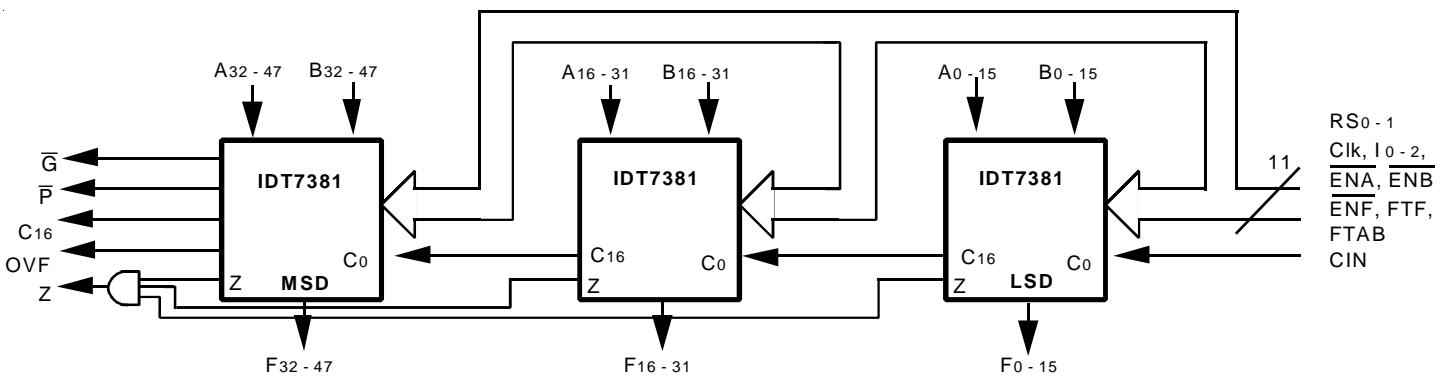


Figure 2. Cascading Three IDT7381s to 48 Bits Wide without a Carry-lookahead Generator

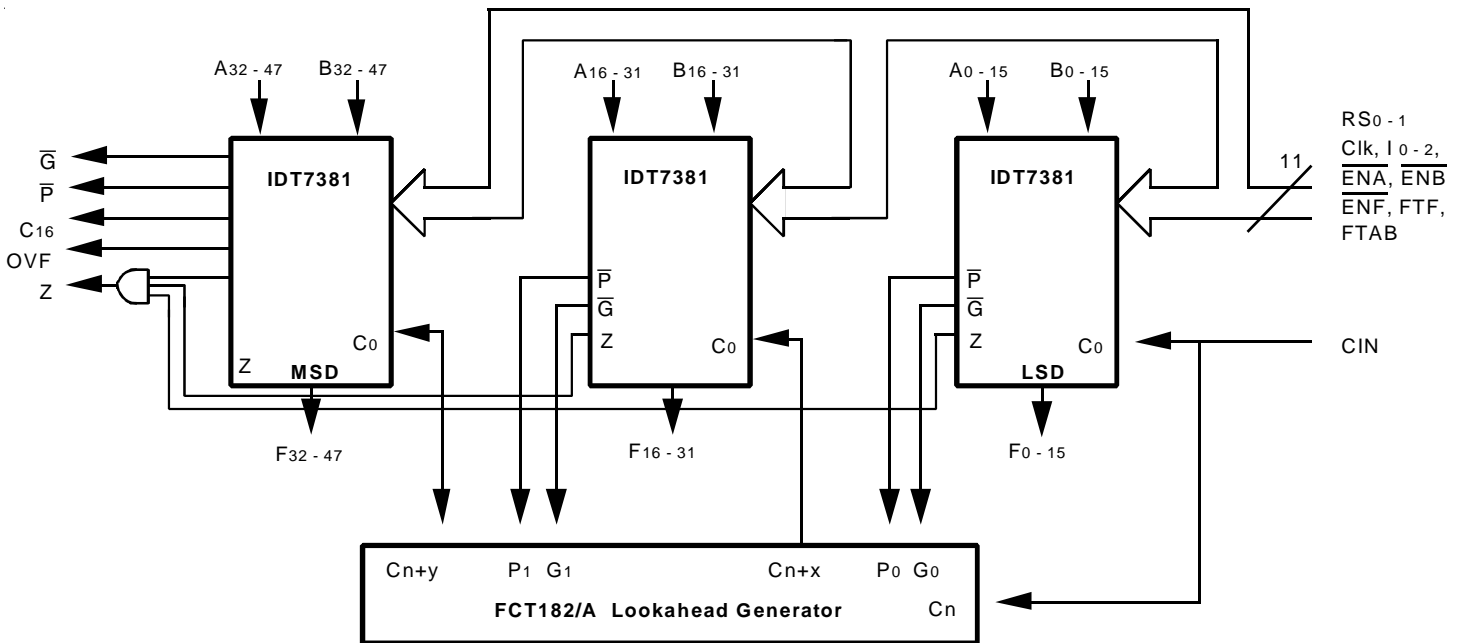


Figure 3. Cascading Three IDT7381s to 48 Bits Wide with a Carry-lookahead Generator

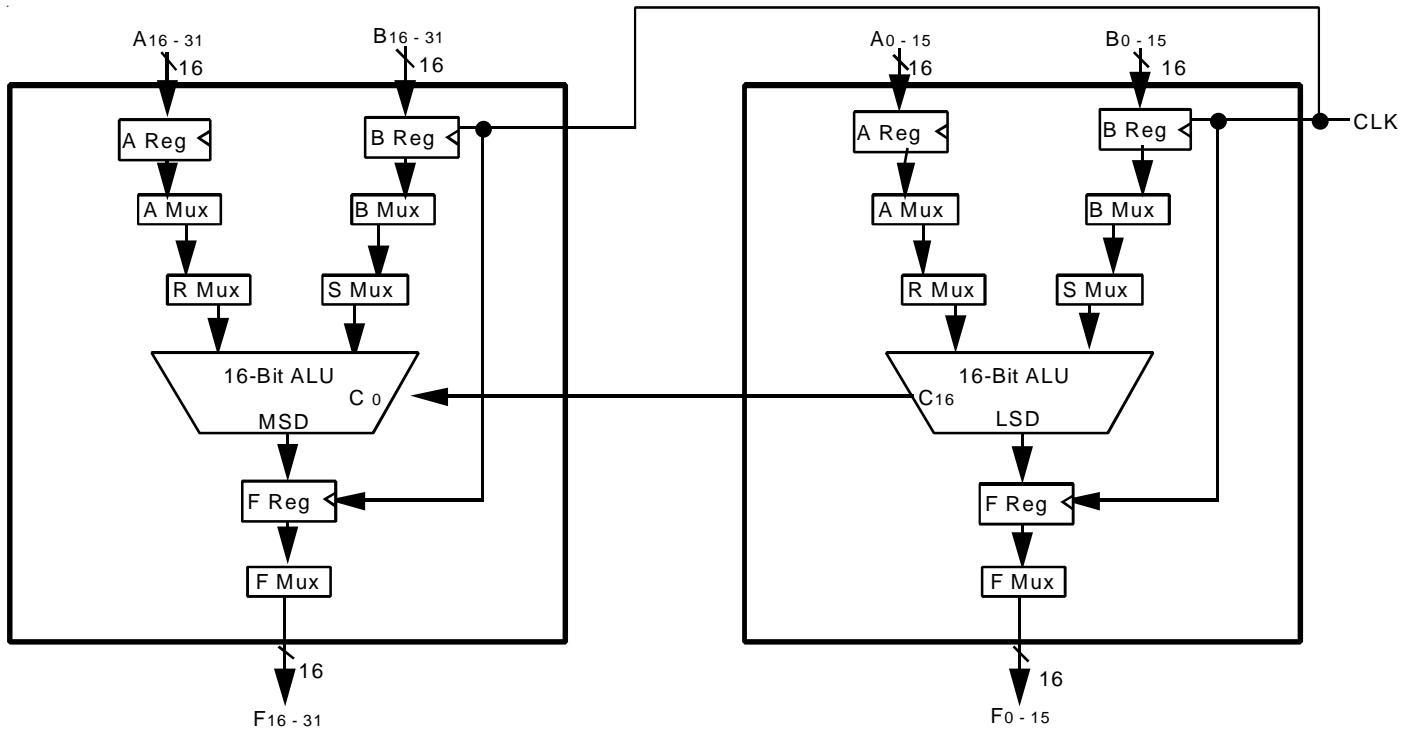


Figure 4. 32-Bit Configuration for FTAB = 0, FTF = 0

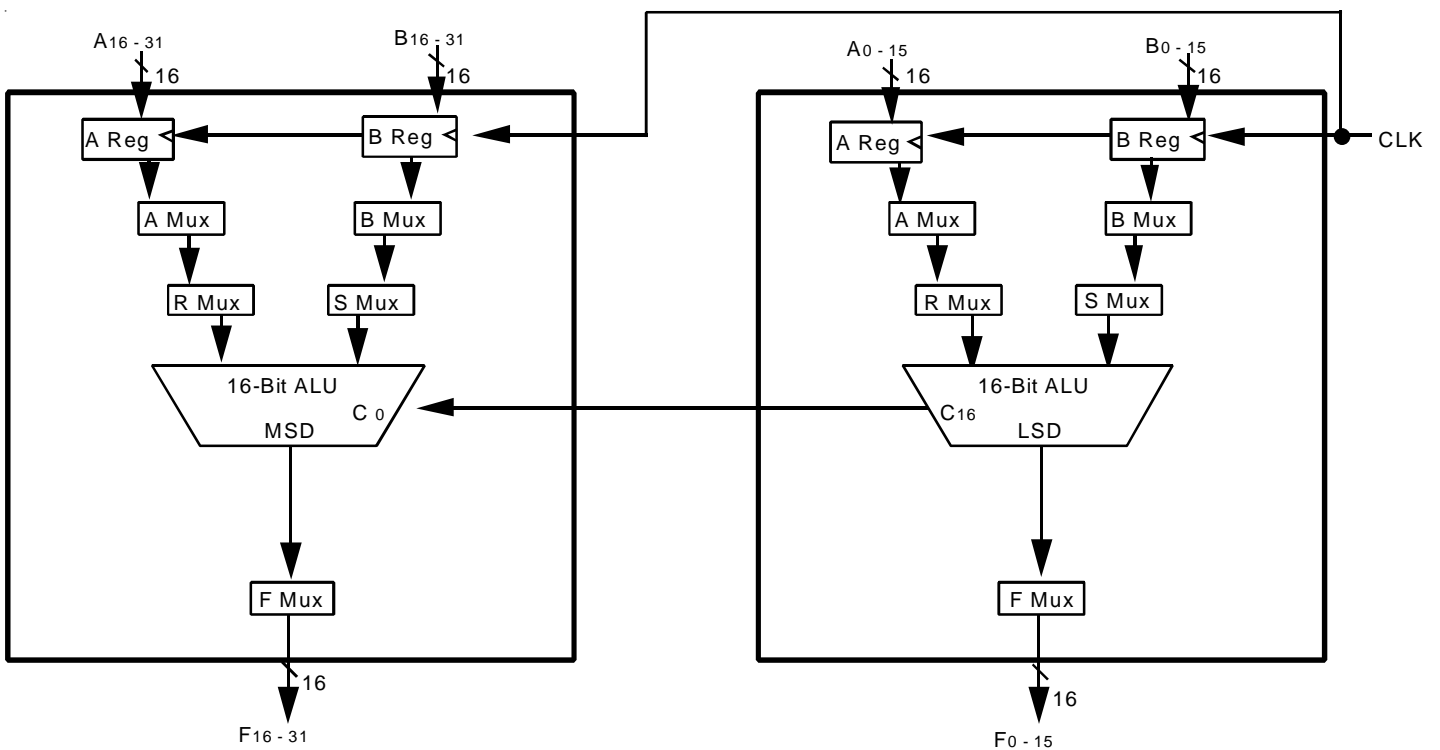


Figure 5. 32-Bit Configuration for FTAB = 0, FTF = 1

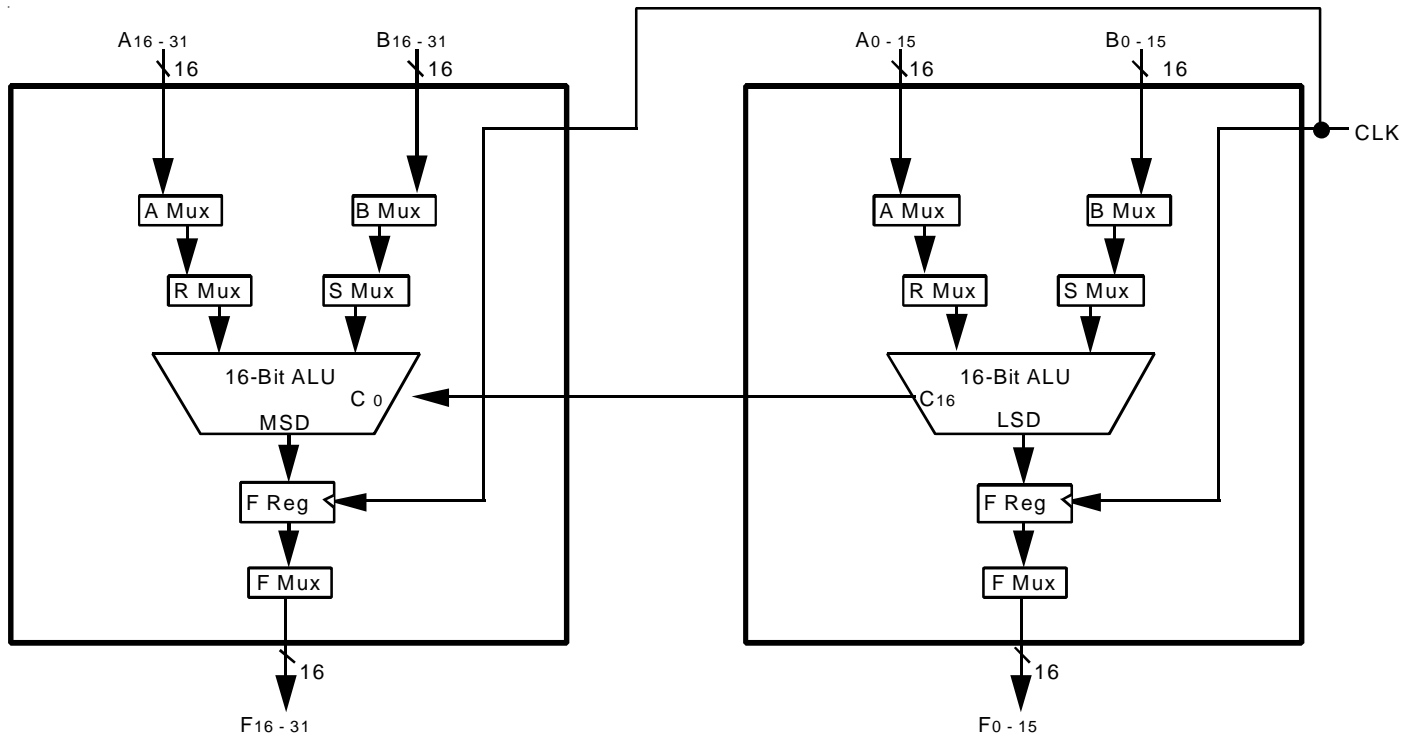


Figure 6. 32-Bit Configuration for FTAB = 1, FTF = 0

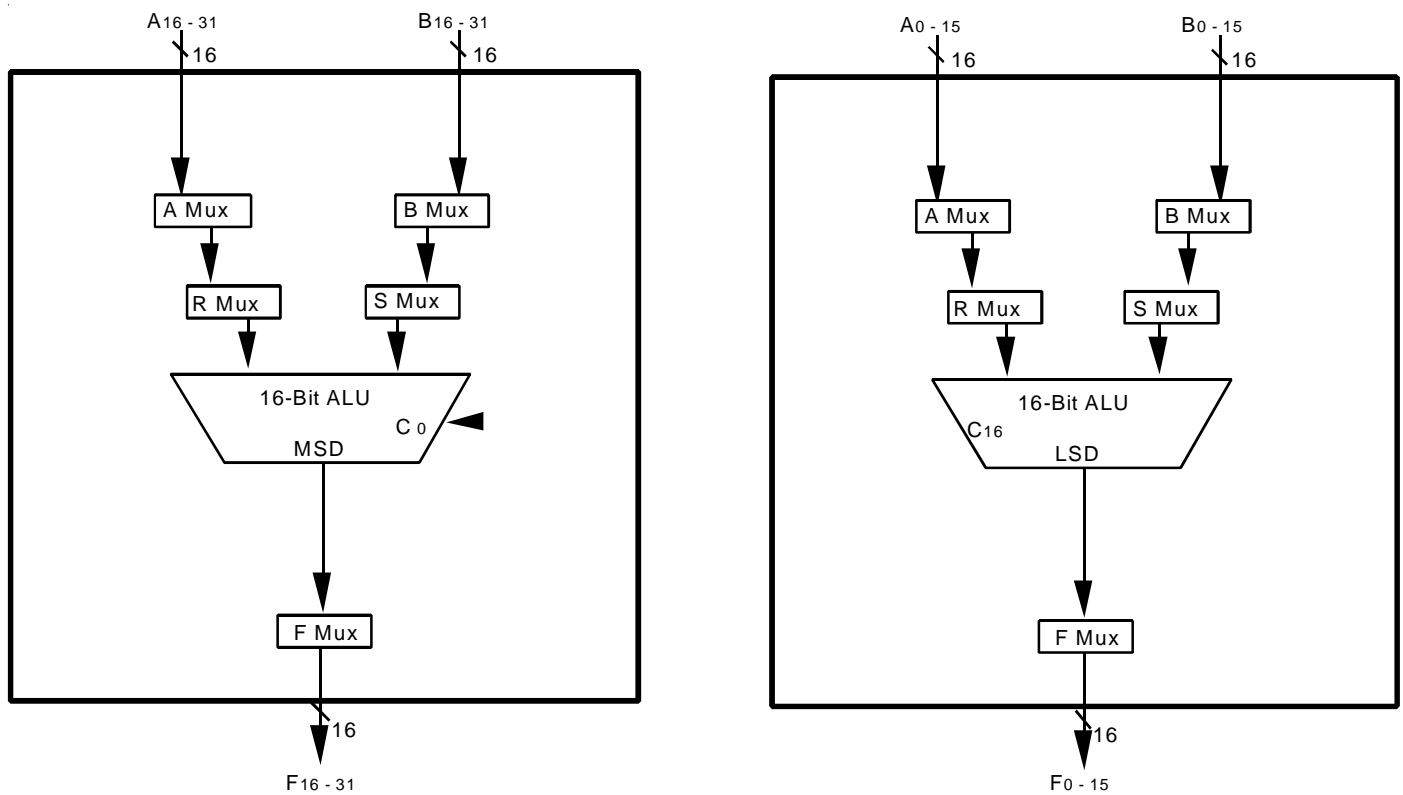


Figure 7. 32-Bit Configuration for FTAB = 1, FTF = 1

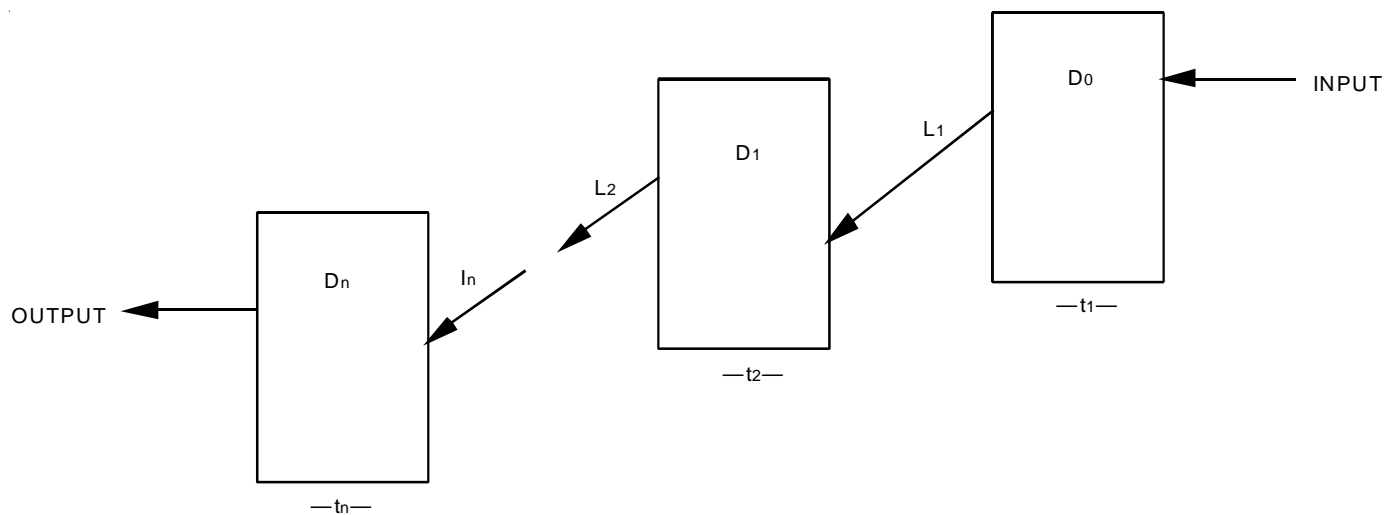


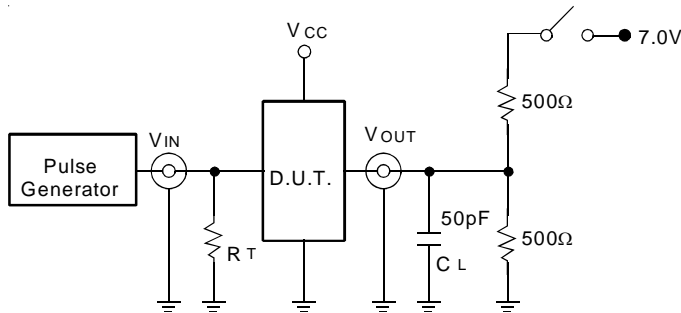
Figure 8. Propagation Delay = $t_1 + t_2 + \dots + t_n$ N-Cascaded Devices

AC TEST CONDITIONS

Input Rise levels	GND to 3V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figure 1

TEST WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



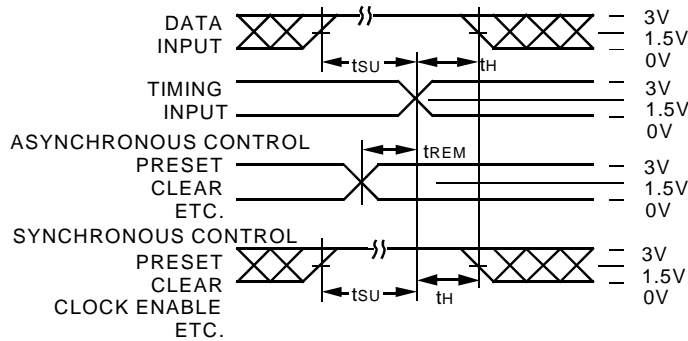
SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

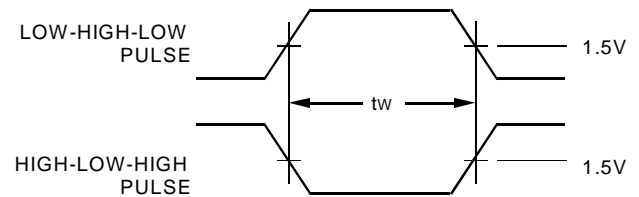
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

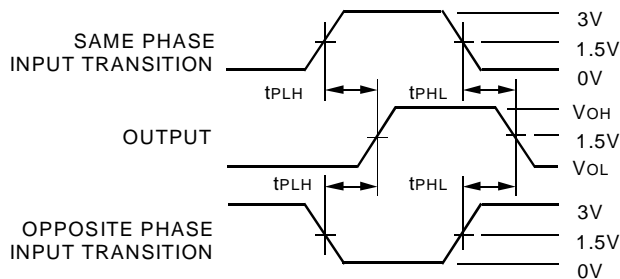
SET-UP, HOLD, AND RELEASE TIMES



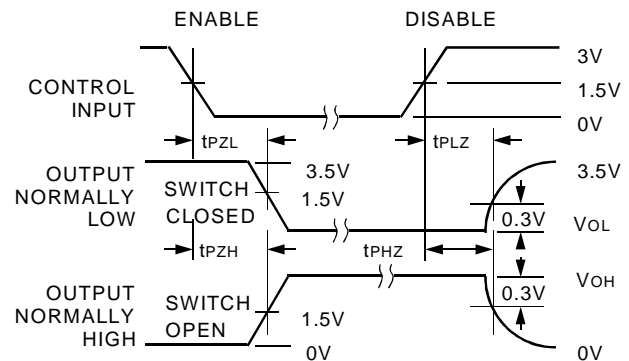
PULSE WIDTH



PROPAGATION DELAY



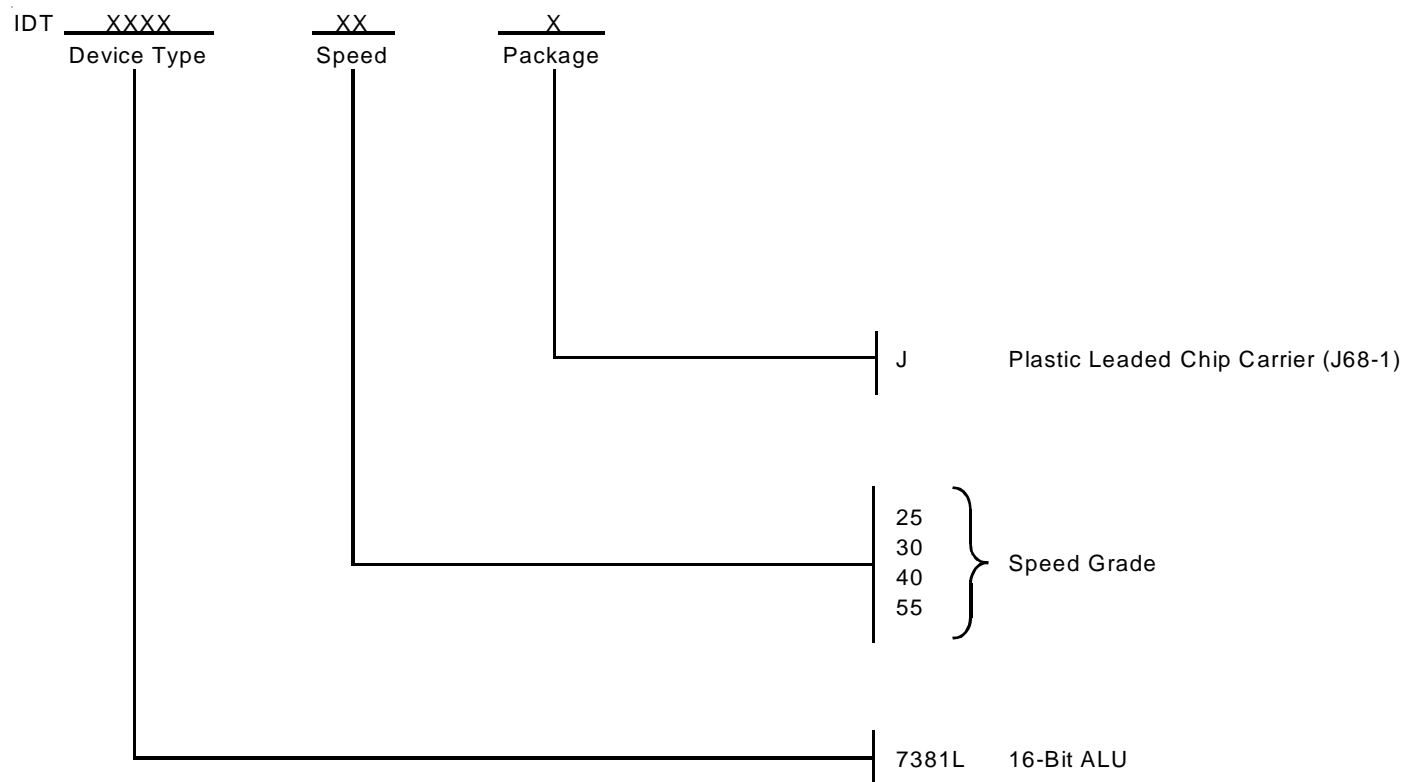
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$

ORDERING INFORMATION



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