INTEGRATED CIRCUITS
UNITRODE

UCC1883
UCC2883
UCC3883

Micropower Peak Current Mode Controller

ISDN I.430 RELATED FEATURES

- Zero-Power Startup Capability
- Restricted Mode Detection
- Precision Programmable Quiescent Current
- Very Low Quiescent Power for CCITT, 25mW Restricted Mode
- Programmable Continuous Input Current Limit

GENERAL FEATURES

- Low Power Peak Current Mode Controller
- Oscillator Synchronizes to Secondary Side Clock
- Leading Edge Blanking of Current Sense Waveform
- 50% Maximum Duty Cycle
- Undervoltage Lockout with Hysteresis
- 5V V_{DD} Logic Supply Regulator
- Programmable Low Line Sensing

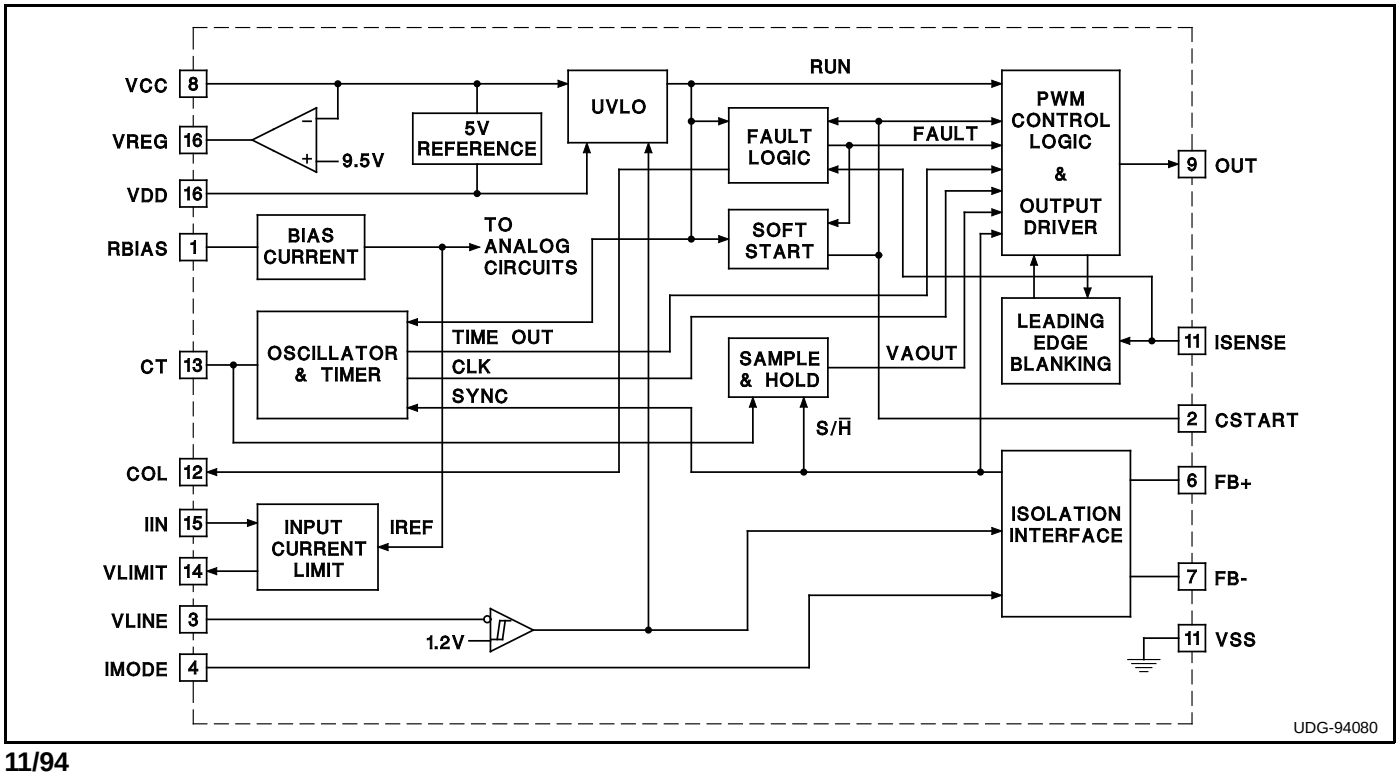
DESCRIPTION

The UCC1883 is a peak current mode PWM controller designed to operate in conjunction with the UCC1885 secondary-side regulation IC. Together these devices provide the features to implement a fully isolated switch mode power supply with improved output regulation. In addition, this combination of ICs will allow a converter to meet the guidelines set forth in CCITT ISDN recommendation I.430. The chip set is intended mainly for use in DC/DC discontinuous flyback power converters, which are the most economical for developing multiple output voltages. Peak current mode control offers the advantages of pulse-by-pulse current limiting, automatic feedforward, and improved load response characteristics. The UCC1885 companion IC provides feedback control voltage and oscillator synchronization information to the UCC1883 via an isolation pulse transformer. The UCC1883 uses the feedback voltage and frequency information from the UCC1885 to determine the current loop control voltage, i.e. the voltage analog of the current commanded by the voltage loop. This internal control voltage is, in turn, used by the UCC1883 in a conventional peak current mode PWM circuit. Internal leading edge blanking of the current sense waveform eliminates the need for an external filtering network on the ISENSE input. When in restricted mode or lightly loaded, the UCC1883 operates with a minimum pulse width determined by the leading edge blanking circuit. This eliminates the spurious EMI generated if arbitrarily short output pulses are produced by the PWM.

In addition to pulse-by-pulse current limiting, an overcurrent threshold is maintained. A fault condition may also be triggered by repeated peak current limit conditions, through the use of the programmable output overload detector. If either of these faults is detected, OUT is immediately disabled, and a programmable restart period occurs before a soft start sequence is initiated.

continued

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 16.5
Maximum VCC Slew Rate 10V/ms
Maximum Voltage:
RBIAS, CSTART, VLINE
IMODE, FB+, FB-, OUT, VREG . . . . . VCC + 0.3V to 18V
VDD 7V
COL, ISENSE, CT . . . . . VDD + 0.3V to 7V
VLIMIT, IIN 0.3V
Minimum Voltage:
VLIMIT . . . . . –VCC
All Other Pins . . . . . –0.3V
Maximum DC Current, Any Pin, Source or Sink 100mA
Maximum Peak Current, Any Pin, Source or Sink 500mA
Storage Temperature . . . . . –65°C to+150°C
Junction Temperature. . . . . –55°C to+150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Note 1: All voltages expressed with respect to VSS, currents are positive into the specified terminal.

Note 2: All maximum signal pin voltage limits apply for cases of zero source impedance. Higher or lower voltages may be impressed through a finite source impedance which causes the input current to be limited to the values specified with total package power dissipation at or below specified limits.

Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

DESCRIPTION (cont.)

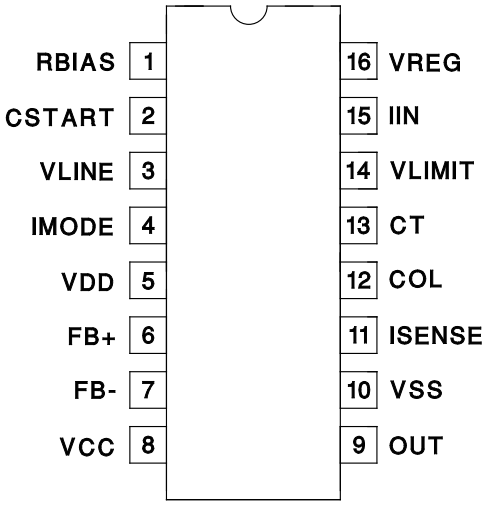
ISDN-specific features allow the UCC1883/UCC1885 combination to be compatible with CITT Recommendation I.430. The linear pre-regulator is intended to control a depletion-mode NMOS pass transistor, such as BSS129. Startup power drawn from the line can be reduced to zero if a bootstrap winding provides power to the UCC1883 VCC pin. An internal current comparator is provided to sense restricted mode directly from the input to the converter. Maximum input current may be accurately programmed and continuously limited with the use of an external PMOS pass transistor. Precision programming of the quiescent current used by the UCC1883 allows the system to meet the 25mW restricted mode power limit, or the current can be set to achieve higher operating frequencies at the cost of increased power consumption.

The UCC1883 is fabricated in Unitrode's 3µM BiCMOS process. Even though the device contains internal clamping diodes on all pins, the part should still be considered static sensitive. Normal ESD handling procedures for CMOS devices should be observed when using the UCC1883.

Pin No.	Pin Name	Pin Type	Function
1	RBIAS	Analog Program	Quiescent Bias Current Set
2	CSTART	Analog Program	Soft Start and Restart Delay Timing Set
3	VLINE	Analog Input	Input Line Voltage Sense
4	IMODE	Analog Input	Input Line Polarity Sense
5	VDD	Analog Output	5V Logic Regulator
6	FB+	Digital I/O	Differential Feedback Communication Signal (+)
7	FB-	Digital I/O	Differential Feedback Communication Signal (-)
8	VCC	Power Supply	Positive Power Supply Input
9	OUT	Digital Output	Power Switch Control Voltage
10	VSS	Power Supply	UCC1883 Ground Reference
11	ISENSE	Analog Input	Primary Current Sense
12	COL	Analog Program	Output Overload Timing Set
13	CT	Analog Program	Oscillator Frequency Set
14	VLIMIT	Analog Output	Input Current Limit Control Voltage
15	IIN	Analog Program	Input Current Limit Set
16	VREG	Analog Output	9.5V Pre-regulator Control Voltage

CONNECTION DIAGRAM

DIL-16
(Top View)
J or N Package



ELECTRICAL CHARACTERISTICS Unless otherwise noted, all specifications apply for T_A = 0°C to 70°C for the UCC3883, T_A = –40°C to +85°C for the UCC2883, –55°C to +125°C for the UCC1883, VCC = 12V , VDD = 5V , RBIAS = 200kΩ, CT = 100pF, T_A=T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Section					
VCC Start Threshold		8.0	9.0	10.5	V
VCC Threshold Hysteresis		1.5	2	2.5	V
Linear Pre-Regulator Section					
Regulated VCC Voltage	(See Note 4)	8.5	9.5	10.5	V
Regulated V_{CC} to UVLO Delta		0	500	800	mV
VCC Override Threshold				11	V
User Bias Section					
RBIAS Voltage	T_J = +25°C	1.17	1.2	1.23	V
RBIAS Voltage Line Regulation	10.0V < VCC < 13.5V		8	16	mV
Total RBIAS Voltage Variation	Initial + Line + Temperature	1.15		1.25	V
Input Current Limit Section					
IIN Offset Voltage	VLIMIT = –3V	–20		20	mV
Output Reference Current	T_J = 25°C, IIN = 0V	1.6	1.9	2.1	µA
I_{REF} Line Regulation	10.0V < VCC < 13.5V		10	50	nA
Total I_{REF} Variation	Initial + Line + Temperature	1.5		2.2	µA
VLIMIT Low Level	IIN = 0.2V, |OUT| < 10nA	-10.5	–9		V
VLIMIT High Level	IIN = 0.2V, |OUT| < 10nA		0.6	1.0	V
VLIMIT Output Current	IIN = –0.2V, VLIMIT = –3V	3	6	14	mA
Oscillator Section					
Initial Accuracy	T_J = 25°C	30	35	40	kHz
Voltage Stability	10.0V < VCC < 13.5V		1	3	%
Total Oscillator Variation	Initial + Line + Temperature	29.5		41.5	kHz
CT Ramp Amplitude		2.35	2.5	2.65	V
Soft Start Section					
Soft Start Current (source)	CSTART = 2.5V	17	30	43	µA
Restart Delay Current (sink)	CSTART = 2.5V	0.5	1	2	mA
Fault Handling Section					
Overload Current Source	COL = 0.5V	1.4	2.3	3.0	µA
Overload Current Sink	COL = 0.5V	1.4	2.2	3.0	µA
Overload Fault Threshold		1.4	1.5	1.6	V
Overcurrent Threshold		1.4	1.5	1.6	V
Overcurrent Delay	(See Figure 1) (Note 6)		100	200	ns
Current Sense Section					
Peak Current Limit Threshold		1.1	1.2	1.3	V
PWM Logic and Output Section					
Minimum Duty Cycle	ISENSE = 0V			0	%
Maximum Duty Cycle	ISENSE = 1.3V	49	50	50	%
OUT Low Level	I_{OUT} = 10mA		0.05	0.15	V
	I_{OUT} = 100mA		0.5	1.5	V
OUT High Level	I_{OUT} = –10mA	11.85	11.95		V
	I_{OUT} = –100mA	10.5	11.5		V
OUT Rise Time	T_J = 25°C,C_{LOAD} = 1nF (See Figure 2)		25	75	ns
OUT Fall Time	T_J = 25°C,C_{LOAD} = 1nF (See Figure 2)		25	75	ns

ELECTRICAL CHARACTERISTICS Unless otherwise noted, all specifications apply for T_A = 0°C to 70°C for the UCC3883, T_A = –40°C to +85°C for the UCC2883, –55°C to +125°C for the UCC1883, VCC = 12V , VDD = 5V , RBIAS = 200kΩ, CT = 100pF, T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Isolation Interface Section					
FB Input High Voltage	FB = V(FB+)-V(FB-), 0 ≤ FB ≤ VDD		1.3	2.1	V
FB Input Low Voltage	FB = V(FB+)-V(FB-), 0 ≤ FB ≤ VDD	–2.1	–1.3		V
FB Input Pulse Width	(See Figure 3) (Note 6)	80	300		ns
FB Output Width	(See Figure 3) (Note 6)		75		ns
LOLINE Status Threshold		1.0	1.2	1.3	V
RSMODE Status Threshold		0.5	2	4	µA
VDD Regulator					
VDD Output	No External Load	4.6	5	5.4	V
VDD Line Regulation	1.0V < VCC < 13.5V		10	30	mV
VDD Load Regulation	–3mA < I_{OUT} < 0mA		100	300	mV
VDD Short Circuit Current Limit	VDD = 0V	7	50	80	mA
Power Supply					
DC Supply Current			200	275	µA
CDD			150		pF

Note 4: BSS129 (or equivalent) External Pass Element, 1µF Ceramic Bypass; See Figure 6.
Note 5: Operating in conjunction with UCCx885 using equal valued RBIAS.
Note 6: Guaranteed by design. Not 100% tested in production.

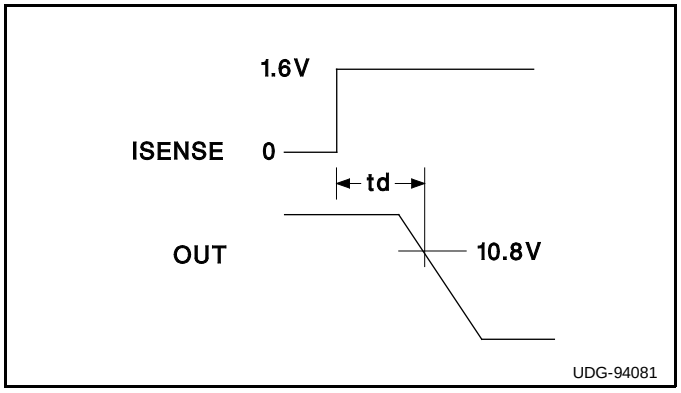


Figure 1. Overcurrent Fault Timing

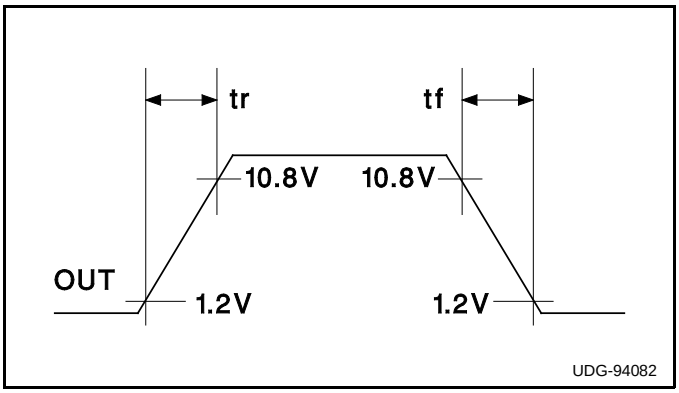


Figure 2. Output Rise & Fall Time

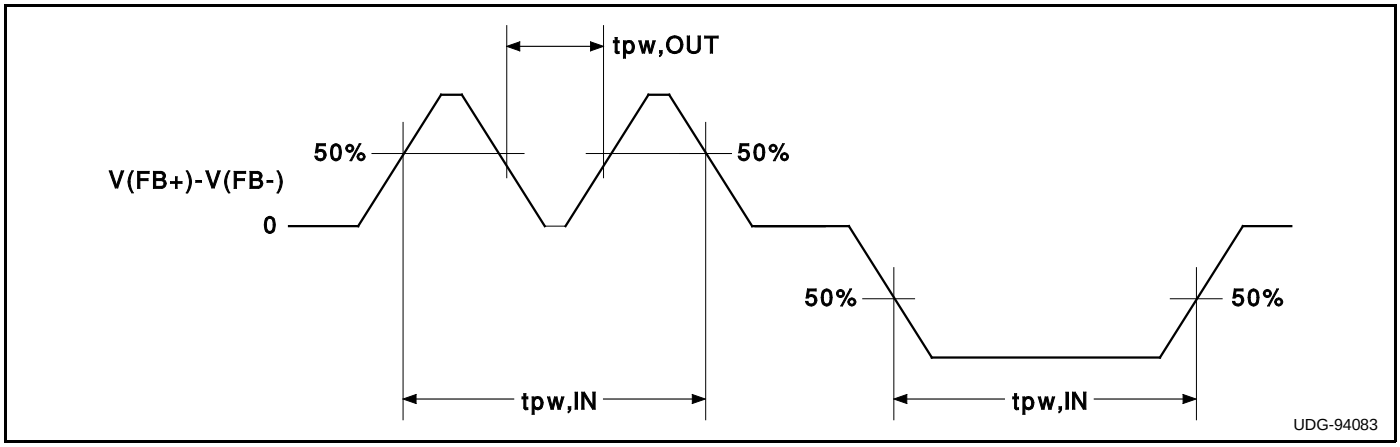


Figure 3. Isolation Interface Timing

APPLICATION INFORMATION

UNDERVOLTAGE LOCKOUT AND SOFT START

When power is first applied to the UCC1883, CSTART is held at VSS until VCC exceeds 9.0V and VDD exceeds 4.4V. During this period of UVLO, the following state exists:

1) CSTART is held low,
2) OUT is held low,
3) VREG is forced to VCC until VCC > 4V, and
4) VLIMIT becomes a high impedance output.

Once adequate operating voltages have been established, the input current limit function is enabled. CSTART and OUT are still held low until the voltage on the VLINE pin exceeds 1.2V, indicating ample voltage is stored on the converter's bulk filter capacitor. At that time, CSTART is released and allowed to charge from an internal 25µA current source. The UCC1883 then begins to transfer energy to the secondary side of the converter by pulse width modulating the ramp voltage on CT against the charging voltage on CSTART. During this soft start period, all fault functions, pulse-by-pulse current limiting, and input current limiting are enabled. Note that the dV/dt of CSTART must be strictly less than the dV/dt established on the UCC1885 SOFTREF pin, if secondary-side soft start is utilized. The UCC1883 continues the blind soft start procedure until the first set of communication pulses is received from the secondary side via the isolation interface. At that time, all control of the power switch is effectively transferred to the secondary-side regulation IC. Should communication pulses never be received, or should they be discontinued during operation, blind PWM operation continues with the output pulse width limited by the internal 50% duty cycle clamp or pulse-by-pulse current limit with all fault processing enabled.

USER BIAS PROGRAMMING

The RBIAS pin may be used to set the amount of quiescent current consumed by certain analog circuits within the UCC1883. A resistor from this pin to VSS establishes a reference current according to the equation

$$IBIAS = \frac{1.2V}{RBIAS}$$

Recommended range for RBIAS is 39.2kΩ to 392kΩ. Internal circuits on the UCC1883 consume a total quiescent current of 9 • IBIAS, plus some fixed currents amounting to about 85µA at room temperature. Additional dynamic current consumption may be calculated with C_{PD} (see specifications), given a certain oscillator frequency f_{OSC}, from the equation

$$I_{DYNAMIC} = C_{PD} \bullet V_{CC} \bullet f_{OSC}$$

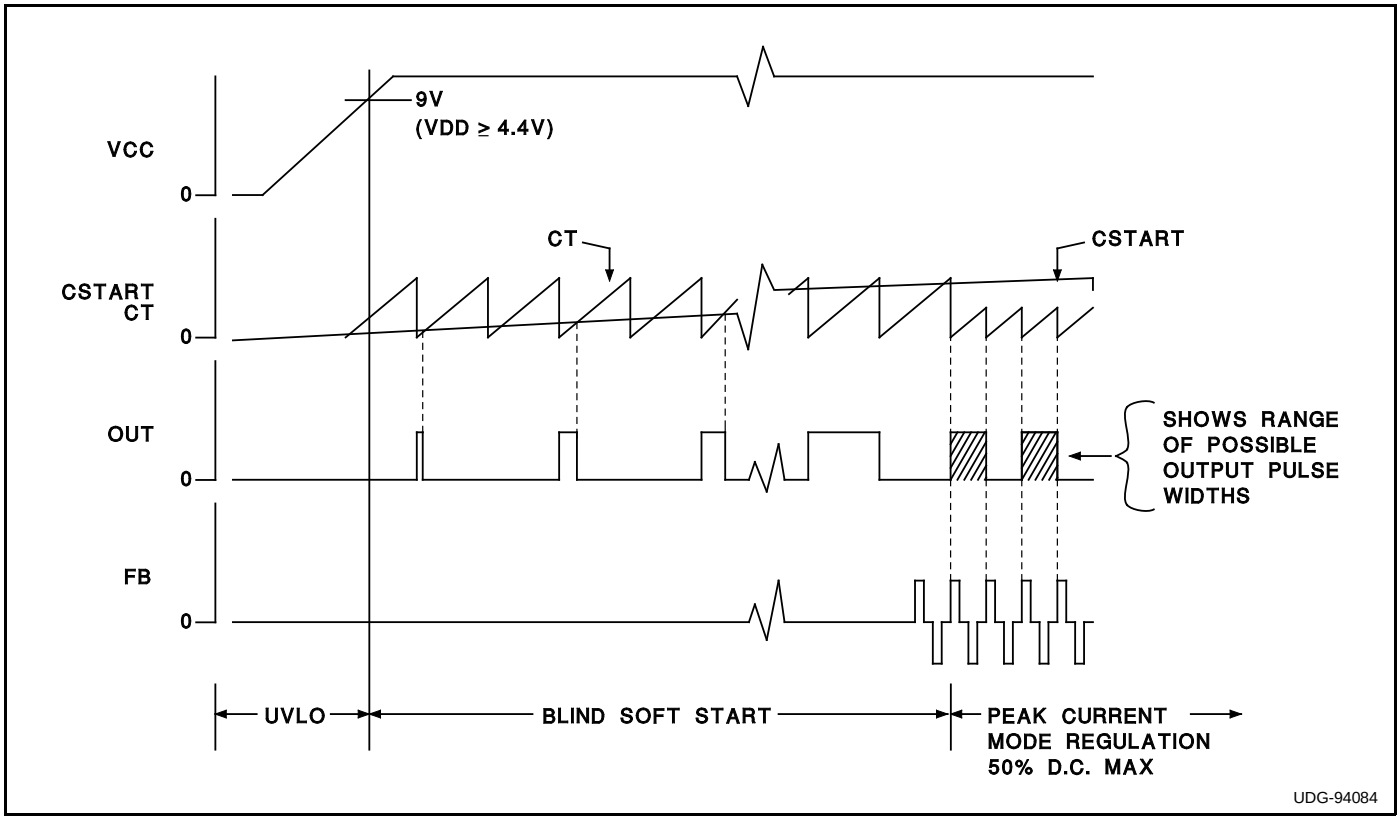


Figure 4. Start Up Waveforms

APPLICATION INFORMATION (cont.)

9.5V LINEAR PRE-REGULATOR

The UCC1883 contains a control amplifier, which when used with a depletion-mode NMOS pass transistor such as the BSS129, can provide a 9.5V linear pre-regulator to supply VCC directly from the input line. The depletion-mode device guarantees the regulator is self-starting. Bypass values less than 3.3µF are recommended when the pre-regulator is utilized. The pre-regulator may subsequently be fully disabled by a tertiary bootstrap winding providing a minimum of 10.6V to the VCC pin. Note that the UCC1883 has 2V of UVLO hysteresis to allow use of more conventional startup circuitry, if the power consumption of such implementations can be tolerated. In these cases, any value of bypass capacitance is acceptable, although a minimum value of 0.01µF is recommended for all configurations.

INPUT CURRENT LIMIT PROGRAMMING

The UCC1883 also incorporates the necessary control amplifier and current reference to implement a continuous input current limit mask conforming to CCITT recommendation I.430. When using this feature, the ratio of R_{SENSE} to R_{BIAS} determines the magnitude of the current passed by an external PMOS transistor. The PMOS device must be able to withstand the maximum input voltage seen by the converter, and its R_{ON} will cause some reduction in efficiency during normal operation, due to conduction losses. Referencing the application diagram of Figure 7, the control amplifier programs a peak input current according to the equation

$$ILIMIT = \left(\frac{RP}{RS} + 1\right) \bullet \frac{0.4}{RBIAS}$$

by driving the gate of the external PMOS device until equal voltage is impressed across RP and RS. In addition to the input capacitance of the PMOS pass device, some compensation capacitance from VLIMIT to VSS may be required. However, too much capacitance on VLIMIT will increase the inrush current response time beyond that allowed by recommendation I.430. A total capacitance of between 330pF and 2.2nF is recommended. A shunt bleeder resistor should be added across the PMOS pass transistor to facilitate converter startup. Due to the large values of resistance which will typically be encountered, a 10pF speedup capacitor across RP is suggested to help maintain good phase margin in the control loop. A clamping diode across RS improves transient response by preventing excessive error voltage from being stored on the RP speedup capacitor during VLIMIT slewing. Finally, a 12V zener clamp from VLIMIT to VSS is recommended to protect the gate of the PMOS device from over voltage and to limit the voltage slew which must occur before entering the current limit state. During normal converter operation, when less than the programmed current limit is being drawn from the line, the control loop opens and VLIMIT moves to its maximum negative value, effectively turning the PMOS limit transistor into a series switch.

If a more accurate reference than that supplied by the UCC1883 is desired, a precision resistor may be wired from an appropriate reference voltage to IIN. Since IIN is

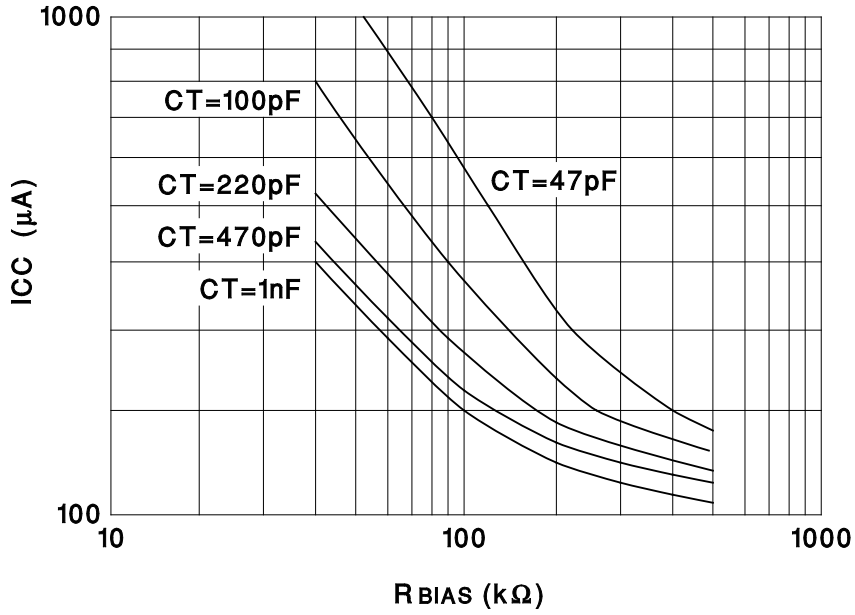


Figure 5. Average DC Current vs. RBIAS (VCC = 12V) Not Including Power Switch Gate Current.

APPLICATION INFORMATION (cont.)

held at VSS (ground) by the current limit control amplifier, the additional current created in this case is equal to the reference voltage divided by the external resistor. A reference of at least 2V is recommended to eliminate errors caused by the input offset voltage of the control amplifier. Because the reference current provided by the UCC1883 sums into the IIN pin a minimum external reference current value of 4V/RBIAS is recommended to minimize errors caused by the initial tolerance of the internal current reference.

FAULT HANDLING

Three fault conditions which immediately disable the output are detected by the UCC1883 housekeeping circuitry. These are:

1) UVLO,
2) 1.5V or higher on the ISENSE pin, and
3) 1.5V or higher on the COL integrator pin.

Unlike the pulse-by-pulse current limit comparator, no leading blanking is applied to the overcurrent fault comparator, which has a nominal 1.5V threshold. A capacitor to VSS may be used on the COL pin to program the output overload fault integrator. The polarity of the 2.2µA current sourced by the internal circuitry driving the COL pin potentially changes on each falling edge of OUT. If the output pulse was terminated as the result of a peak current event, then current is sourced to COL, otherwise current is sunk from COL to VSS. If the voltage on COL ever reaches 1.5V, a fault condition is set.

If any fault condition is detected once UVLO has ended, the fault is latched and a restart delay elapses before a soft start is attempted. This delay is normally controlled by an internal 1µA discharge of the CSTART pin from VDD to 0.2V. If a fault occurs during soft start, the output is immediately disabled, but CSTART is fully charged (4.8V) before a restart delay begins. A fixed restart delay to soft start timing ratio of 25:1 may be obtained with only a capacitor from CSTART to VSS. This ratio may be decreased by adding an external resistor between CSTART and VSS. The value of this resistor should be greater than the value of the current programming resistor on the RBIAS pin.

ISOLATION INTERFACE

In addition to receiving synchronization and duty cycle control information from the secondary side of the converter, the UCC1883 isolation interface also transmits digital status information to the secondary side. This digital information reflects the state of two internal analog comparators which monitor the VLINE and IMODE pins. A voltage of less than 1.2V on VLINE is indicated by a true LOLINE bit, and an input current of less than 2µA into the IMODE pin is interpreted as a true RSMODE (restricted power mode) condition. These digital bits are transmitted across the isolation barrier and appear as outputs on the UCC1885 secondary-side regulation IC. Recall that no UCC1885 output will occur until a voltage greater than 1.2V is initially established on VLINE.

VDD LOGIC SUPPLY

The internal CMOS logic on the UCC1883 runs from a regulated 5V which is available externally at the VDD pin. This pin should be bypassed to VSS with a high quality ceramic capacitor having a value of at least 0.01µF. Values in excess of 10µF are not recommended.

OSCILLATOR

A timing capacitor is connected between CT and VSS to program a natural oscillator frequency according to the equation

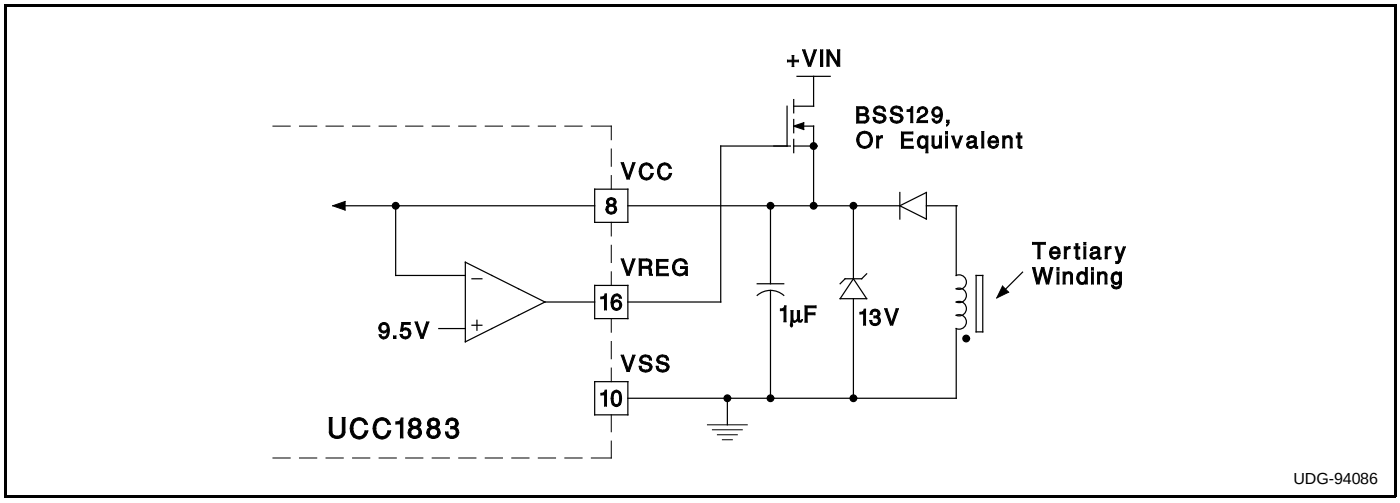


Figure 6. 9.5V Pre-regulator Application

APPLICATION INFORMATION (cont.)

$$f_{OSC} = \frac{0.72}{CT \bullet RBIAS}$$

A ramp voltage running from VSS to 2.5V is created on the CT pin. This oscillator is automatically synchronized to the secondary-side clock frequency when data communication occurs across the isolation interface. Proper synchronization will only occur if the frequency of the secondary-side clock exceeds the natural frequency of the UCC1883 oscillator. A new oscillator cycle (ramp returns to VSS) will be initiated on the rising edge of each positive isolation interface input pulse, with a corresponding decrease in ramp amplitude. The UCC1883 is designed so that the dV/dt established on its CT pin will be nominally the same as that of the UCC1885 CT pin, if equivalent components are used on the RBIAS and CT pins of both devices. However, the natural frequency of the UCC1883 oscillator will automatically be lower, to allow synchronization. Proper CT ramp slope is important to the UCC1883, because it uses this information, along with the pulses received over the isolation interface, to reconstruct the analog output of the UCC1885 voltage error amplifier. This reconstructed voltage is in turn used to control the peak current mode PWM. The ratio of the slope of the UCC1883 timing ramp to the UCC1885 timing ramp sets the gain applied by the UCC1883 to the UCC1885 error amplifier output.

Other variations of the UCC1883 implementing voltage mode control, duty cycles greater than 50%, or faster natural oscillator frequencies may be available. Contact the factory for further information.

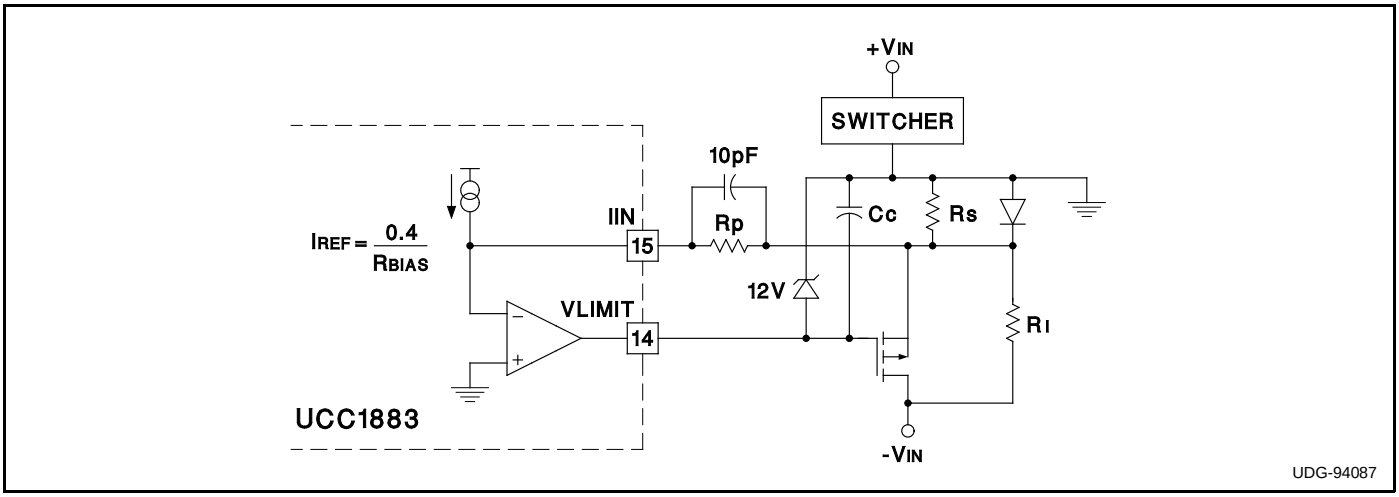


Figure 7. Input Current Limit Application

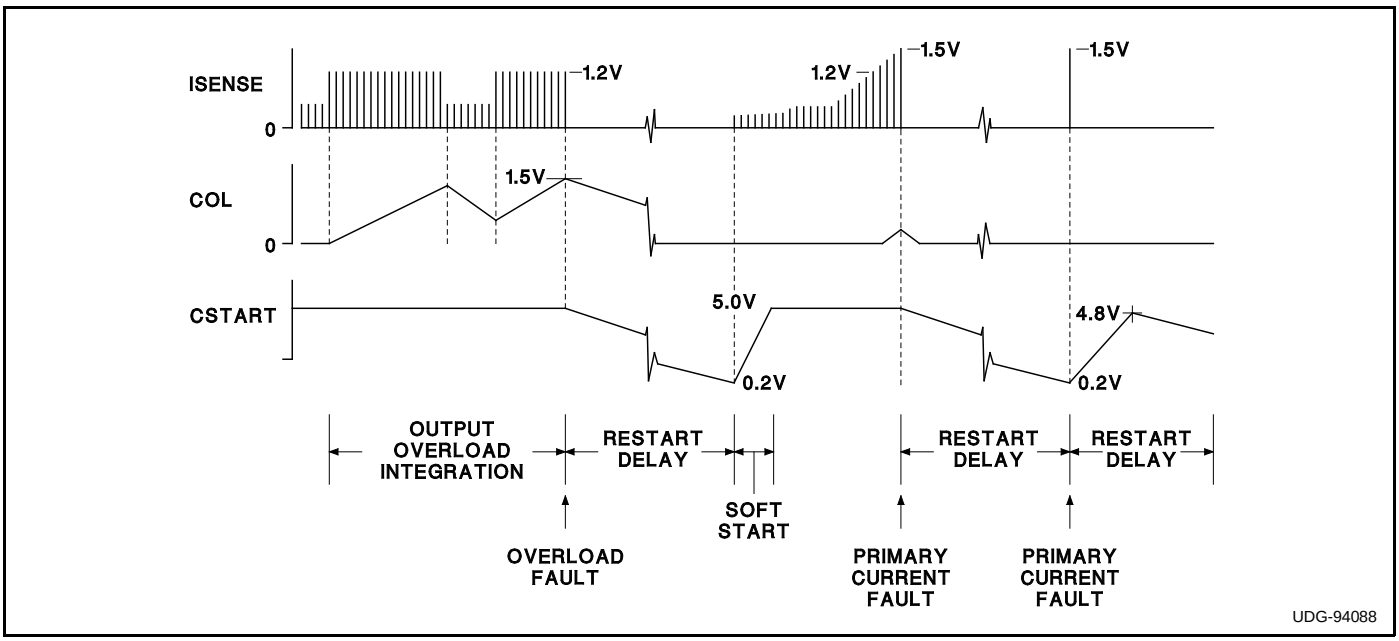


Figure 8. Fault Waveforms

APPLICATION INFORMATION (cont.)

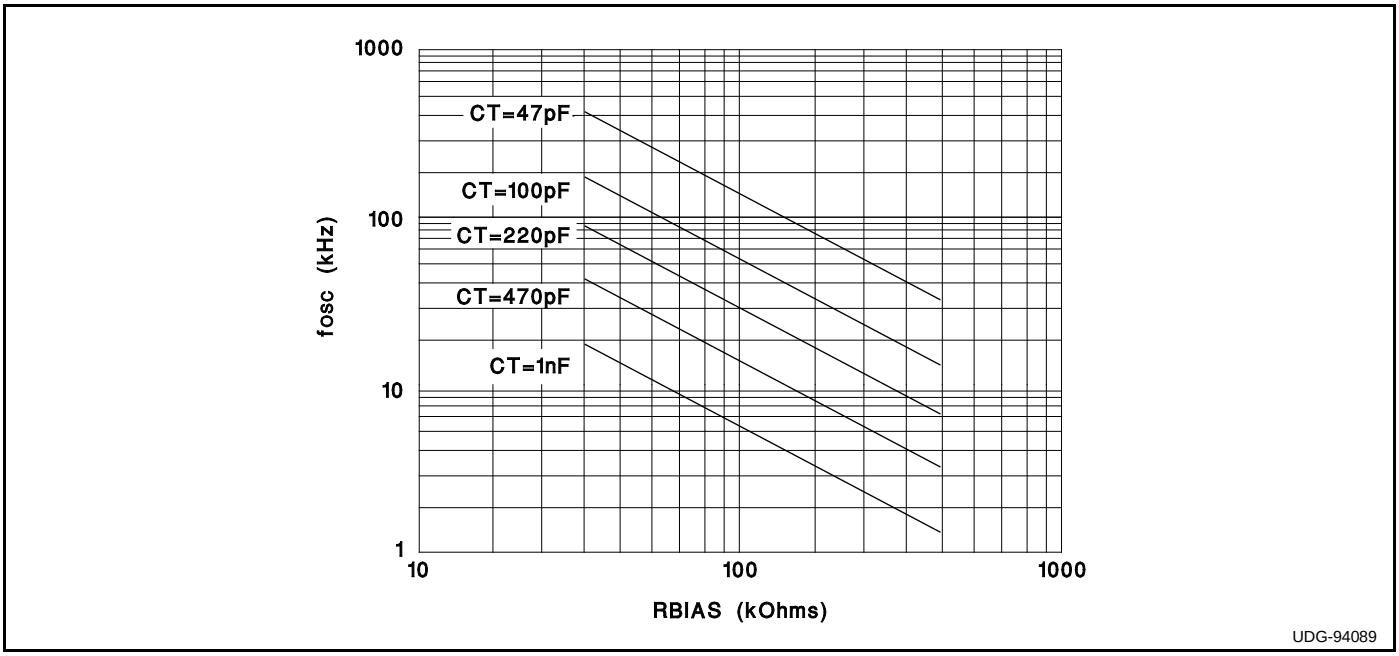


Figure 9. Oscillator Frequency Versus RBIAS

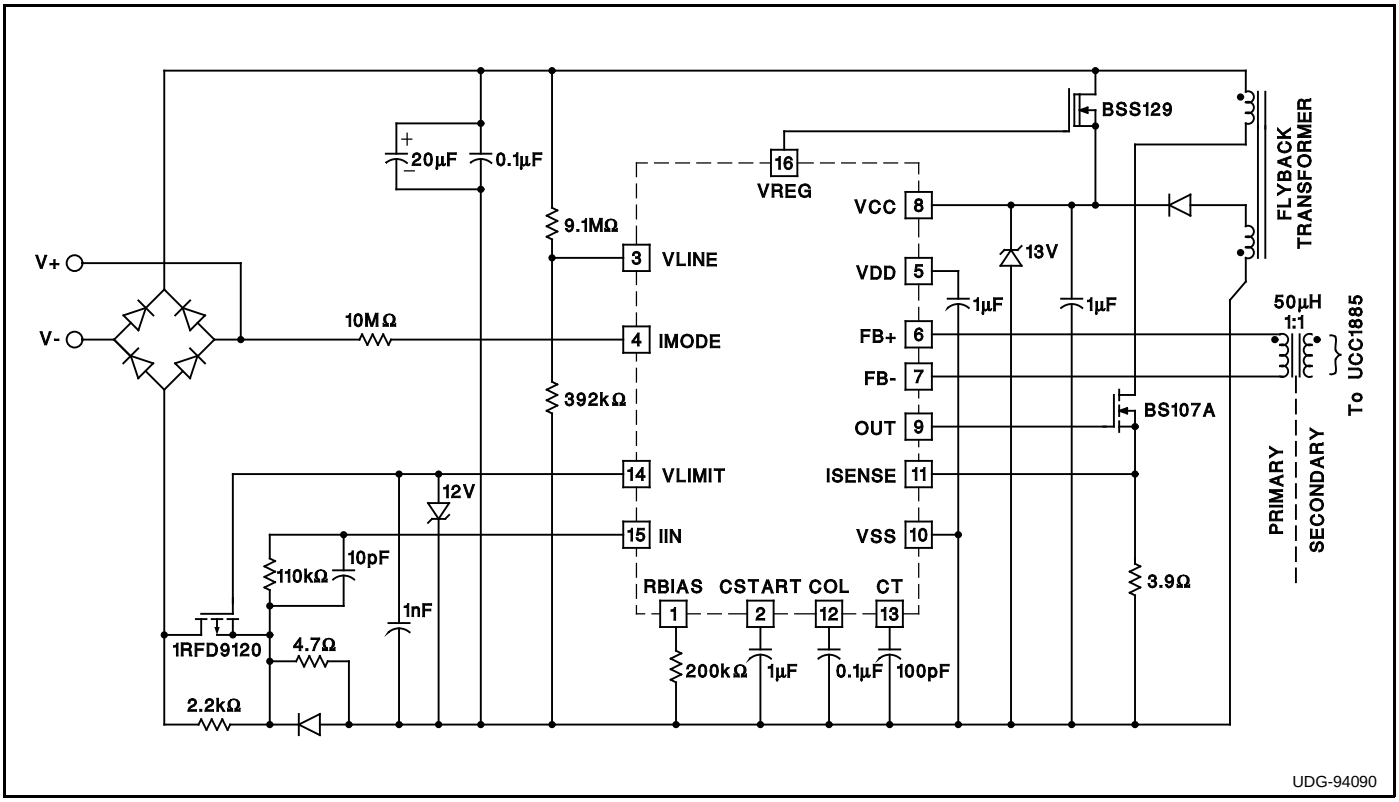


Figure 10. Typical Application Circuit

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