VISHAY.

P-Channel 200-V (D-S) MOSFET
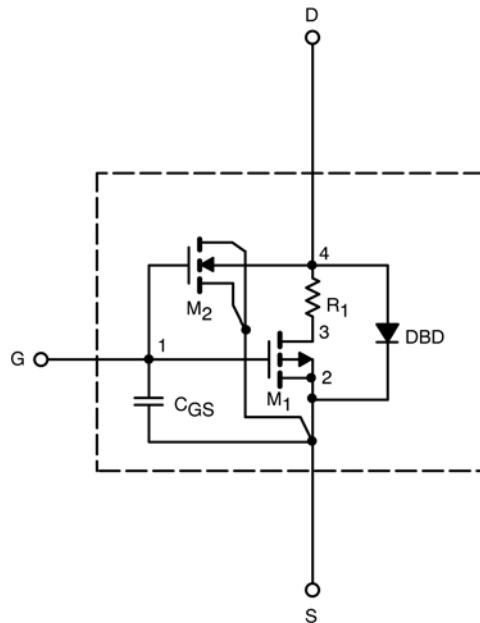
CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

| Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250$ μA	3.1		V
On-State Drain Current [a]	$I_{D(on)}$	$V_{DS} = -5$ V, $V_{GS} = -10$ V	1.3		A
Drain-Source On-State Resistance [a]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -0.4$ A	3.95	3.98	Ω
		$V_{GS} = -6$ V, $I_D = -0.4$ A	4.08	4.06	
Forward Transconductance [a]	g_{fs}	$V_{DS} = -10$ V, $I_D = -0.4$ A	0.5	1	S
Diode Forward Voltage [a]	V_{SD}	$I_S = -0.4$ A, $V_{GS} = 0$ V	−0.72	−0.80	V
Dynamic [b]					
Total Gate Charge	Q_g	$V_{DS} = -100$ V, $V_{GS} = -10$ V, $I_D = -0.4$ A	3.6	4.1	nC
Gate-Source Charge	Q_{gs}		0.8	0.8	
Gate-Drain Charge	Q_{gd}		1.3	1.3	

Notes
a. Pulse test; pulse width $\leq$ 300 μs, duty cycle $\leq$ 2%.
b. Guaranteed by design, not subject to production testing.

COMPARISON OF MODEL WITH MEASURED DATA (T$_J$=25°C UNLESS OTHERWISE NOTED)
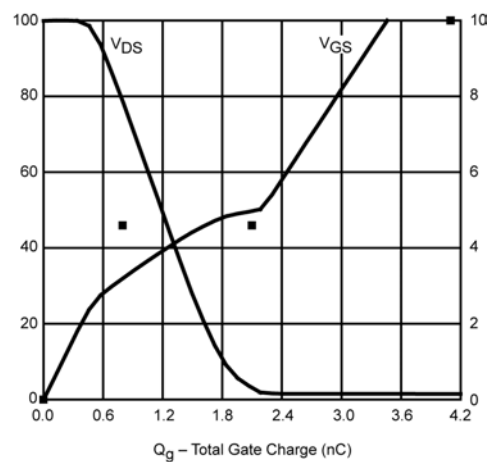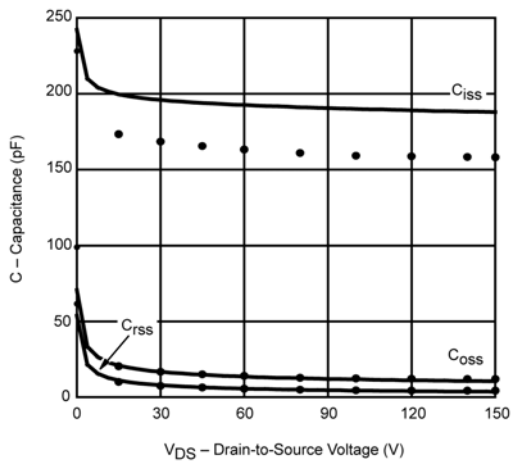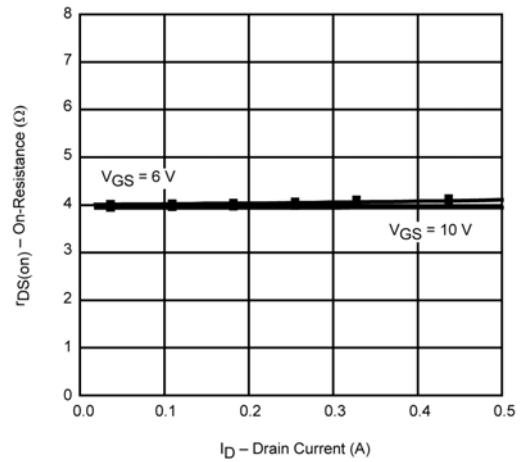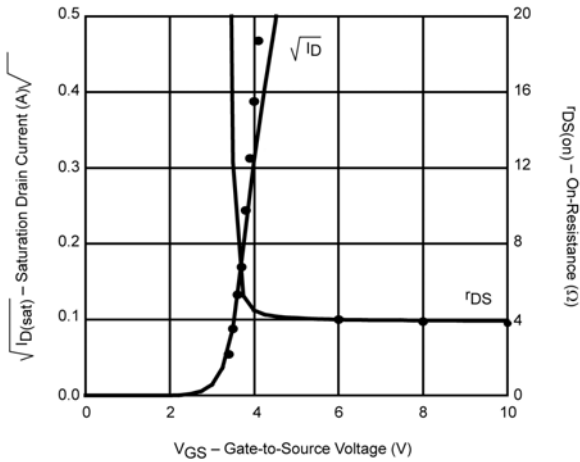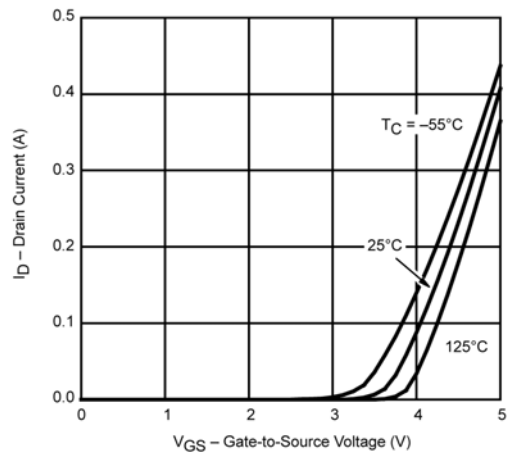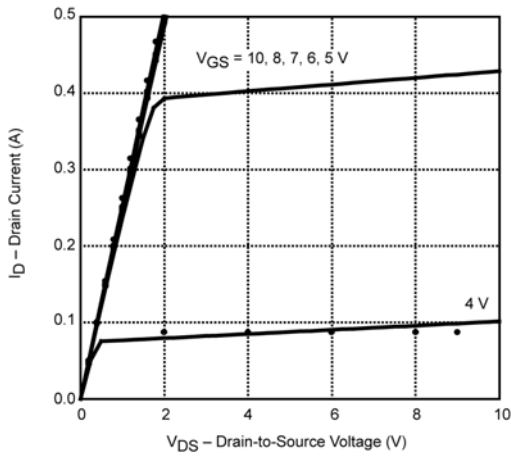
Note: Dots and squares represent measured data.