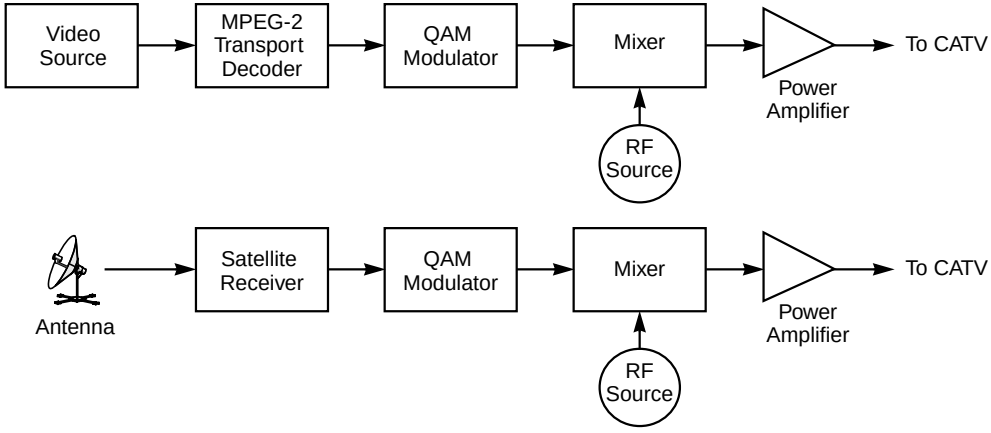
L64777
DVB QAM Modulator
Datasheet

The L64777 chip implements a QAM modulator that is digital video broadcasting (DVB)-compliant, as described in document ETS 300 429. The input is an MPEG-2 system layer-compliant transport stream either in parallel byte-wide or serial format. The chip contains digital signal processing functions, digital-to-analog converters, and sampling clock circuitry that generates a quadrature amplitude modulation (QAM)-modulated output signal in baseband. Users can configure the device by means of its serial interface.

Figure 1 shows a block diagram of a typical CATV transmitter using the L64777 DVB QAM Modulator.

Figure 1 CATV Transmitter Block Diagram with L64777



Introduction

The L64777 chip design is based on the existing LSI Logic L64767 device and includes the following major enhancements:

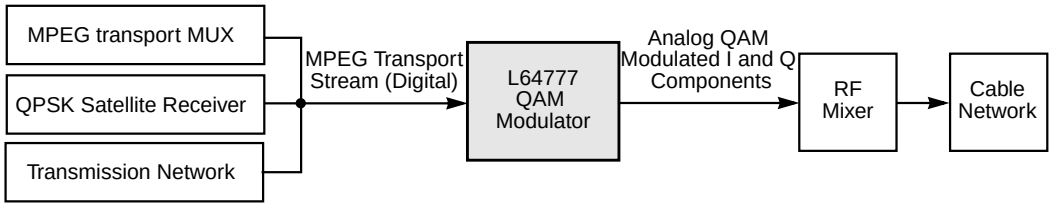
- Two internal digital-to-analog converters generate in-phase and quadrature (I and Q) baseband signals.

- An on-chip voltage-controlled oscillator improves the symbol rate PLL to support most frequently used application ranges.
- A serial interface replaces the eight-bit microprocessor interface.
- A digital numerically controlled oscillator (NCO) and interpolation mode support operation with the L64724 device.

The modulator is intended to follow either an MPEG transport stream source (for example, a transport multiplexer) or a satellite receiver, such as the LSI Logic L64724 (see Figure 2). It processes MPEG-2 system-compliant frames at the input.

You can program the sync word and block length, and the chip can reinsert the sync information. The device handles the MPEG-specific transport-packet error indication (TEI) bit internally.

Figure 2 L64777 Operating Environment



Features and Benefits

The following is a partial list of features and benefits of the L64777.

- DVB standard ETS 300 429-compliant modulation operation
- Highly integrated global synchronization and clock control
- On-chip VCO to support symbol rates up to 10 Msymbols/s
- Digital NCO and interpolation mode to support operation with the L64724
- Four-fold Nyquist filter oversampling
- Maskable interrupts for all error conditions
- Individual module bypass configuration modes
- I and Q baseband outputs both in digital and analog formats

- I^2C-compatible serial interface for control, setup, and monitoring of various chip parameters
- User-controllable input synchronization schemes
- 16, 32, 64, 128, and 256 QAM modes
- Reed-Solomon encoder
- Frame sync byte reinsertion
- Input jitter handling and Reed-Solomon gap insertion by a 128-word circular FIFO buffer
- IEEE 1149.1 JTAG interface for testing
- Up to 10 Mbytes/s parallel data input
- Up to 60 Mbits/s serial data input
- Up to 11.25 Mbaud operation in NCO mode of operation
- Easy interface to most input sources
- 85 ˚C ambient operation without special cooling devices
- Unconstrained serial mode to allow modulation of non-MPEG data stream

Architectural Overview

The L64777 implements the modulator processing chain defined in ETS 300 429. This processing chain is illustrated in Figure 3.

Figure 3 ETS 300 429-Compliant Modulation Operation

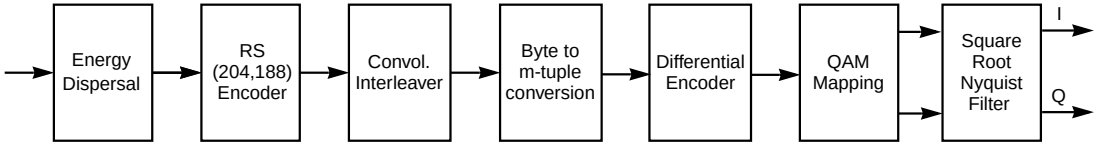
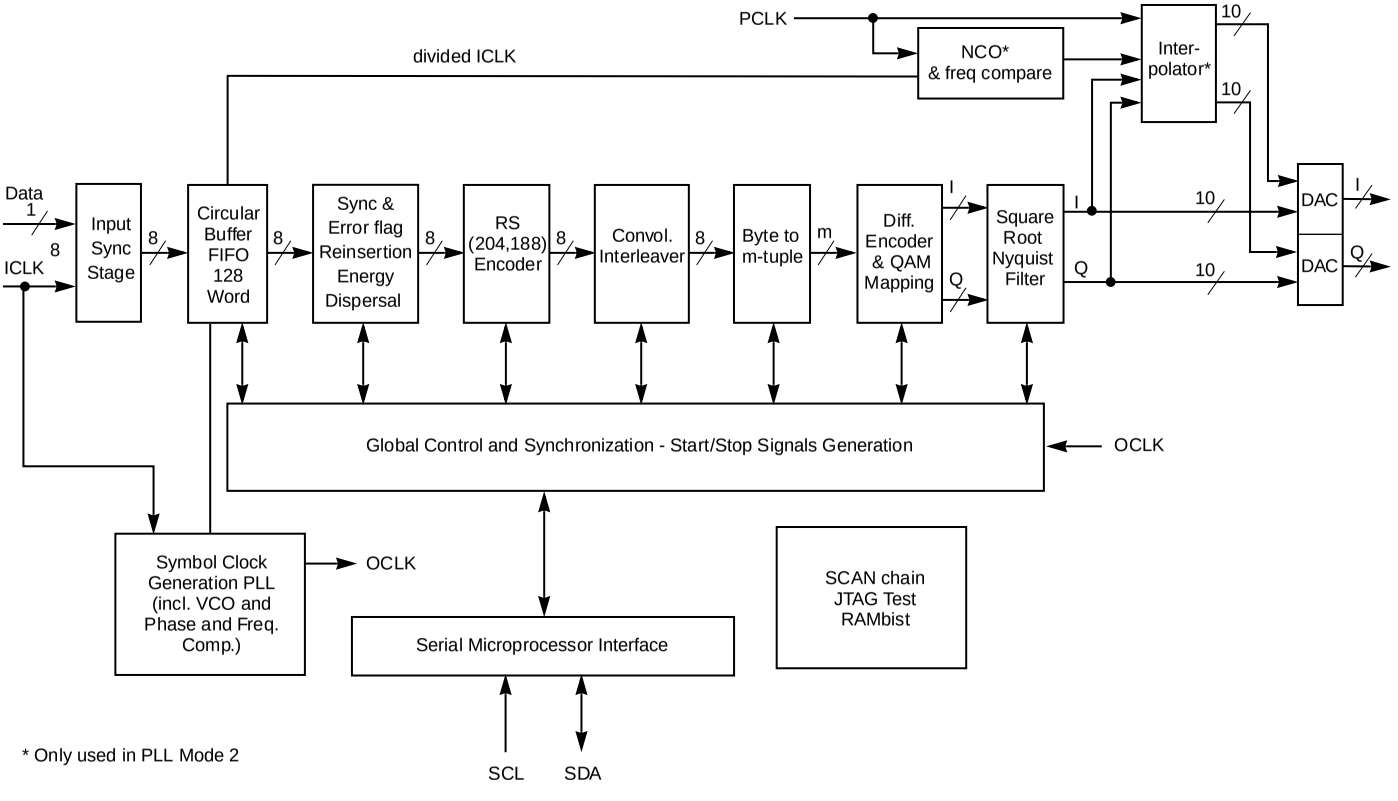


Figure 4 is a block diagram of the L64777 architecture. The input clock drives only the input synchronizing stage. The OCLK, which is four times the QAM symbol rate, is the base of all residual processing.

A numerically controlled oscillator (NCO) module allows the L64777 to interface with the LSI Logic L64724. In this case, the chip must receive the L64724 PCLK clock; thus, the byte_clock output from the L64724 must be applied to ICLK. This assumes the PCLK has generated the byte clock.

The QAM mapping supports 16, 32, 64, 128, and 256 QAM. The input to the device is an MPEG-2 compliant transport stream; its output consists of baseband QAM signals in I and Q.

Figure 4 Data Path



PLL Modes

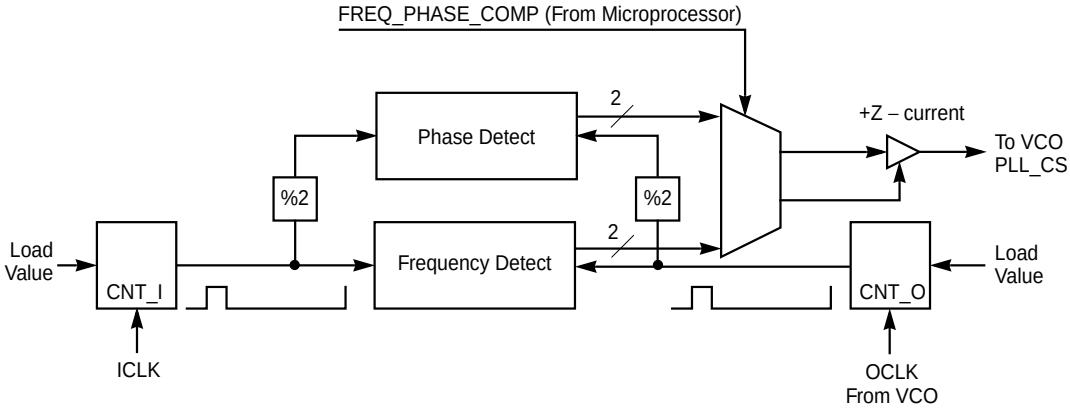
Connecting the L64777 to a satellite receiver and the LSI Logic satellite decoder chipset requires the PLL circuits to lock the input and output clocks. Two modes can achieve this:

- **Mode 1** uses the phase/frequency detector and the dividers of the L64777 to accept an external VCO.
- **Mode 2** connects the PCLK output of the L64724 or the L64734 to the L64777 PCLK clock input, and connects the byte clock output to the ICLK input of the L64777. This is also called the Numerically Controlled Oscillator (NCO) mode of operation. This mode is dedicated to the connection of the L64724.

PLL Mode 1

Figure 5 shows the phase and frequency detection for an external voltage-controlled oscillator (VCO) loop. Choose between frequency and phase detection through the microprocessor interface.

Figure 5 Phase and Frequency Detection with an External VCO



Prescalers (CNT_I) and a divider (CNT_O) in the feedback loop of the PLL generate the internal operating clock (OCLK). Program the 15-bit prescalers through the microprocessor interface, selecting values for CNT_I and CNT_O that minimize CNT_O and reach the required ratio.

PLL Mode 2

In Mode 2, the PCLK input provides an external clock. The L64777 uses the internal NCO to lock to the transport byte clock, provided at ICLK. The chip generates an OCLK internally. Select PCLK to be at least twice the frequency of the internal OCLK.

Consecutive sync blocks can have any gap length between them. Thus, the L64777 can convert an input block to a block with a gap for RS insertion, as long as the size of the 128-byte circular input buffer is sufficient to insert RS gaps and to cope with possible PLL jitter. For an encoder with 16-parity RS insertion, the L64777 selects the size of the circular input buffer with sufficient margin.

When operating on public synchronous networks (such as the synchronous digital hierarchy, SDH, or plesiochronous digital hierarchy, PDH), the system designer must consider possible jitter on the input network. The design of the L64777 permits short-term deviations of input-to-output frequency of $\pm$ 56 bytes before a FIFO overrun condition occurs. This is sufficient for operations on SDH or PDH networks.

On ATM networks, you must prebuffer input data to get a continuous frame rate at the chip input. If high input jitter occurs over an ATM without a prebuffer, the whole PLL regulation of the input-to-output frame rate fails. You must design the size of the prebuffer according to the maximum jitter expected over the asynchronous transfer mode (ATM) network.

I/O

The following subsections describe the input and output of the L64777.

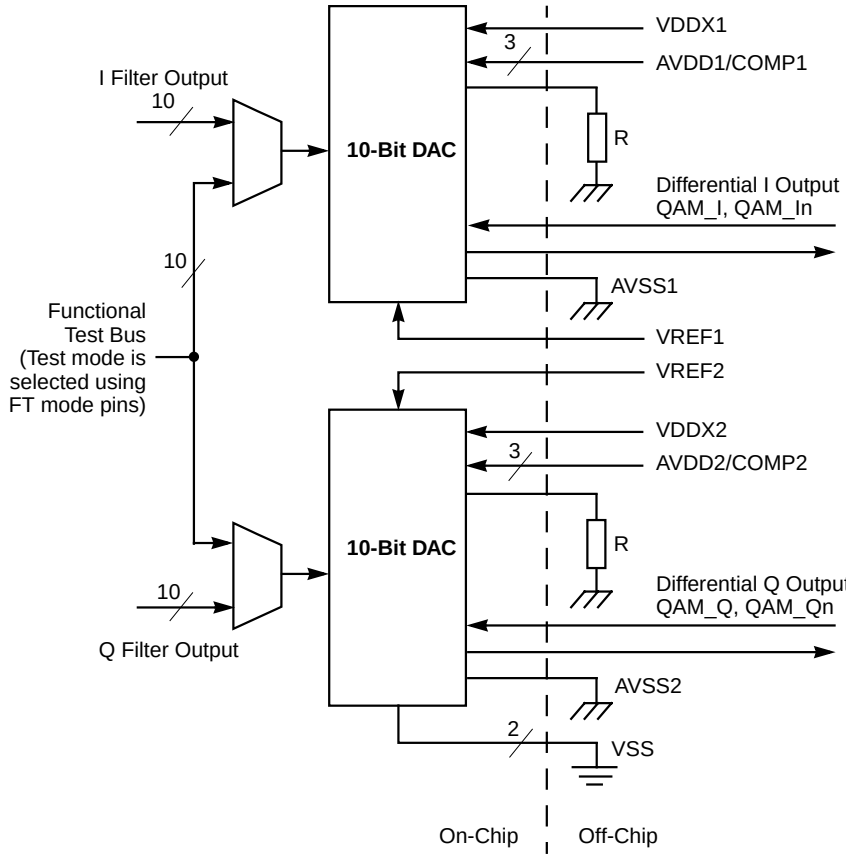
Input

The QAM Modulator accepts serial input data at a maximum 54 MHz clock frequency on the ICLK pin. In Byte-Parallel Input mode (Parallel mode), the maximum frequency on ICLK is 10 MHz.

Output Signals

The L64777 outputs the I and Q components of its signal on two separate analog output interfaces. The output interface contains two internal 10-bit digital-to-analog converters (see Figure 6).

Figure 6 Analog I/Q Output Interface Diagram



The differential outputs terminate externally (the external components must provide termination to both differential lines, and the DAC achieves maximum linearity in differential mode).

The L64777 I and Q component outputs are available in 10-bit digital format. The related clock depends on the PLL mode: OCLK is used in Mode 1; PCLK is used in Mode 2. The output format can be programmed either as a two's complement, or as a sign magnitude representation.

The analog I- and Q-modulated output signals are at a sampling rate of OCLK, which is four times the QAM symbol rate. The input to the digital-to-analog conversion is available also in a digital format at the DIG_I and DIG_Q bus pins.

Control Interface

An external CPU uses the L64777 serial control interface to control and setup the programmable parameters of the chip. This interface is a slave type only, connected to the same serial bus as the LSI Logic L64724.

Serial Microprocessor Interface

A bidirectional microprocessor interface allows write and confidence read-back of internal registers. No interaction during operation is required with the microprocessor, but all registers must be configured after a RESET to guarantee proper operation of the device. A default setup that requires no microprocessor download is built in for 64 QAM.

Input Synchronization

The L64777 transport interface reads the data stream from the transport source, identifies the position of the synchronization bytes, and strips off invalid data. The transport interface can operate in either Parallel or Serial mode.

The L64777 can synchronize the transport interface in two ways. In both modes, it works synchronously with ICLK and reads all signals, including input data, on the raising edge of ICLK.

- In **external synchronization** mode, the transport interface specifies the position of the external sync byte by asserting FSTARTIN HIGH during sync byte input. In serial mode, the interface must assert the signal HIGH during the first bit (MSB) of the input stream.
- In **internal synchronization** mode, the L64777 does not require a block start indication and finds the position of the programmed sync byte automatically.

Sync Acquisition Phase

In the sync acquisition phase, the number of sync detections required for sync and loss is programmable from 3 to 5. TS is the designation for the number of track steps. After TS error-free consecutive detections of the sync byte S at the correct locations, the L64777 declares synchronization; if a mismatch occurs, it goes back to the search state.

Validating the detection of the sync word three times ensures a probability of false alarm equal to $P_{fa} = (2^{-8})^3 = 6*10^{-8}$. Validating the detection of the sync word five times insures a probability of false alarm equal to $P_{fa} = (2^{-8})^5 = 9*10^{-13}$.

Sync Tracking Phase

The sync tracking phase checks the detection of S at the correct location (i.e., every P bytes). TS – 1 mismatches are tolerated, but at the last mismatch the L64777 declares a loss-of-sync and goes back to state S0 to look for new synchronization.

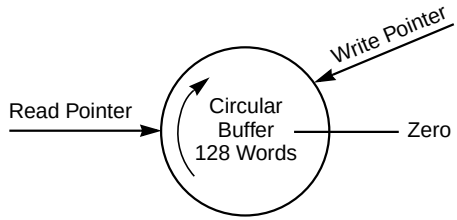
FIFO Clock Conversion

The L64777 uses a dual-ported RAM to implement the circular buffer FIFO function. The circular buffer has a write pointer driven by ICLK and a read pointer driven by the Symbol clock, OCLK/4. The device does not prevent collisions of the pointers; rather, the PLL-VCO follow-up time and proper initial setup of the pointer distance must guarantee this.

For FIFO initialization, the L64777 loads a user-programmable pointer distance of 0 to 127 cycles (the FIFO delay value of Register 2 in Group 2) into the read address pointer (after each microprocessor delay register access) and sets the write address pointer to zero (see Figure 7). After this initialization, both pointers run free, and the OCLK to ICLK frequency relationship determines how the read and write pointers advance.

To allow outside watching of the asynchronous pointers, an alarm comparator indicates when both pointers are equal. Because both counters are Gray Code counters (in which changes occur only in one bit) the spikes and glitches of the asynchronous signals are minimized.

Figure 7 FIFO Pointer Concept



When specifying the microprocessor download value for the read pointer initialization, you must use Gray Code. The write pointer also is Gray Code counter-driven; it initializes to zero when the read counter is loaded.

Properly programmed delay values in Gray Code guarantee that the read pointer is directly opposite the write pointer most of the time; this increases system immunity against PLL frequency swings, which might occur during the phases of an unstable input signal. Smaller distances also can reduce system delay.

Sync/EF Reinsertion Unit

The following subsections describe the Sync/EF modes, error flag insertion, and scrambler.

Sync Insertion Mode

The Sync/EF unit inserts new sync words if that mode is programmed. Sync insertion can be useful to work against bit errors in sync bytes, even if sync is already inserted in the stream. If the bitstream contains sync bytes that the device uses for synchronization, the regenerated sync bytes conceal single errors in the synchronization pattern.

Error Flag Insertion

The next processing task is the error flag handling for MPEG-2 transport packets. If ERRORIN indicates a decoder error at the first byte of a frame, the L64777 sets the TRANSPORT_ERROR_INDICATOR bit of the MPEG-2 packet. This is the MSB of the second byte in a packet. If there is no error indication, the L64777 passes the TRANSPORT_ERROR_INDICATOR bit transparently.

Energy Dispersal (Scrambler) Unit

The function of the Scrambler is specified for the serial domain by the *Digital Broadcasting Systems for Television Sound and Data Services: Framing Structure, Channel Coding and Modulation Cable Systems*. The energy dispersal module (scrambler) operates in Parallel mode based on the algorithm of the serial domain.

The scrambler block consists of two major modules: one to generate a pseudo-random binary sequence (PRBS) that modifies the incoming data stream, and the other a control module that properly aligns data with the PRBS.

Reed-Solomon Encoder

Reed-Solomon (RS) error correction codes are systematic and operate on bytes rather than single-bit data streams. The codes are expressed by convention as two numbers, the first indicating the total code word length (N), and the second indicating the number of message bytes (K). The difference between these two numbers (N – K) is the number of check bytes.

The error-correcting power of an RS code is related to the number of redundant check symbols in its code words. In general, an RS code with 2t check symbols per code word can correct up to “t” byte errors per code word. Higher redundancy allows more errors to be corrected.

Forward Error Correction (FEC)

FEC requires an encoder that appends redundant check information to the message before transmission. The bytes with an indeterminate number of bits are referred to as symbols. The message symbols and following redundant check symbols make up code words. The check symbols are redundant because they are derived from the message and are appended to the message. Check symbols are also referred to as “redundant check bytes,” and sometimes as “correction bytes.”

A large number of check symbols allows the decoder to correct a large number of transmission errors. The redundant check symbols in a message allow a decoder at the receiving end of a transmission line to detect transmission errors and reconstruct the original message content.

After generating a code word, the encoder transmits it to a decoder. The decoder compares the bitstream in the message data to the encoding in the check bytes to detect transmission errors. The L64777 can reconstruct the original message precisely from the check symbols, as long as the code word has no more than $\lfloor (R)/2 \rfloor$ byte errors, where R = the number of redundant check bytes.

Error Handling and Correction

A bit error occurs when a transmitted 0 is received as a 1, or vice versa. A byte error occurs when one or more bits in the byte have errors. For example, a byte with only one bit error is counted as one byte error, and a byte with m bit errors (all bits are inverted) is also counted as 1 byte error. As long as a code word has no more than t = $\lfloor (R)/2 \rfloor$ byte errors, the RS decoder corrects all errors.

To achieve RS encoding at the lowest possible gate count and power consumption, the check byte parameters of the RS encoder in the L64777 are fixed to R = 16, according to the DVB standard. When the RS encoder is switched off, data feeds through without check-word insertion at an internal delay of two clock cycles.

Convolutional Interleaver

The convolutional interleaver rearranges the ordering of a sequence of symbols in a deterministic manner. A (B, N) periodic interleaver has the following characteristics:

- The minimum separation at the interleaver output is B symbols for any two symbols that are separated by less than N symbols at the interleaver input.
- Any burst of b < B errors inserted by the channel results in single errors at the deinterleaver output.

The scheme is also referred to as a convolutional interleaver/ deinterleaver (based on the Forney approach).

The L64777 interleaver performs periodic interleaving with two fixed parameters: B, the desired interleaving depth, and M, defined as:

$$M = \left\lceil \frac{N}{B} \right\rceil$$

The values of the interleaver in the L64777 are: N = 204, B = 12, and M = 17. You can switch off the interleaver. It is fully transparent with an intrinsic delay of three clock cycles.

The main modules are a set of configured RAM-based delay lines to implement the proper delay for individual data bytes, and a controller to handle and generate the strobes needed by subsequent modules in the data path.

Bytes to M-tuples Converter

This unit cuts down bytes to slices of m = 1, 2, 3, 4, 5, 6, 7, and 8 bits. The programming parameter, mSize, must be set to m – 1. The order is the MSB of the oldest byte first. See the *Digital Broadcasting Systems for Television Sound and Data Services: Framing Structure, Channel Coding and Modulation Cable Systems* for a detailed specification. When cutting six-bit symbols, it cuts three bytes into four symbols. The case of four-bit symbols is trivial (eight bits are split into two sets of four bits each).

Differential Encoder and QAM mapping

This block performs differential encoding and mapping for 16 and 64 QAM, as specified in the *Digital Broadcasting Systems for Television Sound and Data Services: Framing Structure, Channel Coding and Modulation Cable Systems*, the baseline document, and its extensions. The QAM 256 mapping is taken from the DVB document 1190.

The encoder performs differential encoding on the two most significant bits of each symbol.

Square Root Nyquist Filter

This pulse-shaper module implements a programmable square-root raised cosine filtering function with a default of 15% roll-off factor. The precision of the internal Nyquist filter computations, and the width of the output data bus, are sufficient for QAM modulations up to 256. The filter operates at four times the oversampling rate.

Each of the two I and Q branches has one filter, realized as polyphase structures. Each filter consists of four filter branches, which compute 1-phase filter results at the symbol rate. Thus, the L64777 Nyquist filter

module generates the desired pulse shape by combining the outputs of four identical filter branches for I and Q.

For an oversampling factor of four, the filter executes the above sequence at four times the symbol rate (60 MHz in PLL mode).

Global Control and PLL Module

The L64777 interface supports serial and parallel input modes at the input interface. The global control generates the clocking for the input and output interfaces; it also controls the data path. It contains all the necessary logic to chain the processing units together.

The global control manages the output data stream so that it is continuous (no gaps between the symbols), assuming that the incoming data rate is constant (on average). To achieve this, a PLL must derive the output clock OCLK from the input transport stream rate.

The PLL module consists of two independent clock dividers for ICLK and OCLK. The dividers are 15-bit binary counters that have a count sequence length that is programmable.

The default values written by the external microprocessor are: OCLK divider = 32, ICLK divider = 6 for 64 QAM.

Interpolator

In PLL Mode 2, the interpolator retimes the output samples that the Nyquist filter calculated. The interpolator is clocked with PCLK and generates the output samples in the PCLK sampling grid. The interpolator takes the required retiming information from the NCO.

PCLK is at least twice the frequency of the original OCLK obtained by the formula for PLL Modes 1 and 2. The square root raised cosine filter also compensates for the sin(x)/x frequency characteristic of the digital-to-analog converter with the faster sampling grid.

Serial Microprocessor Interface

The external microprocessor controls the QAM mode of operation, 16 to 256 QAM. It also controls the mode of input synchronization (that is, whether to lock synchronization to sync bytes or input pulses). The

microprocessor interface downloads the filter coefficients and the delay value for proper FIFO initialization.

The microprocessor interface uses an I^2C-compatible serial control protocol. The interface is slave-only and can not be a master to the serial bus. The base address of the component is composed of a fixed five-bit address and two selectable bits, which are fed through SB_BASE[1:0].

Test Unit

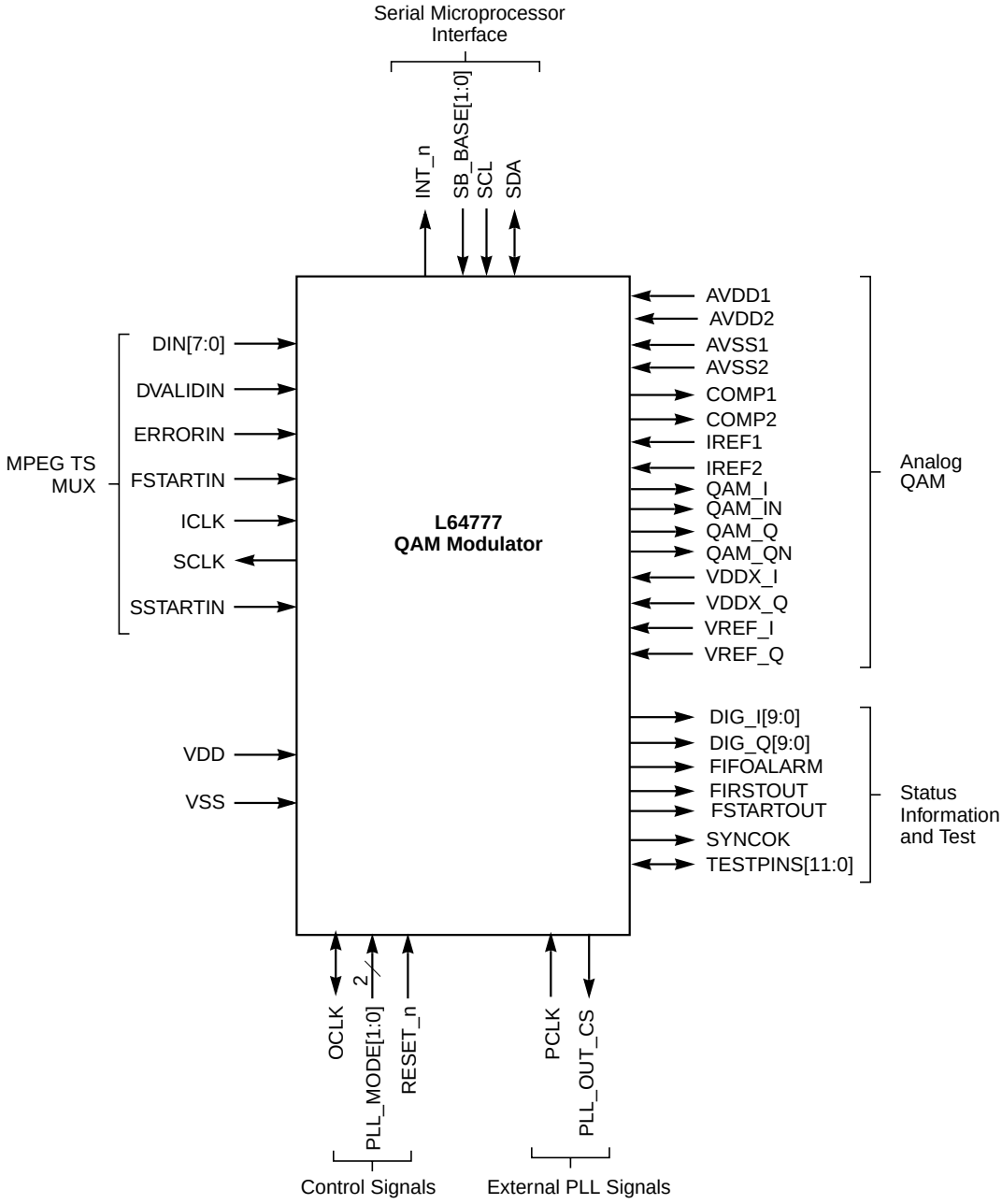
The L64777 supports:

- Full scan test
- BIST for the two RAMs
- JTAG boundary scan
- Digital-to-analog conversion test
- PLL tests

Signals

Figure 8 shows the L64777 interface signals in their respective groupings. Within each category, the signals are described in alphabetical order by signal mnemonic.

Figure 8 Logic Symbol for the L64777



MPEG Transport Stream Multiplexer Signals

DIN[7:0] **QAM Modulator Parallel/Serial Data In** **Input**

Serial data enters the L64777 on DIN[0]; parallel data enters on DIN[7:0]. The modulator samples DIN[7:0] at the positive edge of ICLK. The DIN[7:0] input accepts data with any number of invalid bits in between. The modulator disregards invalid bits or bytes and does not take them into the input FIFO.

DVALIDIN **Clock Enable Input** **Input**

When DVALIDIN is active (HIGH), the L64777 accepts data from DIN[7:0] on a continuous basis. When DVALIDIN is LOW, data input to the internal FIFO and internal data processing stop, and the encoder does not accept new input from the DIN[7:0] pins. DVALIDIN functions independently of the modulator.

ERRORIN **Error Detection Flag** **Input**

The ERRORIN pin is asserted to flag uncorrectable errors. The L64777 checks the ERRORIN status at the first bit of a frame; then, if required (HIGH = set error bit), it copies the value of that bit to the MPEG error-indication bit.

FSTARTIN **External Sync Input** **Input**

The FSTARTIN pin is asserted to mark the beginning of an MPEG transport packet by a hardwired signal. If the incoming bitstream contains no unique sync words, this pulse must be applied to the L64777. The L64777 forces synchronization with FSTARTIN pulses into the chip; it does not flywheel-stabilize synchronization as in the sync word detection mode. In the sync insertion mode, the L64777 regenerates the DVB-defined sync information and inserts it into the QAM Modulator.

ICLK **QAM Modulator Input Clock** **Input**

ICLK is a positive-edge-triggered clock. The L64777 clocks DIN[7:0], DVALIDIN, ERRORIN, FSTARTIN and SSTARTIN on the rising edge of ICLK. ICLK is either a byte clock or a bit clock, depending on control register (Register 1) setup for parallel/serial mode.

SCLK **Modulator Symbol Clock Output** **Output**
SCLK is a clock output synchronous to internally processed symbols and bytes; it is identical to OCLK/4. The L64777 uses SCLK to determine the phase of the Nyquist filter output. The rising edge of SCLK is followed by Phase 0. The falling edge is the transition of Phase 1 to Phase 2 in 4-fold oversampling mode.

SSTARTIN **Sync Sequence Start** **Input**
The SSTARTIN pin is asserted to mark the beginning of a new, fully reset sequence by a hardwired signal. The L64777 evaluates the SSTARTIN negative slope and restarts all internal sequences at the next Block/Frame start following the negative SSTARTIN slope. If no SSTARTIN is applied, all internal sequences run free after the reset.

Status Information Signals

DIG_I[9:0] **Digital I Component** **Output**
This port provides modulator I-component output in digital format. Depending on the PLL mode, either OCLK or PCLK is the related clock.

DIG_Q[9:0] **Digital Q Component** **Output**
This port provides modulator Q-component output in digital format. Depending on the PLL mode, either OCLK or PCLK is the related clock.

FIFOALARM **FIFO Collision Detected** **Output**
If this alarm occurs, the FIFO control has detected equal pointers for read and write access. A detected collision most probably indicates unlocked external PLL-VCO circuitry. The L64777 synchronizes this signal with SCLK-driven flip-flops for the output.

FIRSTOUT **First Block of New Sequence Out** **Output**
FIRSTOUT occurs together with FSTARTOUT and indicates the head of a sync block that has just-reset sequences, as controlled by SSTARTIN. FIRSTOUT is the acceptance of a SSTARTIN negative slope delayed by all internal processing modules.

FSTARTOUT **Frame Start Output** **Output**
FSTARTOUT is asserted during the first symbol in every sync frame. The width of FSTARTOUT reflects the

number of bytes that the gap parameter inserts. A one-cycle width indicates no inserted gaps; a width of 17 means 16 inserted bytes as an Reed-Solomon gap. FSTARTOUT is applied only in sync word detection mode. If FSTARTIN pulses force synchronization, FSTARTOUT is constantly LOW.

SYNCOK **SYNC Detection/Phase Monitoring** **Output**
In internal sync mode, this pin indicates undisturbed synchronization status when HIGH. This signal is asserted when the number of track steps required for synchronization is fulfilled. If FSTARTIN pulses force synchronization, SYNCOK is constantly LOW.

Test Signals

FTMODE[2:0] **Functional Test Bus** **Input**
These must be tied to 0.

IDDTN[3] **IDD Test Mode** **Input**
IDDTN is a production test pin.

NT_OUT[4] **Nand Tree Output** **Output**
NT_OUT is a production test pin.

SCAN_ENABLE[5]
Scan Enable **Input**
This pin enables scan chain shift.

TNn[11] **Test Output Enable** **Input**
TNn switches all 3-state buffers to high-impedance mode for testing.

TRSTn[10] **Test Reset** **Input**
Reset for the JTAG unit.

TMS[9] **Test Mode Select** **Input**
TMS selects the JTAG unit test mode.

TDO[8] **Test Data Output** **Output**
TDO is the JTAG unit data output.

TDI[7] **Test Data Input** **Input**
TDI is the JTAG unit data input.

TCK[6] **Test Mode Clock** **Input**
TCK is the JTAG test mode clock.

Control Signals

OCLK **Encoder Out/Processing Clock In** **Bidirectional**
OCLK is a positive-edge-triggered clock. The L64777 internally processes data based on a fraction of OCLK (for example: scrambler, interleaver, Reed-Solomon encoder) and references data outputs (I, Q, FSTARTOUT) to OCLK.

PLL_MODE[1:0]
Select PLL Mode **Input**
To select the PLL mode:

0b00 or 0b01 for external PLL usage
0b11 for NCO usage.

RESET_n **Reset** **Input**
This pin resets all internal data paths. Reset timing is asynchronous to the device clocks. Reset affects all the configuration registers and the filter coefficients, which must be downloaded again after reset.

External PLL Signals

PCLK **Processing Clock: PLL Mode 2** **Input**
The PCLK output of the L64724 provides this clock, which drives the digital signal processing of interpolation and the NCO. When using Mode 1, leave this pin open.

PLL_OUT_CS **PLL Current Source** **3-State Output**
This pin is a charge pump for an external PLL low pass to control frequency. The comparator is frequency- and phase-sensitive. The pin is normally on 3-state Z level and drives positive and negative current, as required. Depending on the configuration, the current source can be inverted.

Analog QAM Signals

AVDD1 **Analog VDD Input: I Component DAC** **Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

AVDD2 **Analog VDD Input: Q Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

AVSS1 **Analog VSS Input: I Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

AVSS2 **Analog VSS Input: Q Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

COMP1 **Compensation Output: I Comp. DAC Analog Output**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

COMP2 **Compensation Output: Q Comp. DAC Analog Output**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

IREF1 **Reference Current: I Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

IREF2 **Reference Current: Q Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

QAM_I **Symbol I Modulation Analog Output**
QAM_I is the positive differential analog in-phase output signal of the modulator.

QAM_IN **Symbol I Modulation Inverted Analog Output**
QAM_IN is the corresponding inverted differential part to QAM_I.

QAM_Q **Symbol Q Modulation Analog Output**
QAM_Q is the positive differential analog quadrature output signal of the modulator.

QAM_QN **Inverted Differential of QAM_Q** **Analog Output**
QAM_QN is the corresponding inverted differential part to QAM_Q.

VDDX_I **Isolated Power: Digital-to-Analog Converter, I Channel** **Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

VDDX_Q **Isolated Power: Digital-to-Analalog Converter, Q Channel** **Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

VREF_I **Reference Voltage Input: I** **Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

VREF_Q **Reference Voltage Input: Q** **Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

Serial Microprocessor Interface Signals

INT_n **Interrupt Request** **Output**
The L64777 asserts INT_n LOW when the interrupt is enabled and an interrupt condition occurs. INT_n is an open drain output that requires an external pull-up resistor for operation.

SB_BASE[1:0]
Serial Bus Base Address **Input**
The external microprocessor must apply these two signals as static signals to the device because they determine the two LSBs of the serial bus base address.

SCL **Serial Clock Line** **Input**
In conjunction with SDA, SCL controls the microprocessor interface.

SDA	**Serial Data Access** In conjunction with SCL, SDA controls the microprocessor interface.	**Bidirectional**

Specifications

This section provides information about the electrical ratings, pins, and packaging for the L64777.

AC/DC Specifications

The following subsections list the electrical requirements, provide the AC timing characteristics, show the AC timing diagrams, and list the AC timing values for the L64777 decoder.

Electrical Ratings

The tables in this section specify the electrical requirements for the L64777 decoder. Table 1 provides the L64777 absolute maximum electrical and temperature ratings. Table 2 provides the L64777 recommended operating conditions. Table 3 lists the DC characteristics for the L64777.

Table 1 L64777 Absolute Maximum Ratings

Symbol	Parameter	Limits	Unit
V_{DD}	DC Supply	–0.3 to 3.9	V
V_{IN}	LVTTL Input Voltage	–1.0 to V_{DD} + 0.3	V
V_{IN}	5 V Compatible Inputs	–1.0 to 6.5	V
I_{IN}	DC Input Current	10	mA
T_{STG}	Storage Temperature Range (Plastic)	–40 to +150	°C
T_J	Operating Junction Temperature Range	0 to +125	°C

Table 2 L64777 Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
V_{DD}	DC Supply	+ 3.14 to + 3.45	V
T_A	Ambient Temperature	0 to + 70	°C

When studying the values in Table 3, note that the L64777 follows the LSI Logic G10®-p process, which is characterized by a 0.35-micron gate length.

Table 3 L64777 DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{DD}	Supply Voltage		3.14	3.3	3.45	V
V_{IL}	Input Voltage LOW		Vss – 0.5		0.8	V
V_{IH}	Input Voltage HIGH		2.0		V_{DD} + 0.3	V
V_{OH}	Output Voltage HIGH	I_{OH} = – 4.0 mA	2.4		V_{DD}	V
V_{OL}	Output Voltage LOW	I_{OL} = 4.0 mA		0.2	0.4	V
I_{OZ}	Current 3-State Leakage w/Pulldown	V_{DD} = Max, V_{OUT} = V_{SS} or V_{DD}	– 10	± 1	10	µA
I_{IN}	Input Current Leakage	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	– 10	± 1	10	mA
I_{IN}	Input Current Leakage w/Pullup	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	– 62	– 215	– 384	mA
I_{IN}	Input Current Leakage w/Pulldown	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	– 62	– 215	– 384	mA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}			2	mA
I_{CC}	Dynamic Supply Current	ICLK = 54 MHz, PLL MODE 3 PCLK 90 MHz VDD = Max		50		mA

1. Specified at V_{DD} = 3.3 V ± 5% at ambient temperature over the specified range.

AC Timing Diagrams for L64777

Figure 9 illustrates the TS input timing.

Figure 9 TS Input Timing

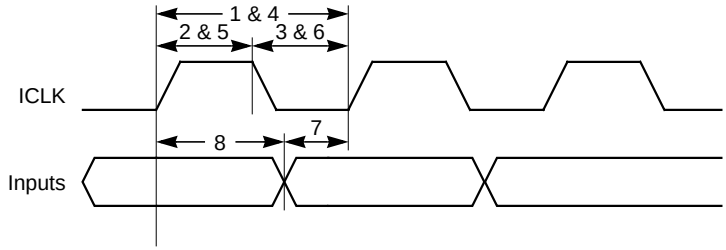


Figure 10 illustrates the reset timing of the L64777.

Figure 10 L64777 RESET Timing Diagram

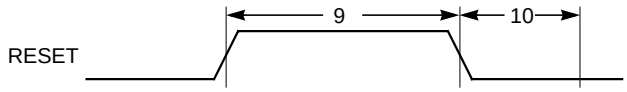
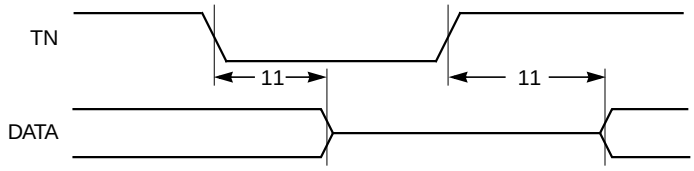


Figure 11 illustrates the 3-state delay timing of the L64777 bus.

Figure 11 L64777 Bus 3-State Delay Timing



Note: Complete the AC timings during the design phase.

The numbers in column 1 of Table 4 refer to the timing parameters in the preceding figures. All parameters in this table apply for T_A = 0 ˚C to 85 ˚C, V_{DD} = 3.1 V to 3.6 V, and an output load of 50 pF.

Table 4 L64777 Preliminary Timing Parameters

No.	Parameter	Description	Min	Max	Unit
1	tCYCLE	Clock Cycle OCLK	32	–	ns
2	tPWH	Clock Pulse Width HIGH OCLK	7	–	ns
3	tPWL	Clock Pulse Width LOW OCLK	7	–	ns
4	tI_CYCLE	Clock Cycle ICLK	18.5	–	ns
5	tI_PWH	Clock Pulse Width HIGH ICLK	9	–	ns
6	tI_PWL	Clock Pulse Width LOW ICLK	9	–	ns
7	tI_S	Input Setup Time to ICLK	6	–	ns
8	tI_H	Input Hold to ICLK	2	–	ns
9	tRWH	Reset Pulse Width HIGH	50	–	ns
10	tWK	Wake-up Time after RESET (used for RAM initialization during microprocessor configuration access)	1280 2560	– –	ICLK cycles with DVALIDIN = HIGH OCLK cycles
11	tTDLY	Delay from TN	–	20	ns

Pin Descriptions and Lists

The following subsections provide descriptions for the electrical pins, as well as numerical and alphabetic listings of all L64777 pins.

L64777 Electrical Pin Descriptions

Table 5 summarizes the electrical properties of the pins on the L64777. The table provides the signal types for both output and input pins, and the drive capacity for outputs.

Table 5 L64777 Pin Description Summary

Mnemonic	Description	Type	Drive (mA)	Active
AVDD1	Supply for DAC	Analog Input	–	–
AVDD2	Supply for DAC	Analog Input	–	–
AVSS1	Analog Supply for DAC	Analog Input	–	–
AVSS2	Supply for DAC	Analog Input	–	–
COMP1	Compensation Output for DAC	Analog Output	–	–
COMP2	Compensation Output for DAC	Analog Output	–	–
DIG_I[9:0]	Digital I Output	Output	4	HIGH
DIG_Q[9:0]	Digital Q Output	Output	4	HIGH
DIN[7:0]	Data Input	TTL Input	–	HIGH
DVALIDIN	Data Enable Input	TTL Input	–	HIGH
ERRORIN	Error Flag Input	TTL Input	–	LOW
FIFOALARM	FIFO Alarm Output	Output	4	HIGH
FIRSTOUT	Beginning of Sequence	Output	4	HIGH
FSTARTIN	Frame Start Input	TTL Input	–	HIGH
FSTARTOUT	Frame Start Output	Output	4	HIGH
FTMODE[2:0]	Functional Test Mode	Input w/Pulldown	–	HIGH
GND	Ground	Analog	–	–
ICLK	Input Clock	TTL Input	–	LOW/ HIGH
IDDTN	IDD Test	TTL Input w/Pullup	–	LOW
INT_n	Interrupt Request	Open Drain, Driving Low	4	LOW

Table 5 L64777 Pin Description Summary (Cont.)

Mnemonic	Description	Type	Drive (mA)	Active
IREF1	Reference Current Input	Analog Input	–	–
IREF2	Reference Current Input	Analog Input	–	–
NT_OUT	Nand Tree	Output	4	HIGH
OCLK	VCO Clock Output or External Clock Input	Bidirectional	–	LOW/ HIGH
PCLK	Clock Input for PLL Mode 2	TTL input	–	HIGH
PLL_MODE[1:0]	Select PLL Mode	Input w/Pulldown	–	HIGH
PLL_OUT_CS	PLL Current Source	3-state Current Source	4	3-state
QAM_I	Positive DAC Output I Channel	Analog Output	–	–
QAM_In	Negative DAC Output I Channel	Analog Output	–	–
QAM_Q	Positive DAC Output Q Channel	Analog Output	–	–
QAM_QN	Negative DAC Output Q Channel	Analog Output	–	–
RESET_n	Chip Reset	TTL Input	–	LOW
SB_BASE[1:0]	Serial Bus Base Address Selector	Input w/Pulldown	–	HIGH
SCAN_ENABLE	Scan Enable	TTL Input w/Pulldown	–	HIGH
SCL	Serial Control Line	Input (5 V-tolerant)	4	HIGH
SCLK	Symbol Clock Output	Output	4	LOW/ HIGH
SDA	Serial Data Access	Bidirectional (5 V-tolerant)	4	Open-drain

Table 5 L64777 Pin Description Summary (Cont.)

Mnemonic	Description	Type	Drive (mA)	Active
SSTARTIN	Sequence Start Input	TTL Input	–	HIGH
SYNCOK	Sync Detection Flag	Output	4	HIGH
TCK	JTAG Test Clock	TTL Input w/Pulldown	–	+[1]
TDI	JTAG Test Data In	TTL Input w/Pulldown	–	HIGH
TDO	JTAG Test Data Out	Output	4	HIGH
TMS	JTAG Test Mode Select	TTL Input w/Pulldown	–	HIGH
TNn	3-State Mode	TTL Input w/Pullup	–	LOW
TRSTn	JTAG Test Reset	TTL Input w/Pulldown	–	LOW
VDDX_I	Supply for Digital DAC Part	Analog Input	–	–
VDDX_Q	Supply for Digital DAC Part	Analog Input	–	–
VREF_I	Voltage Reference	Analog	–	–
VREF_Q	Voltage Reference	Analog	–	–

1. Also 5 V compatible.

Pin Lists for the L64777

Table 6 L64777 Numerical Pin List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
VDD	1	PLL_MODE.0	31	TRSTN	61	VDD	91
VSS	2	PLL_MODE.1	32	VDD	62	VSS	92
QAM_I	3	IDDTN	33	TDO	63	NT_OUT	93
QAM_IN	4	TN	34	INT_N	64	VSS	94
AVDD1	5	RESET_N	35	VSS	65	SCAN_ENABLE	95
IREF1	6	VSS	36	VDD	66	FTMODE.0	96
COMP1	7	DIG_Q.0	37	FIFOALARM	67	FTMODE.1	97
VREF_I	8	DIG_Q.1	38	FIRSTOUT	68	FTMODE.2	98
AVSS	9	DIG_Q.2	39	SYNCOK	69	SB_BASE.0	99
VDDX_I	10	DIG_Q.3	40	FSTARTOUT	70	SB+BASE.1	100
VDDX_Q	11	DIG_Q.4	41	VSS	71	VSS	101
AVSS2	12	VSS	42	VDD	72	PCLK	102
VREF_Q	13	VDD	43	DIN.7	73	VSS	103
COMP2	14	DIG_Q.5	44	DIN.6	74	VDD	104
IREF2	15	DIG_Q.6	45	DIN.5	75	SCLK	105
AVDD2	16	DIG_Q.7	46	DIN.4	76	DIG_I.0	106
QAM_QN	17	DIG_Q.8	47	VDD	77	DIG_I.1	107
QAM_Q	18	DIG_Q.9	48	VSS	78	DIG_I.2	108
NC	19	VSS	49	VSS	79	DIG_I.3	109
GND	20	VSS	50	ICLK	80	DIG_I.4	110
NC	21	VDD	51	DIN.3	81	VDD	111
NC	22	OCLK	52	DIN.2	82	DIG_I.5	112
NC	23	VDD	53	DIN.1	83	DIG_I.6	113
NC	24	VSS	54	DIN.0	84	DIG_I.7	114
NC	25	VSS	55	VSS	85	DIG_I.8	115
VSS	26	TCK	56	VDD	86	DIG_I.9	116
PLL_OUT_CS	27	TDI	57	DVALIDIN	87	VDD	117
VDD	28	TMS	58	ERRORIN	88	VSS	118
VDD	29	VSS	59	FSTARTIN	89	SCL	119
NC	30	VDD	60	SSTARTIN	90	SDA	120

1. *NC* pins are not connected.

Table 7 L64777 Alphabetical Pin List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AVDD1	5	DIN.4	76	PLL_MODE.1	32	VDD	77
AVDD2	16	DIN.5	75	PLL_OUT_CS	27	VDD	86
AVSS	9	DIN.6	74	QAM_I	3	VDD	91
AVSS2	12	DIN.7	73	QAM_IN	4	VDD	104
COMP1	7	DVALIDIN	87	QAM_Q	18	VDD	111
COMP2	14	ERRORIN	88	QAM_QN	17	VDD	117
DIG_I.0	106	FIFOALARM	67	RESET_N	35	VDD	62
DIG_I.1	107	FIRSTOUT	68	SB+BASE.1	100	VDDX_I	10
DIG_I.2	108	FSTARTIN	89	SB_BASE.0	99	VDDX_Q	11
DIG_I.3	109	FSTARTOUT	70	SCAN_ENABLE	95	VREF_I	8
DIG_I.4	110	FTMODE.0	96	SCL	119	VREF_Q	13
DIG_I.5	112	FTMODE.1	97	SCLK	105	VSS	2
DIG_I.6	113	FTMODE.2	98	SDA	120	VSS	26
DIG_I.7	114	GND	20	SSTARTIN	90	VSS	36
DIG_I.8	115	ICLK	80	SYNCOK	69	VSS	42
DIG_I.9	116	IDDTN	33	TCK	56	VSS	49
DIG_Q.0	37	INT_N	64	TDI	57	VSS	50
DIG_Q.1	38	IREF1	6	TDO	63	VSS	54
DIG_Q.2	39	IREF2	15	TMS	58	VSS	55
DIG_Q.3	40	NC	22	TN	34	VSS	59
DIG_Q.4	41	NC	30	TRSTN	61	VSS	65
DIG_Q.5	44	NC	21	VDD	1	VSS	71
DIG_Q.6	45	NC	19	VDD	28	VSS	78
DIG_Q.7	46	NC	23	VDD	29	VSS	79
DIG_Q.8	47	NC	24	VDD	43	VSS	85
DIG_Q.9	48	NC	25	VDD	51	VSS	92
DIN.0	84	NT_OUT	93	VDD	53	VSS	94
DIN.1	83	OCLK	52	VDD	60	VSS	101
DIN.2	82	PCLK	102	VDD	66	VSS	103
DIN.3	81	PLL_MODE.0	31	VDD	72	VSS	118

1. *NC* pins are not connected.

Package Pinout

Figure 12 Package 120-Pin PQFP Pinout

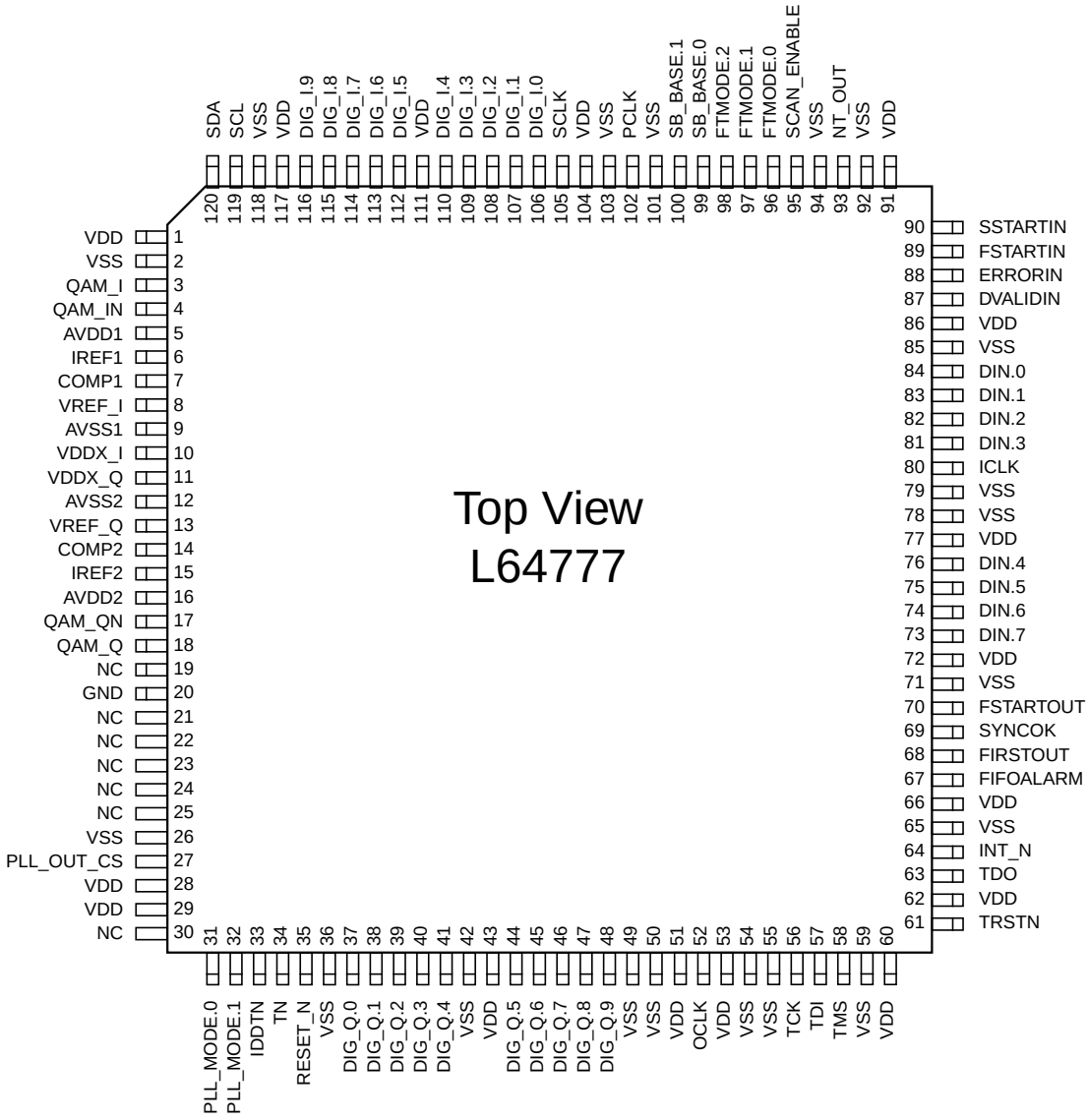


Figure 13 provides a mechanical drawing of the 120-pin PQFP for the L64777.

Figure 13 120-pin PQFP (PE) Mechanical Drawing

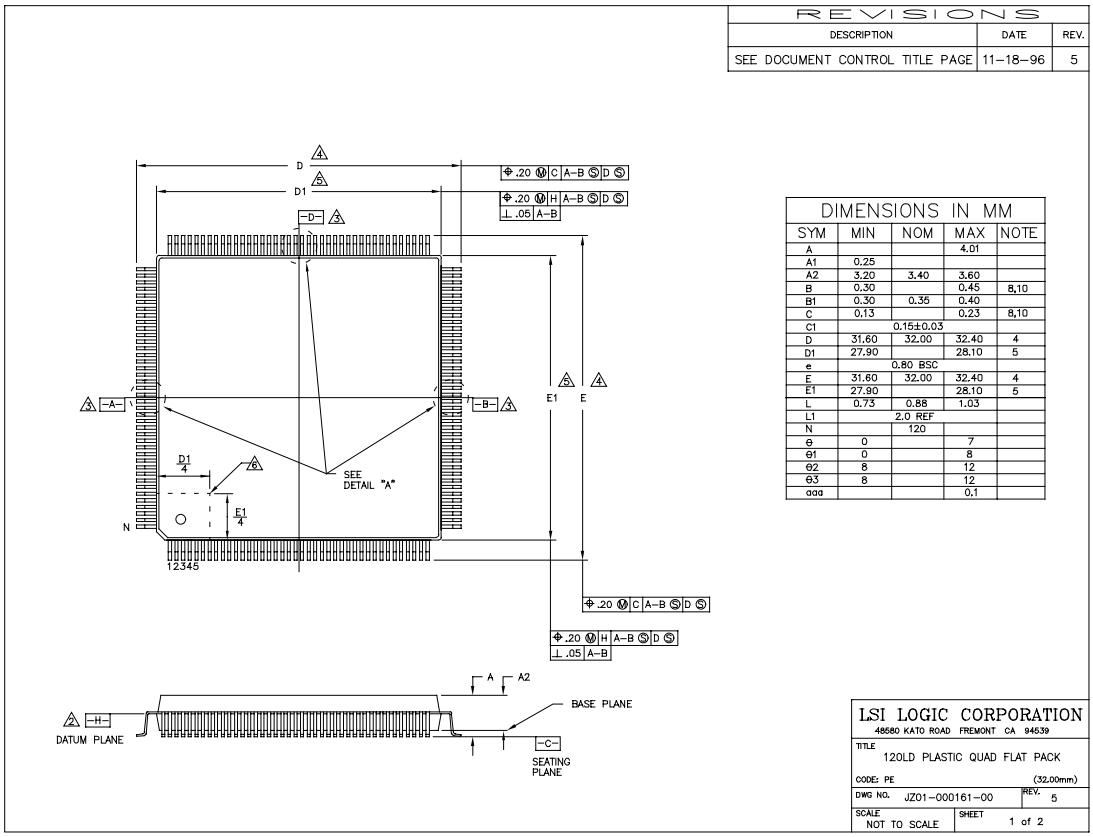


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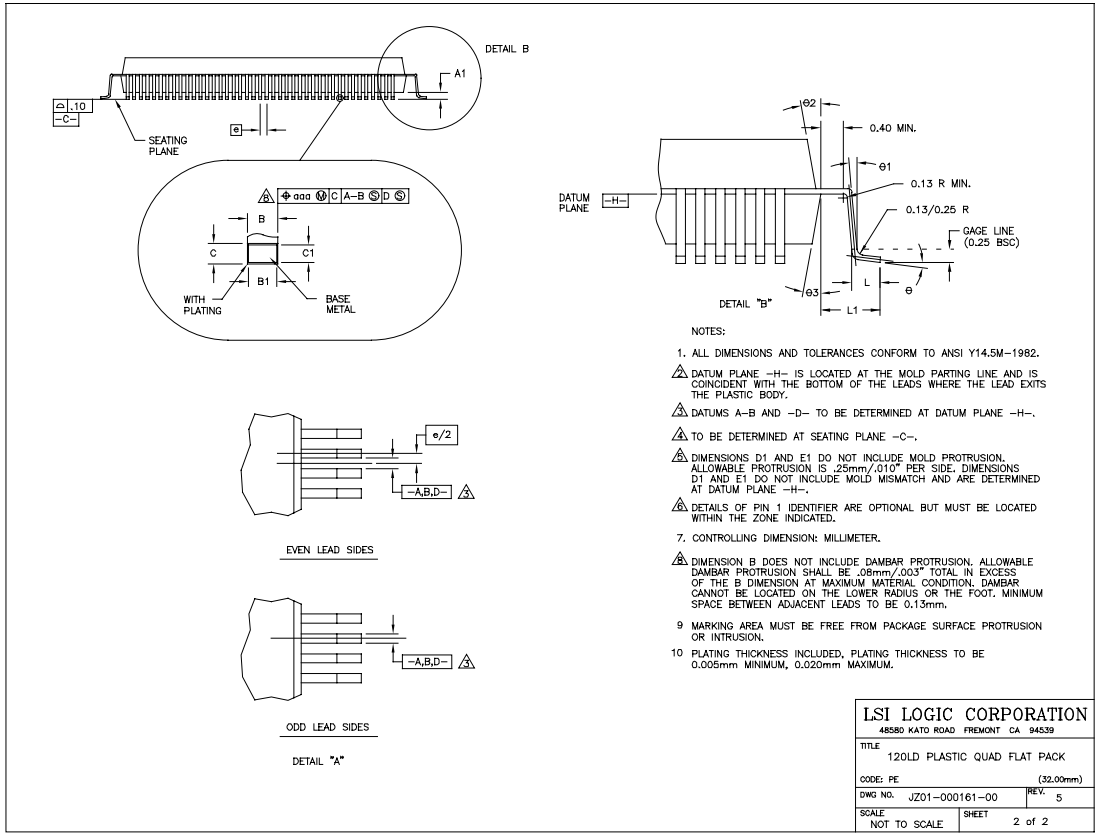
Figure 13 120-pin PQFP (PE) Mechanical Drawing (Cont.)



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