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Photon Vision Systems

High Performance Area CMOS Image Sensors
ACS-I XXXX Family
ACS-I 512, 1024, 2048 – CPGA, -POLY
Integrated Imaging System on a Chip, Digital Output

The Photon Vision Systems ACS-I series is a family of high performance area image sensors designed for a wide variety of applications in the scientific and medical markets, including:

Inspection
Gauging
Spectrometry
Cell counting/measurements and imaging
Medical imaging
Laser beam profiling
Astronomy
Object tracking
Identification Systems
2D and 1D bar code reading
Etc.

Description

The ACS-I XXX family of Imagers consists of an array of low dark current photo-diode pixels. This sensor is based on our patented Active Column Sensor ™ (ACS) technology, which provides far superior performance over most any CMOS imager on the market today. Each pixel also contains a storage site, allowing electronic shutter or adaptive exposure control. These Imaging systems may be controlled externally, or operate completely autonomously using the on-chip configuration registers and programmable multi-mode controller.

These devices are available in a variety of package types, or are available in die form for chip on board applications.

All that is needed to complete a camera is a single power supply and an external oscillator. This minimum configuration will allow the device to run at default settings. A remote control can be used to modify the device settings to control the myriad of on board capabilities.

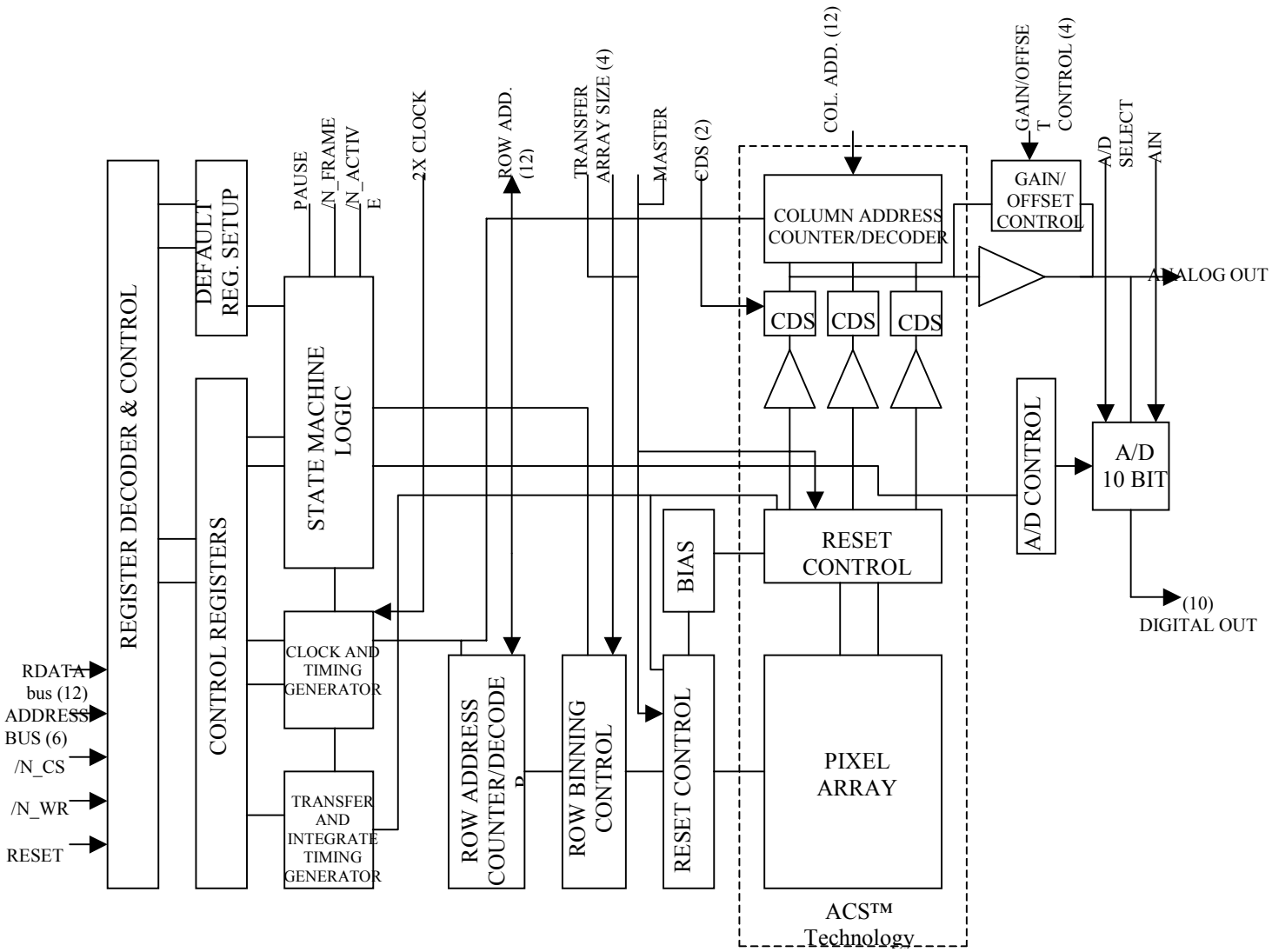
This device is protected by patent number 6,084,229and other patents pending.

Key Features

- Independent programmable timers for exposure control and readout.
- Low Cost Compared to CCD systems
- Single Supply Operation
- High Sensitivity
- On chip row binning for divide by 2 or divide by 4 resolution modes.
- Dual shutter control for rolling or snap shot (strobed) modes.
- Accumulation mode for auto exposure Operation.
- Sample and Hold.

- Low Dark Current.
- On board high speed 10 bit ADC, parallel digital output
- PVS-BUS™ High Speed Analog output
- Programmable offset/gain control
- Fully Integrated on chip FPN cancellation
- Dual simultaneous programmable regions of interest
- External or internal synchronization Control.
- Random, sequential, or interlaced readout.
- Optically clear glass package (Packaged Version)
- User selectable output voltage, 3.3 or 5.0 VDC for digital video, pixel clock, and sync signals.
- Cascadable, tri-state buses allow multiple imagers to be cascaded together on common busses.

Functional Block



Electrical Characteristics/Recommended Operating Conditions

Pixel Type	Active Column Sensor ™ photo diode		
Array Size	512x512 (ACS-I 512)	1026 x 1026 (ACS-I 1024)	2048 x 2048 (ACS-I 2048)
Pixel Size (Pitch)	12u X 12u		
Imaging Active Area	6.15mm X 6.15mm	13.21mm X 13.21mm	24.58mm X 24.58mm
Output	2K ohm output impedance Analog and 10bit digital		
Fill Factor approx.	≥60 %		

Parameter	**Test Conditions**	**Min**	**Typical**	**Max**	**Units**
Supply Voltage		4.75	5.0	5.25	V
Power Consumption			150	300	mW
Input High Level		2.5			V
Input Low Level				0.7	V
Pixel Read Rate - Analog		0.5	24	30	MHz
Pixel Read Rate - Digital		1.2		24	MHz
Analog output External Load			2000		Ohms
Digital Output External Load			1		TTL Gate
Output Voltage at Saturation	Analog Out.	0.8	0.9	1.1	V
Output Voltage at Dark	Analog Out.	2.6	2.8	3.2	V
Linearity per pixel	5%-70% avg.	0.05	2.5	5.0	%SAT
Dark Signal	1 sec. Integration time		<0.2	<2.0	%SAT
Dynamic Range (RMS)	Vsat/RMS Noise Analog Out.		60	70	dB
Conversion factor - user selectable	See Note 1	2.5		10	µv/e
Pixel – Pixel FPN	Across array		0.5		rms %
Full Well	See Note 1		600k		electrons
Quantum Efficiency	@500nm		50.0 Nom.		% Norm.
Read Noise			50	100	rms electrons
Spectral response	See curve	350		1100	nm
Image Lag		0.1	1.0	3.0	%SAT
Relative Humidity		0		90	%
Operating Temperature		0		70	°C

Notes: 1. Digitized 10 bits up to 24 Mhz, Analog output up to 30 Mhz. Conversion factor is user selectable via setup registers.

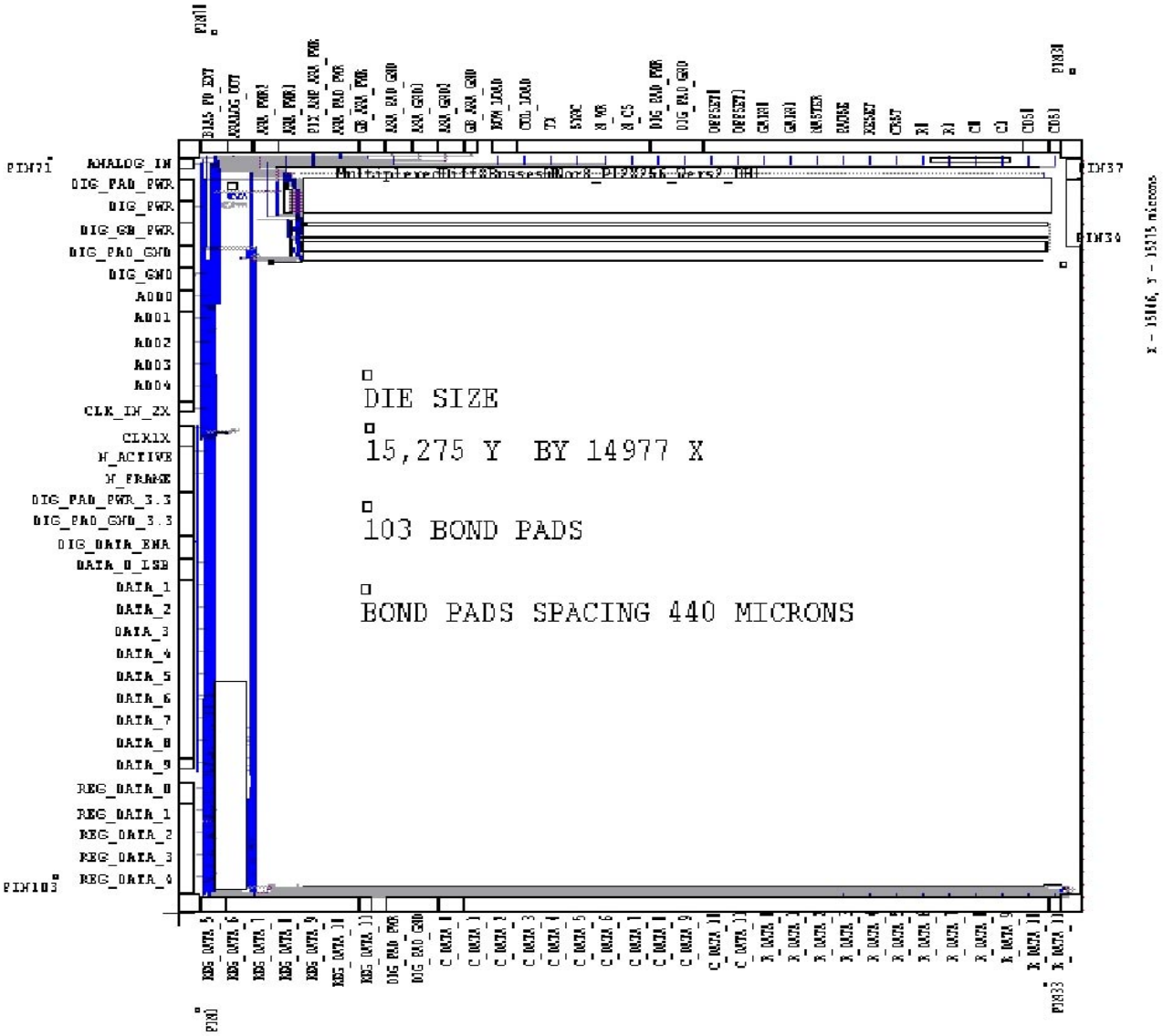
2. Specs. Given at pixel rates of 5.0MHz at 24 deg. C.

Absolute maximum ratings, T_A = 25°C unless otherwise noted, see Note †

Supply voltage range, V_{DD} ---------- 0 V to 5.15 V
Digital input current range, I ---------- –20 mA to 20 mA
Operating case temperature range, T C (see Note 2)---------- –10°C to 85°
Operating free-air temperature range, T A ---------- 0°C to 60°C
Storage temperature range ---------- –20°C to 85°C
Humidity range, Rh ---------- 0-100%, non-condensing
Lead temperature 1.5 mm (0.06 inch) from case for 10 seconds---------- 255°C

† Exceeding the ranges specified under “absolute maximum ratings” can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated above, is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.
NOTES: 1. Voltage values are with respect to the device GND terminal.
2. Case temperature is defined as the surface temperature of the package measured directly over the integrated circuit.

Figure 1 - Die bond pad layout



Device Bond-out

Bond No.	Name	Signal Type	Description
1	REG_DATA_5	Bi-directional I/O See pins 54, 55	Setup Register data bit 5. See Register setup table for more information
2	REG_DATA_6	Bi-directional I/O See pins 54, 55	Setup Register data bit 6. See Register setup table for more information
3	REG_DATA_7	Bi-directional I/O See pins 54, 55	Setup Register data bit 7. See Register setup table for more information
4	REG_DATA_8	Bi-directional I/O See pins 54, 55	Setup Register data bit 8. See Register setup table for more information
5	REG_DATA_9	Bi-directional I/O See pins 54, 55	Setup Register data bit 9. See Register setup table for more information
6	REG_DATA_10	Bi-directional I/O See pins 54, 55	Setup Register data bit 10. See Register setup table for more information
7	REG_DATA_11	Bi-directional I/O See pins 54, 55	Setup Register data bit 11, MSB. See Register setup table for more information
8	DIG_PAD_PWR	Digital Pad Power 5.0 VDC	Power in for Digital Pad circuits except video DATA Pads, see pins 83-98. Connected on-chip with pins 53, 72, 73, and 74.
9	DIG_PAD_GND	Digital Pad Power Ground	Power ground for Digital Pad circuits except video DATA Pads, see pins 83-98. Connected on-chip with pins 52, 75, and 76.
10	C_DATA_0 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address LSB BIT 0 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
11	C_DATA_1 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 1 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
12	C_DATA_2 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 2 - If in SLAVE mode, input column Pin must be connected whenever in SLAVE mode, do not float. address for random access. If in MASTER mode, output for currently addressed pixel.
13	C_DATA_3 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 3 - If in SLAVE mode, input column Pin must be connected whenever in SLAVE mode, do not float. address for random access. If in MASTER mode, output for currently addressed pixel.
14	C_DATA_4 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 4 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
15	C_DATA_5 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 5 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
16	C_DATA_6 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 6 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
17	C_DATA_7 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 7 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
18	C_DATA_8 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 8 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
19	C_DATA_9 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 9 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
20	C_DATA_10 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 10 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
21	C_DATA_11 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address MSB BIT 11 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
22	R_DATA_0 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address LSB BIT 0 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
23	R_DATA_1 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 1 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.

24	R_DATA_2 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 2 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
25	R_DATA_3 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 3 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
26	R_DATA_4 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 4 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
27	R_DATA_5 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 5 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
28	R_DATA_6 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 6 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
29	R_DATA_7 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 7 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
30	R_DATA_8 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 8 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
31	R_DATA_9 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 9 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
32	R_DATA_10 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 10 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
33	R_DATA_11 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address MSB BIT 11 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
34	N.C.	No connection	Do not connect
35	LAST_PIXEL_OUT	Digital Input	When high, the last pixel of a frame is not output, instead, the ANALOG_IN (pin 71) is output. When low, the last pixel is output.
36	N.C	No connection	Do not connect
37	EXT_ANALOG_SELECT	Digital Input	When high, the analog input is output, when low video is output.
38	CDS1	Digital Input CDS0 CDS1 0 0 - Full CDS 0 1 - Quasi CDS 1 0 – No CDS 1 1 – Transfer and readout	CDS Mode select MSB - If in SLAVE mode, input CDS Mode select. Use in conjunction with pin 39. Standard readout mode Readout mode used for snapshot Readout mode used during adaptive exposure control Transfer and Readout
39	CDS0	Digital Input See table, pin 38	CDS Mode select LSB - If in SLAVE mode, input CDS Mode select. Use in conjunction with pin 38.
40	C1	Digital Input	Reserved for future use - Do Not Connect
41	C0	Digital Input	Reserved for future use - Do Not Connect
42	R1	Digital Input R1 R0 0 0 - 1X 0 1 - 2X 1 X - 4X	Row Binning control MSB - If in SLAVE mode, input Row Binning control. Use in conjunction with pin 43. 1X - Device outputs full vertical pixel resolution 2X - Every 2 rows are binned, vertical resolution is divided by2 4X - Every 4 Rows are binned, vertical resolution is divided by 4
43	R0	Digital Input See table, pin 42	Row Binning control LSB - If in SLAVE mode, input Row Binning control. Use in conjunction with pin 42.

44	CRST	Digital Input TX CRST 0 X - M1 1 X - M2 X 0 - M3 X 1 - M4	Exposure Control LSB, used in conjunction with pin 57. If in SLAVE mode, input Exposure control. This is a global (all pixels) function. Note that TX and CRST are global for all pixels at once. M1 - Transfer accumulated charge from pixel to Storage site. M2 - Storage Site retains current charge M3 - Reset pixels M4 - Accumulate charge at pixel - Begin Integrating
45	RESET	Digital Input	RESET Command bit. Forces master reset of state machine to default values.
46	PAUSE	Digital Input 0 - Transfer and read 1 - Transfer and pause	PAUSE Control bit. If in SLAVE mode, input PAUSE. When bit is on, the device will halt after transferring the charge to the hold site. This will prevent the readout cycle from beginning until the bit is cleared. Note that in MASTER mode, both the SETUP register control bit for PAUSE and this PAUSE signal must both be OFF for a read cycle to begin.
47	MASTER	Digital Input 0 - SLAVE Mode 1 - MASTER Mode	MASTER/SLAVE Mode select. When ON, device is in MASTER mode. When OFF, device is in SLAVE Mode. When in MASTER mode, those signals indicated with the 'M/S' symbol indicate that the function of these signals is depends on the selected Mode. Typically when the device is in MASTER mode, the 'M/S' signals like the row and column address buses output the currently accessed pixel. When in SLAVE mode, the 'M/S' signals are used to externally access these buses for random access.
48	GAIN1	Digital Input GAIN0, 1 OFFSET0, 1 0 0 1 1 - S1 0 0 1 0 - S2 0 0 0 1 - S3 0 0 0 0 - S4 0 1 1 1 - S5 0 1 1 0 - S6 0 1 0 1 - S7 0 1 0 0 - S8 1 0 1 1 - S9 1 0 1 0 - S10 1 0 0 1 - S11 1 0 0 0 - S12 1 1 1 1 - S13 1 1 1 0 - S14 1 1 0 1 - S15 1 1 0 0 - S16	GAIN and OFFSET control. Works in conjunction with pins 49-51. If in SLAVE mode input desired Gain and offset from table below. Default is 1X gain and no offset. GAIN SETTING / OFFSET SETTING (Volts) S1 - 1.00 / 0.00 S2 - 1.33 / 0.30 S3 - 2.00 / 0.60 S4 - 4.00 / 0.90 S5 - 4.00 / 0.30 S6 - 4.00 / -0.30 S7 - 4.00 / -0.90 S8 - 2.00 / 0.00 S9 - 2.00 / -0.60 S10 - 1.33 / -0.30 S11 - NA S12 - NA S13 – NA S14 - NA S15 - NA S16 - NA
49	GAIN0	Digital Input See table, pin 48.	GAIN and OFFSET control. Works in conjunction with pins 48, 50, and 51. If in SLAVE mode input desired Gain and offset from table – see pin 48.
50	OFFSET1	Digital Input See table, pin 48.	GAIN and OFFSET control. Works in conjunction with pins 48, 49, and 51. If in SLAVE mode input desired Gain and offset from table – see pin 48.
51	OFFSET0	Digital Input See table, pin 48.	GAIN and OFFSET control. Works in conjunction with pins 49-50. If in SLAVE mode input desired Gain and offset from table – see pin 48.
52	DIG_PAD_GND	Digital Pad Power Ground	Power ground for Digital Pad circuits except video DATA Pads, see pins 83-98. Connected on-chip with pins 9, 75 and 76.
53	DIG_PAD_PWR	Digital Pad Power 5.0 VDC	Power in for Digital Pad circuits except video DATA Pads, see pins 83-98. Connected on-chip with pins 8, 53, 72, 73, and 74.
54	$\overline{\text{N\_CS}}$	Digital Input	Controls direction of REG_DATA lines, pins 99-100 and pins 1-7, by reading or writing to setup registers. Works in conjunction with pin 55. See SETUP REGISTER TIMING diagrams for details. Verbal description - Register WRITE cycle: With pin 54 high, set pin 54 low and input register address on the ADD lines, pins 77-81 and also input register data to REG_DATA lines, pins 99-100 and 1-7. Pulse pin 54 low for one clock cycle to write the data to the setup register. Verbal description - Register READ cycle: With pin 54 high, set pin 55 high and input register address on the ADD lines, pins 77-81. Set pin 54 low to output register data to REG_DATA lines, pins 99-100 and 1-7.

55	_____ N_WR	Digital Input	Controls direction of REG_DATA lines, pins 99-100 and pins 1-7, by reading or writing to setup registers. Works in conjunction with pin 54. See SETUP REGISTER TIMING diagrams for details. Do not change the state of this pin whenever pin 54 is low, or register data corruption and/or unpredictable operation or device damage may result.
56	SYNC	Digital Input	External Input that controls the exposure state machine when the stop bit of the control register is set to zero. Rising edge of SYNC starts the exposure control state machine. This allows external synchronization of the imager. Otherwise if STOP bit in the control register is high, the imager free runs asynchronously.
57	TX	Digital Input See table, pin 44	Exposure Control MSB, used in conjunction with pin 44. If in SLAVE mode, input Exposure control. This is a global (all pixels) function.
58	COL_LOAD	Digital Input SLAVE only	Load Column Address that is loaded onto C_DATA bus (pins 10-21) into imager. Only Works in SLAVE mode.
59	ROW_LOAD	Digital Input SLAVE only	Load Row Address that is loaded onto the R_DATA bus (pins 22-33) into imager. Only works in SLAVE mode.
60	GB_ANA_GND	Guard Band analog Ground.	Ground input for Analog guard band. Use with pin 64 and must be connected.
61	ANA_GND2	Analog Circuits 2 Ground	Ground input for the A/D. Use with pin 68 and must be connected.
62	ANA_GND1	Analog Circuits 1 Ground	Ground input for the A/D. Use with pin 67 and must be connected.
63	ANA_PAD_GND	Analog Pad Ground	Ground input for analog pads. Use with pin 65 and must be connected.
64	GB_ANA_PWR	Guard Band analog POWER 5.0 VDC	Power in for Analog Guard Band. Use with pin 60 and must be connected.
65	ANA_PAD_PWR	Analog Pad POWER 5.0 VDC	Power in for analog pads. Use with pin 63 and must be connected.
66	PIX_AMP_ANA_PWR	Analog Power 5.0 Volts	Power to Column amplifier
67	ANA_PWR1	Analog Circuits 1 POWER 5.0 VDC	Power in for the A/D. Use with Pin 62 and must be connected.
68	ANA_PWR2	Analog Circuits 2 POWER 5.0 VDC	Power in for the A/D. Use with pin 61 and must be connected.
69	ANALOG_OUT	Analog Video Out	Video output - analog. Do not Connect if using Digital output. See Electrical Parameters for maximum load. Referenced to pin 61.
70	BIAS_PAD_EXT	Analog pixel Bias	Tie a 10-30pF capacitor from this pin to analog ground, pin 63.
71	ANALOG_IN	Analog input, Range 0.9-3.2 VDC	Referenced to pin 62. Use this pin to input an external analog signal for referencing the A/D and/or calibration. Note that the last pixel of each frame read is the converted value of this reference, not the value of the pixel, when Control Reg. 1 bit 1 is set high.
72	DIG_PAD_PWR	Digital Pad Power 5.0 VDC	Power in for Digital Pad circuits except video DATA Pads, see pins 83-98. Connected on-chip with pins 8, 53, 73, and 74.
73	DIG_PWR	Digital Circuits Power 5.0 VDC	Power in for Digital circuits except video DATA Pads, see pins 83-98. Connected on-chip with pins 8, 53, 72, and 74.
74	DIG_GB_PWR	Digital Guard Band Power 5.0 VDC	Power in for Digital Guard Band. Connected on-chip with pins 8, 53, 72, and 73.
75	DIG_PAD_GND	Digital Pad Ground	Power in for Digital Pad circuits except video DATA Pads, see pins 83-98. Connected on-chip with pins 9, 52, and 76.
76	DIG_GND	Digital Ground	Ground input for Digital circuits. See also pin 75. Connected on-chip with pins 9, 52, and 75.
77	ADD0	Digital Input Setup Register Address Bit 0 - LSB.	Setup register address bit 0 - LSB. Address bus for access to the SETUP REGISTERS. See pins 54-55, 99-103, and 1-7.
78	ADD1	Digital Input Setup Register Address Bit 1.	Setup register address bit 1. Address bus for access to the SETUP REGISTERS. See pins 54-55, 99-103, and 1-7.
79	ADD2	Digital Input Setup Register Address Bit 2.	Setup register address bit 2. Address bus for access to the SETUP REGISTERS. See pins 54-55, 99-103, and 1-7.

80	ADD3	Digital Input Setup Register Address Bit 3.	Setup register address bit 3. Address bus for access to the SETUP REGISTERS. See pins 54-55, 99-103, and 1-7.
81	ADD4	Digital Input Setup Register Address Bit 4 - MSB.	Setup register address bit 4. Address bus for access to the SETUP REGISTERS. See pins 54-55, 99-103, and 1-7.
82	CLK_IN_2X	Digital Input Master Clock	Input for Master Clock, must be 2X desired pixel read rate.
83	CLK1X	Digital Output Pixel Clock	Output Pixel Clock Rate. Note that this pin is referenced to pin 87.
84	_____ N_ACTIVE	Digital Output Row video Valid	Output goes low when an active line of video is output. Note that this pin is referenced to pin 87.
85	_____ N_FRAME	Digital Output Frame Valid	Output goes low when an active frame of video is output. Note that this pin is referenced to pin 87.
86	DIG_PAD_PWR_3.3	Digital Pad Power for Digital Video 3.3 OR 5.0 VDC	Power select for digital video and control lines, pins 83-98. If 5.0 VDC signal levels are desired for these pins, then input 5.0 VDC. If 3.3 VDC signal levels are desired, then input 3.3 VDC here.
87	DIG_PAD_GND_3.3	Ground for DIG_PAD_3.3 Ground	Ground in for power supply used for pin 86.
88	DIG_DATA_ENA	Digital Input Digital video Data enable.	When ON, the on-chip A/D is enabled, and digital video is output. When enabled, do not connect the analog output (see pin 71). When OFF, the DATA lines, pins 89-98 are tri-stated. This features allows imagers to be cascaded. When OFF and using the analog output, do not connect the digital video lines, pins 89-98.
89	DATA_0_LSB	Tri-state Output Digitized video Bit 0 LSB	When pin 88 is ON, digital video is output as Bit 0, LSB. When pin 88 is OFF, this output is tri-stated. Do not connect this pin if using analog video out, pin 69.
90	DATA_1	Tri-state Output Digitized video Bit 1	When pin 88 is ON, digital video is output as Bit 1. When pin 88 is OFF, this output is tri-stated. Do not connect this pin if using analog video out, pin 69.
91	DATA_2	Tri-state Output Digitized video Bit 2	When pin 88 is ON, digital video is output as Bit 2. When pin 88 is OFF, this output is tri-stated. Do not connect this pin if using analog video out, pin 69.
92	DATA_3	Tri-state Output Digitized video Bit 3	When pin 88 is ON, digital video is output as Bit 3. When pin 88 is OFF, this output is tri-stated. Do not connect this pin if using analog video out, pin 69.
93	DATA_4	Tri-state Output Digitized video Bit 4	When pin 88 is ON, digital video is output as Bit 4. When pin 88 is OFF, this output is tri-stated. Do not connect this pin if using analog video out, pin 69.
94	DATA_5	Tri-state Output Digitized video Bit 5	When pin 88 is ON, digital video is output as Bit 5. When pin 88 is OFF, this output is tri-stated. Do not connect this pin if using analog video out, pin 69.
95	DATA_6	Tri-state Output Digitized video Bit 6	When pin 88 is ON, digital video is output as Bit 6. When pin 88 is OFF, this output is tri-stated. Do not connect this pin if using analog video out, pin 69.
96	DATA_7	Tri-state Output Digitized video Bit 7	When pin 88 is ON, digital video is output as Bit 7. When pin 88 is OFF, this output is tri-stated. Do not connect this pin if using analog video out, pin 69.
97	DATA_8	Tri-state Output Digitized video Bit 8	When pin 88 is ON, digital video is output as Bit 8. When pin 88 is OFF, this output is tri-stated. Do not connect this pin if using analog video out, pin 69.
98	DATA_9	Tri-state Output Digitized video Bit 9	When pin 88 is ON, digital video is output as Bit 9. When pin 88 is OFF, this output is tri-stated. Do not connect this pin if using analog video out, pin 69.
99	REG_DATA_0	Bi-directional I/O See pins 54, 55	Setup Register data bit 0, LSB. See Register setup table for more information
100	REG_DATA_1	Bi-directional I/O See pins 54, 55	Setup Register data bit 1. See Register setup table for more information
101	REG_DATA_2	Bi-directional I/O See pins 54, 55	Setup Register data bit 2. See Register setup table for more information
102	REG_DATA_3	Bi-directional I/O See pins 54, 55	Setup Register data bit 3. See Register setup table for more information
103	REG_DATA_4	Bi-directional I/O See pins 54, 55	Setup Register data bit 4, MSB. See Register setup table for more information

SETUP REGISTERS

When the device is in MASTER mode, the on-chip state machine uses the information in the setup registers to control the imager. These registers are 12 bits wide. The register data can be accessed via the bi-directional REG_DATA 12 bit wide parallel bus, pins 1-7 and 99-103. These are accessed via a 5 bit address bus ADD, pins 77-81. The Input signals N_CS (pin 54) and N_WR (pin 55) are used to control the reading of, or writing to, of the setup registers. See SETUP REGISTER ACCESS TIMING diagrams, below.

Region of Interest Registers:
The device has the ability to control 2 regions of interest simultaneously. This allows for faster sub frame readout. The ROI Registers must contain a valid non-zero value for that ROI to operate. Note that at least one of the ROI's must be setup in order to scan video. The ROIs can overlap, but note that the pixels read in the first ROI are valid in the overlap region. When the second ROI is read, the pixels sharing the same rows as that of the first ROI will not be valid.

The SETUP registers are as follows;

REGISTER ADDRESS (Hex)	NAME	DESCRIPTION	DEFAULT VALUE
0	ROI 0 Row Start	Row Address of pixel for ROI 0 to Start – must be less than REG. 1.	0
1	ROI 0 Row Stop	Row Address of pixel for ROI 0 to Stop – Must be greater than REG. 0.	1023
2	ROI 0 Col. Start	Column Address of pixel for ROI 0 to Start – must be less than REG. 3.	0
3	ROI 0 Col. Stop	Column Address of pixel for ROI 0 to Stop – Must be greater than REG. 2.	1023
4	ROI 1 Row Start	Row Address of pixel for ROI 1 to Start – must be less than REG. 5.	0
5	ROI 1 Row Stop	Row Address of pixel for ROI 1 to Stop – Must be greater than REG. 4.	0
6	ROI 1 Col. Start	Column Address of pixel for ROI 1 to Start – must be less than REG. 7.	0
7	ROI 1 Col. Stop	Column Address of pixel for ROI 1 to Stop – Must be greater than REG. 6.	0
8	Reserved	Do not write to this register	0
9	Reserved	Do not write to this register	0
A	Reserved	Do not write to this register	0
B	Reserved	Do not write to this register	0
C	Reserved	Do not write to this register	0
D	Reserved	Do not write to this register	0
E	Reserved	Do not write to this register	0
F	Reserved	Do not write to this register	0
10	FFS HOLDOFF	Full Frame Shutter Mode Holdoff Control Register. This register contains the 'hold off' time from the start of the state machine logic until the pixel site is allowed to accumulate charge. The pixels are held in reset for this time period. The register default is 0 for full frame integration.	0
11	TRANSFER	Transfer Control Register. The charge is transferred from the pixel to the storage site when the state machine logic reaches the value of this register. If the STOP bit (bit 11) in Control Register 0 is set high, a new frame cycle will then begin.	0
12	CONTROL 0	Control Register 0 – See Register 0 bit description, below.	See Below
13	CONTROL 1	Control Register 1 – See Register 1 bit description, below.	See Below
14	ROLLING HOLDOFF	Rolling Shutter mode Holdoff Control Register, controls exposure time in rolling shutter mode. This register determines the number of rows back from the current row being read to reset and put back into integration that row. Units are in rows.	0
15-1F	Reserved	Do not write to these Registers.	0

CONTROL REGISTERS:

CONTROL REGISTER 0 and 1 are broken into separate control bits, as described below. Note that some of these bits have a corresponding I/O pin. The I/O pin is used for the described function whenever the device is in SLAVE mode, otherwise, the I/O pin is ignored in MASTER mode. See the bond out table above for more information.

CONTROL REGISTER BIT DESCRIPTIONS

CONTROL REGISTER	BIT #	Name	Description	Default
0	0	F1	Offset select bit 1. Works in conjunction with bits 1, 2, and 3 below. See bond out description for pin 50 for more information. This bit only works in MASTER mode.	0
0	1	F0	Offset select bit 0. Works in conjunction with bits 0, 2, and 3. See bond out description for pin 51 for more information. This bit only works in MASTER mode.	0
0	2	G1	Gain select bit 1. Works in conjunction with bits 0, 1, and 3. See bond out description for pin 48 for more information. This bit only works in MASTER mode.	1
0	3	G0	Gain select bit 0. Works in conjunction with bits 0, 1 and 2 above. See bond out description for pin 49 for more information. This bit only works in MASTER mode.	1
0	4	SYNC	Same as I/O pin 56, used only in MASTER mode. See BOND OUT table above for more information.	0
0	5	TM	Transfer Mode bit select – Reserved for future use	0
0	6	CS2	Clocks select bit 2. Works in conjunction with CS1, see bit 7 below.	0
0	7	CS1 CS2 CS1 0 0 – SR1 0 1 – SR2 1 0 – SR3 1 1 – SR4	Clock Select bit 1, in conjunction with CS2, selects the clock rate for pixel read out. Frequency is based on 40 MHz Master clock. Frequency will vary with varying Master clock. SR1 is 20Mhz. (Master clock/2) SR2 is 10Mhz. (Master clock/4) SR3 is 5Mhz. (Master clock/8) SR4 is 2.5Mhz. (Master clock/16)	0
0	8	CS0 CS0 - 0 250us CS0 - 1 1ms	Clock Select bit 0, selects time base for exposure control. Periods based on 40MHz Master input clock. Period will vary with varying Master clock. CS0 set to 0 selects 250us clock period (4 kHz). Max. integration is 1 second. CS0 set to 1 selects 1ms clock period (1 kHz). Max. integration is 4 seconds.	0
0	9	CDS1 CDS1 CDS0 0 0 – RM0 0 1 – RM1 1 0 – RM2 1 1 – RM3	Same as I/O pin 38, used only in MASTER mode. See BOND OUT table above for more information. Works in conjunction with bits 5 and 10. RM0 – unsupported mode RM1 – Rolling shutter, destructive readout RM2 – Snap Shot shutter, non-destructive readout RM3 – Snap Shot shutter, destructive read	1
0	10	CDS0	Same as I/O pin 39, used only in MASTER mode. See BOND OUT table above for more information. Works in conjunction with bits 5 and 9.	0
0	11	!STOP	STOP bit, this is a true low bit. When this bit is set to 0, the state machine logic will halt the device at the end of the next read cycle. The next cycle will occur when SYNC pin 56 is asserted (Asynchronous capture) When set to 1, the state machine allows continuos cycles.	0

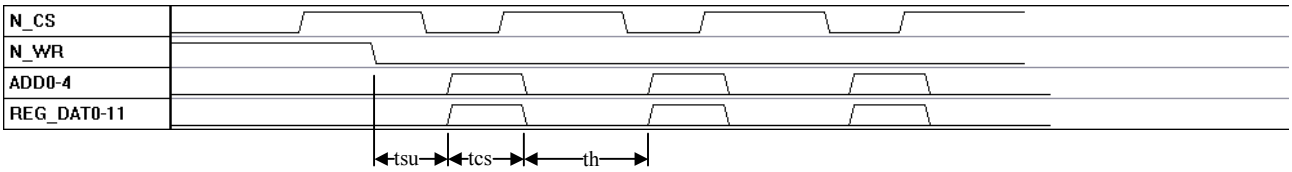
1	0	REV0	Device Revision. Bits 4,3,2,and 1 form the revision level for the device.	1
1	1	REV1		0
1	2	REV2		0
1	3	REV3		0
1	4	REV4		0
1	5	RSH	Rolling Shutter Holdoff enable bit. When set to 1, Holdoff is enabled.	0
1	6	AUX-BYPASS	Same as bond pad 35. When set to 1, the analog input that is connected to bond pad 71is digitized and output as the last pixel of each frame. When set to 0, the last pixel is digitized and output.	1
1	7	PAUSE	Same as I/O pin 46, used only in MASTER mode. See BOND OUT table above for more information.	0
1	8	C1	Same as I/O pin 40, used only in MASTER mode. See BOND OUT table above for more information.	0
1	9	C0	Same as I/O pin 41, used only in MASTER mode. See BOND OUT table above for more information.	0
1	10	R1	Same as I/O pin 42, used only in MASTER mode. See BOND OUT table above for more information.	0
1	11	R0	Same as I/O pin 43, used only in MASTER mode. See BOND OUT table above for more information.	0

TIMING DIAGRAM: SETUP REGISTER WRITE AND READ

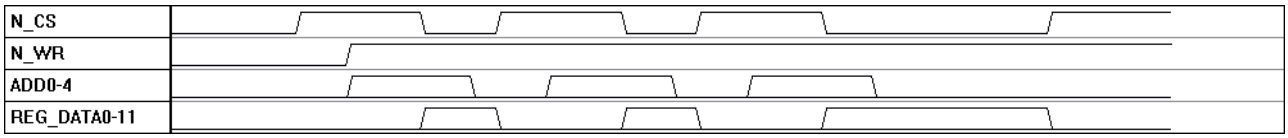
The following timing diagrams illustrate setup register writing and reading. It is important to note that the writing and reading of the setup registers is asynchronous, that is these operations are not clock dependant.
CAUTION: Do not change the state of N_WR whenever N_CS is low. Register reading and writing can only occur when the device is in MASTER mode. Note minimum pulse duration is 1 master clock pulse.

Note that a register write cycle will occur on the rising edge of N_CS while N_WR is low. A register read cycle occurs on the falling edge of N_CS whenever N_WR is high. Data is written to, or read from, the registers, within 50ps of the edge transition. This simplifies timing of signals to access the registers. You only must have valid address and data on the buses during a N_CS transition, therefore the timing diagrams below do not show actual times. For simplicity of operation, you can use the CLK1X as an event, if desired. For example, write the Address and data to the ADD and DATA buses, then while holding those values, on subsequent clocks, strobe the N_CS and N_WR lines.

WRITE CYCLE: Following shows 3 registers being written to. Apply valid address, 0-15(hex) to address bus lines ADD0-ADD4, and valid data (12 bits) to the REG_DATA bus, REG_DATA_0 - REG_DATA_11. Note diagram shows setting N_WR signal low only while N_CS is high.



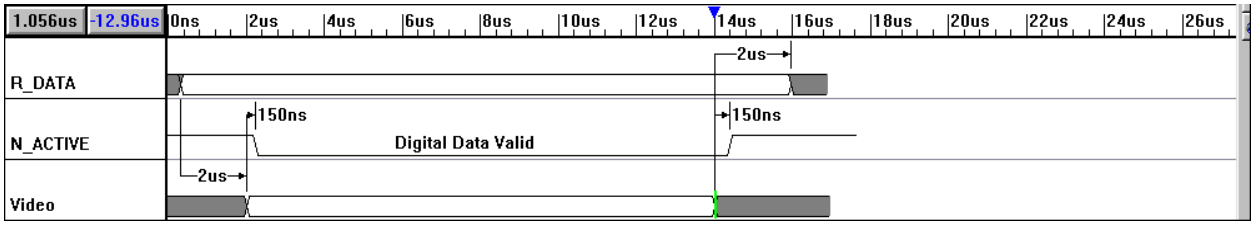
READ CYCLE: Following shows 3 successive register reads. Apply valid address, 0-15(hex) to address bus lines ADD0-ADD4. Data will be output to the REG_DATA Bus, REG_DATA_0 - REG_DATA_11 on the high to low transition of N_CS, and will remain valid until N_CS is taken high again. Note diagram shows setting N_WR signal high only while N_CS is high.
Minimum tsu – 5ns, Minimum tcs – 5ns, minimum th – 10ns. The maximum time for these signals is that the summation of all three must be less than one frame time.



VIDEO OUT TIMING DIAGRAMS:

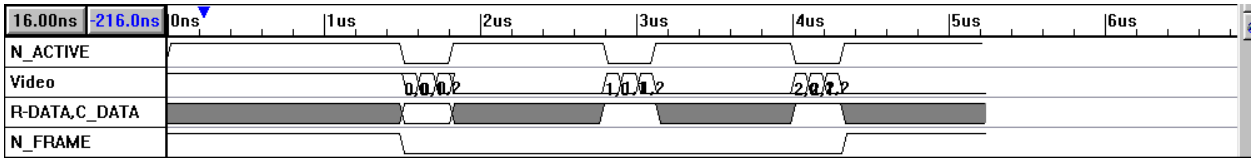
The following illustrates video output timing. Both the Analog out and the Digital out are shown. Note that at the end of every row read, whether within an ROI or entire frame, there is a 40 clock (CLK1X) delay where the video data is not valid. At 40MHz CLK_IN_2X, this corresponds to a 2 microsecond delay. The CLK1X signal is the pixel out clock.

Note that the video data, whether digital or analog, lags the column and row address by 5 CLK_IN_2X cycles. In other words, when the sixth pixel row and column address appears on the R_DATA and C_DATA buses (SLAVE or MASTER mode), the first pixels data is output on the video ports.



VIDEO ROW DATA TIMING DIAGRAM.

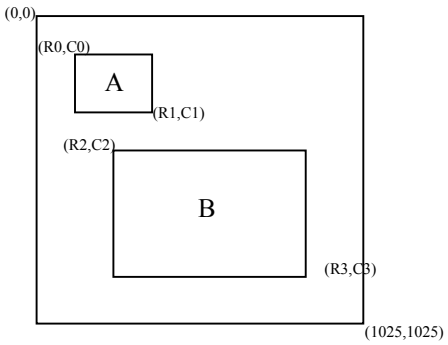
Diagram shows a few pixels selected. Times shown are based on input CLK2X frequency of 40MHz.



FRAME TIMING DIAGRAM

Diagram shows video output for a 3 by 3 ROI, again with a 40MHz CLK2X.

Region of Interest or sub-frame readout:
The two ROI's can be programmed anywhere on the array. If the a portion of the second region occupies the same rows as the first region, the video output of the shared rows of the second region will be invalid.



ROI Reg Set	Registers	Values
0	Row Start 0	R0
	Row Stop 0	R1
	Col Start 0	C0
	Col Stop 0	C1
1	Row Start 1	R2
	Row Stop 1	R3
	Col Start 1	C2
	Col Stop 1	C3

REGION OF INTEREST READOUT: Regions of Interest are read out in the order that they are programmed. Once a row stop value of zero is encountered, readout ends. The only delay between readouts is the regular retrace.

MODES OF OPERATION

FULL FRAME SNAPSHOT SHUTTER – DESTRUCTIVE READOUT

This mode captures an image by simultaneously integrating all pixels. After integration, all pixels are simultaneously transferred to the hold site. This cycle begins when SYNC line is asserted after the !STOP bit is released in synchronous mode, or immediately after the !STOP bit is released in asynchronous mode. The FFS HOLDOFF register and TRANSFER register count down and all pixels are held in reset until the FFS HOLDOFF register reaches zero, and then the pixels begin to integrate. Once the TRANSFER register reaches zero, all pixels are transferred to the hold site. Therefore the integration time is the difference between the FFS HOLDOFF and the TRANSFER registers in exposure clock periods as defined by CS0. The array is then read out progressively. If !STOP equals one, another cycle will begin. Otherwise, the device will halt until !STOP becomes one.

FULL FRAME SNAPSHOT SHUTTER – NON-DESTRUCTIVE READOUT

This mode operates in similar fashion to FFS mode described above, except that the pixels are read non-destructively. The cycle begins in the same manner as Full Frame Destructive, and pixels are sampled when the TRANSFER register reaches zero. All pixels are read out non-destructively, and therefore the CDS is disabled. Another cycle begins after the transfer register is reloaded if !STOP is one. If !STOP is not one, the machine will go halt when read out is completed.

ROLLING SHUTTER – DESTRUCTIVE READOUT

A cycle begins the same way as Full Frame Destructive, although this method samples one row at a time. Each row is read the same as Full Frame Destructive, but it is reset and unless a ROLLING HOLDOFF is set, begins integrating immediately after the reading. The rolling holdoff register can be used to prevent the image from becoming over-exposed. A row will not begin integrating again until an additional number of lines equal to the rolling holdoff register are read. As with the other modes, another cycle begins when !stop is one, and the machine goes idle when !stop is zero. If multiple regions of interest with a different number of pixels per row are used, the exposure for different ROIs will not be equal because of different line times for the multiple ROIs. The following equations can be used:

Exposure time = (number of lines – rolling holdoff)(line time)

Line time = (2 uSEC) + (pixels per line)(50 nSEC)

Active Column Sensor Series Pixel Operations

This is a review of pixel operations as allowed by ACS sensor configuration. Figure # 1, is representative of the pixel schematic of the ACS sensor. Normal pixel operation consists of a sequence of steps that involves resetting the pixel and the hold site, an integration period to accumulate the video signal, a sampling of the video signal and back ground information, and then starting the process again for the next frame of video. The order of steps may change and some steps may be repeated within a cycle, but the fundamental steps are included. There are three allowed operations for sensing the video signal. The first method, named "Rolling Shutter", the background is sampled on the Hold capacitor and then the pixel video value is transferred and re-sampled for KTC reduction. The second method named, "Electronic Shutter" is useful for freeze frame operations. In this method the video signal is sampled on the Hold capacitor to end exposure and store the video value and the pixel is reset and re-sampled for video background information. The third method, named "Adaptive Exposure Control" for nondestructive read operations, allowing the video to be sampled and re-sampled until the desired signal has accumulated, the pixel is then reset and re-read for video background information. Which method is utilized will depend on the application. The detailed discussion that follows will assist.

Before we begin the detailed discussion of the pixel operations, the pixel structure and its components will be described. All pixel operations are accomplished on a row-by-row or global basis. A row operation is defined as all pixels in a row as having the same signal or operation performed at the same time. A global operation is defined as the signal or operation is applied to all pixels on the array at the same time. All descriptions herein involve row operations unless otherwise noted. Referring to Figure # 1, at the top of the drawing is the dual gate Select FET of the Active Column Sensor (ACS). This dual gate FET has the dual purpose of selecting a row of pixels as well as sensing the accumulated charge within the pixel. The Row Select line turns each row of Select FETs "on". The select FET is part of a Unity Gain Amplifier, with the remainder of the UGA located at each column and is the reason that the source and drain of the Select FET run the length of the column of pixels. The UGA configuration per pixel eliminates the pixel to pixel variations known as Fixed Pattern Noise that plague other image sensors. The next FET below the Select FET is the Hold FET that is controlled by the Hold Select line. When the Hold FET is selected or turned "on" and turned back "off", or deselected, the value in the pixel photodiode is sampled and stored on the capacitor. The value stored could either be the reset value the pixel is reset to or the accumulated pixel value after the pixel has integrated light for a given time period. When the row is selected and the Hold FET is deselected the value stored in the capacitor is the value sensed by the UGA. The next FET is the Bias FET, when selected biases the Pixel to the reset value via the Rest Bias line.

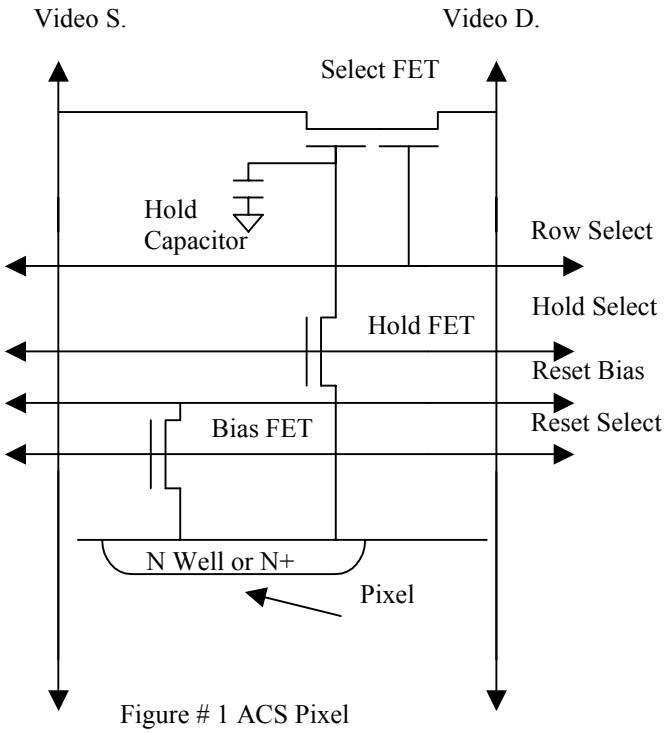


Figure # 1 ACS Pixel

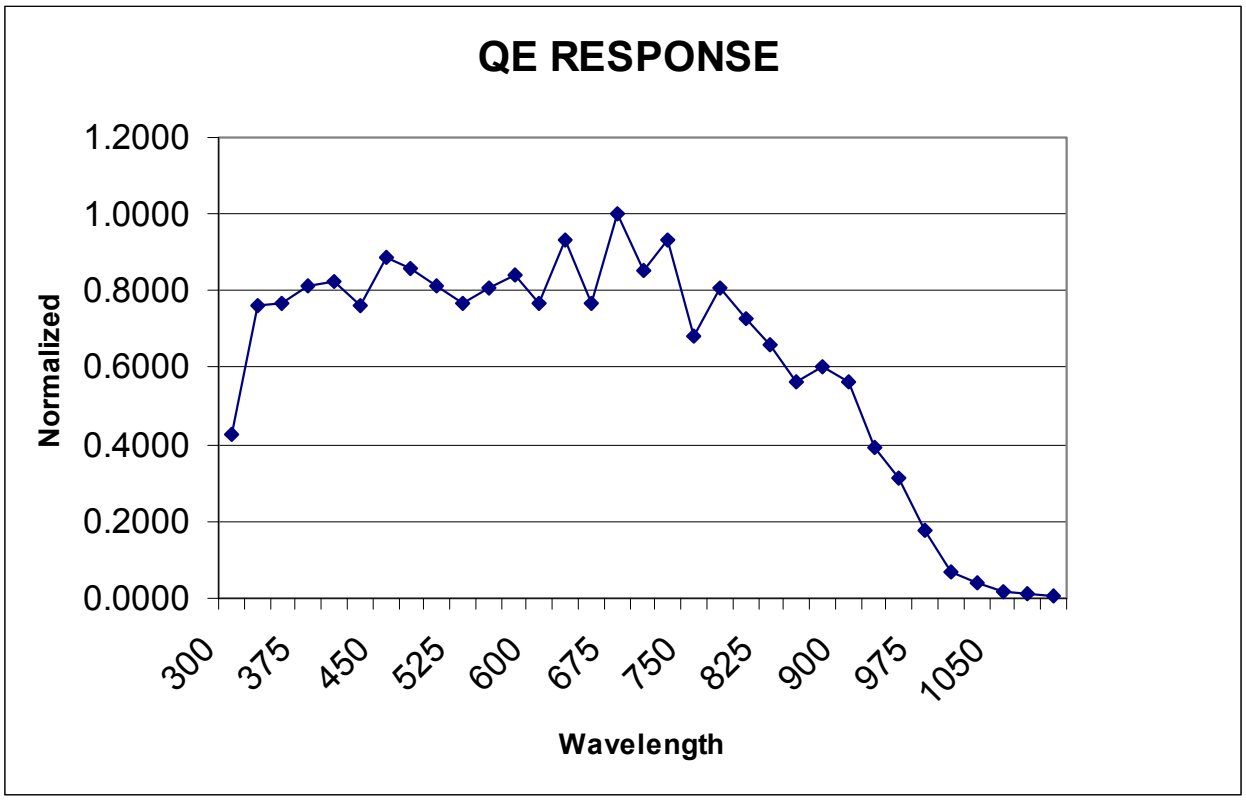
In more detail the "Rolling Shutter" method described above allows for KTC noise reduction. This read-out method starts with the Hold FET and the Bias FET selected. This allows for the pixel and the capacitor to be reset to the initial reset bias. The Bias FET and the Hold FET are subsequently released or deselected. The pixel is allowed to integrate for one frame time and the row is selected for reading. The value in the Hold capacitor that was set to the initial reset values is read first. The Hold FET is selected, allowing the Pixel value to be read next. The reset and pixel values are subtracted from each other for virtually pattern noise free video. The process is repeated from frame to frame in normal rolling shutter video and the same can be accomplished in a global frame sequence. Reading or sensing are used interchangeably for the ACS sensors as the accumulated pixel signal is only sensed when read. The signal isn't destroyed as in Charge Coupled Devices (CCDs) and in effect is only sensed and left undisturbed for further reading allowing noise elimination or

continued signal accumulation for optimal image contrast. The “sensing” of the pixel signal is a key advantage over CCDs.

Electronic shutter allows video to be temporarily stored on the Hold capacitor. The sequence starts with the Hold FET and the Reset FET turned “on” to bias both the Hold capacitor and the pixel to the same level. The Reset FET and the Hold FET are turned “off”. The pixel is allowed to integrate. The Hold FET is selected, the video on the pixel is sampled, and the Hold FET is turned “off” or deselected. When the row is selected for reading, the Row FET is selected and the stored video is read. Then, the Rest FET and Hold FET are selected, re-biasing the pixel to the reset value and both are turned off. The rest value is sampled and subtracted for pattern noise free video.

The “Adaptive Exposure Control” method describes Non Destructive Read Out (NDRO) for ACS sensors. The pixels are biased to the reset value by selecting and deselecting the Hold FET and Reset FET as previously described. The pixels are allowed to integrate. The Hold FET is selected and deselected for sampling the pixel value. The value is read for optimal signal levels. If more integration is desired the pixels are allowed to integrate longer and pixel value is re-sampled by selecting and deselecting the Hold FET. When the desired signal level has been achieved, a row is selected for reading by selecting the Select FET and sampling the video by selecting and deselecting the Hold FET. The Hold and Bias FETs are then Selected and deselected to re-bias the pixels the reset value and the back ground.

These are the standard methods allowed and controlled internally by the ACS sensors series. If the imager is operated in the slave mode, greater operator control allows more flexibility, to minimize the number of operations performed per frame of Video and potentially reduce the associated noise generated.



DEVICE PACKAGING OPTIONS:

The device is available in 2 packaging options:

1. PGA – Ceramic Pin Grid Array with glass lid., 144 pins. See drawing 40016, sheets 1-3, below. P/N ACS-I XXXX-CPGA. This package option valid for ACS-I 512 and 1024 only.
2. Polymer package with glass lid, SMD with 132 pads, P/N ACS-I XXXX-POLY. Valid for ACS-I 512 and ACS-I 1024 only.

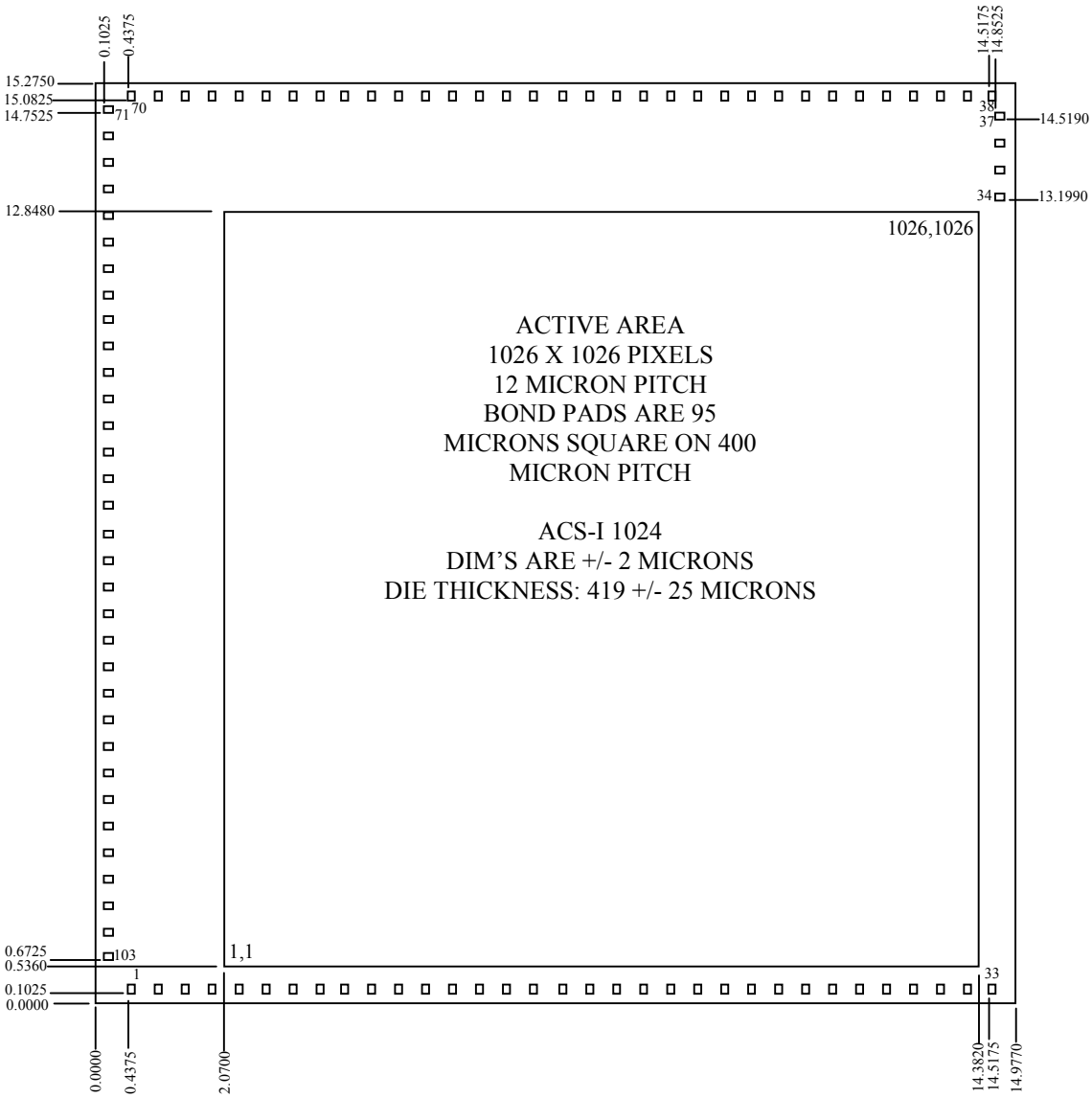
ACS-1024 DIE OUTLINE

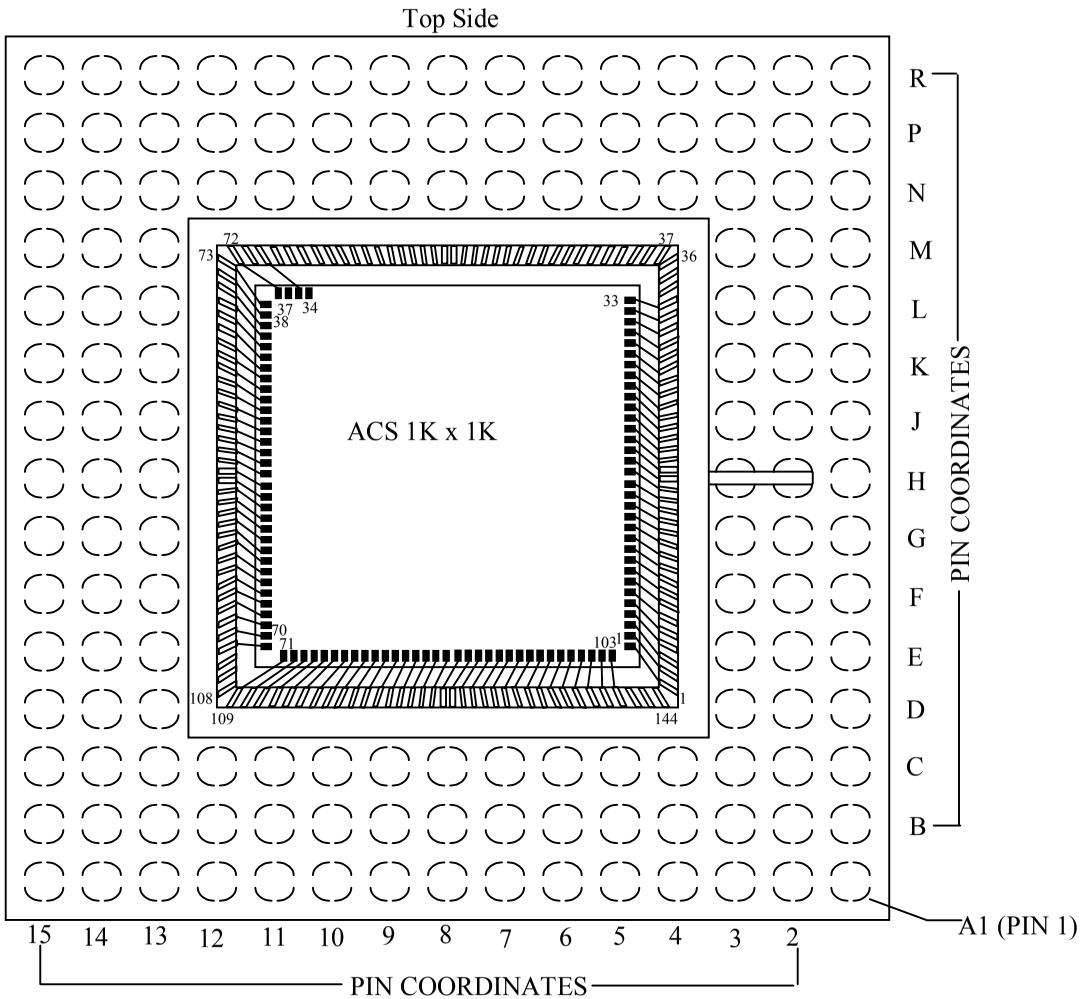
Drawing #: 40017 Rev: 1

Originator: **Date:**

Checked: **Date:**

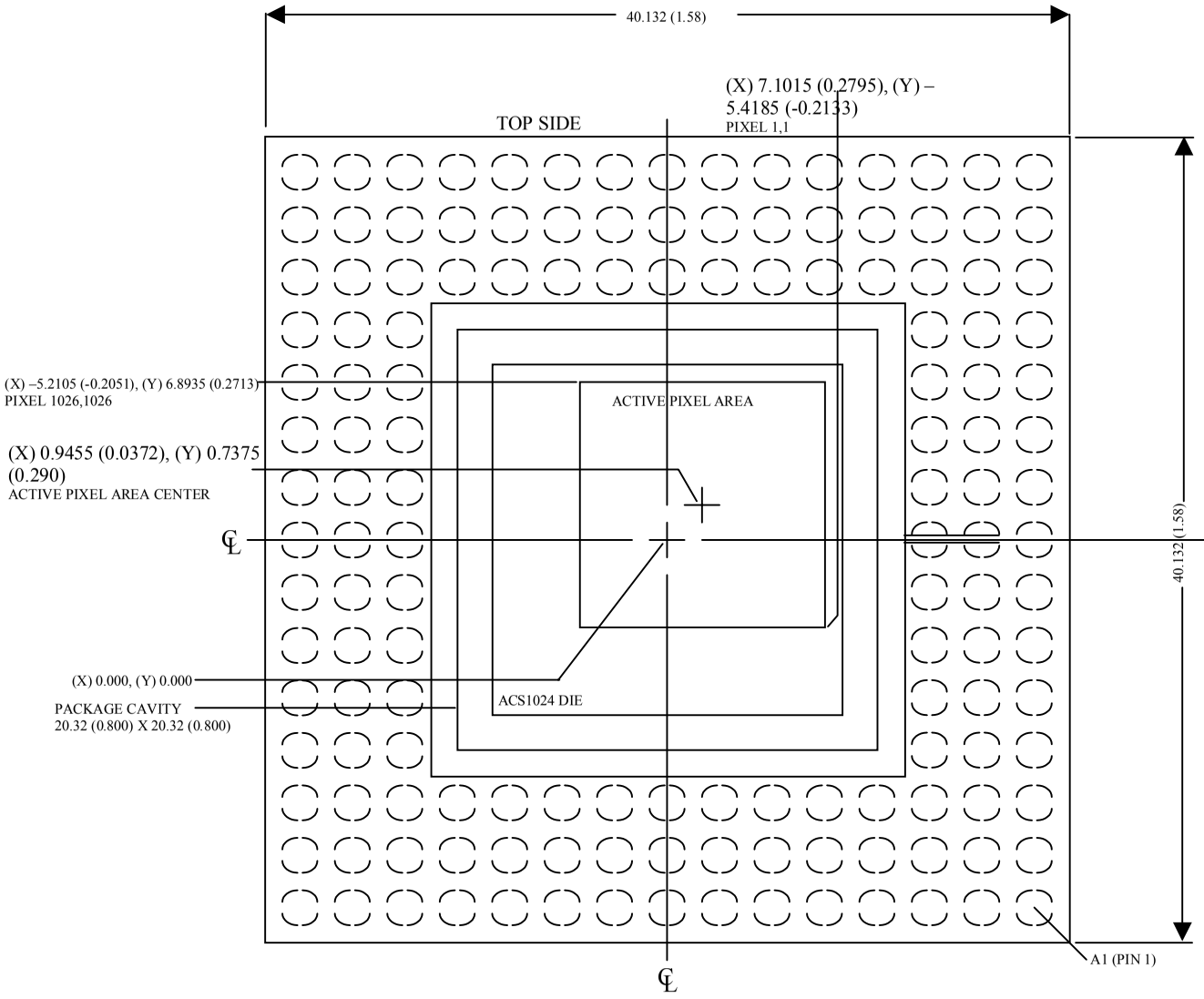
Approved: **Date:**

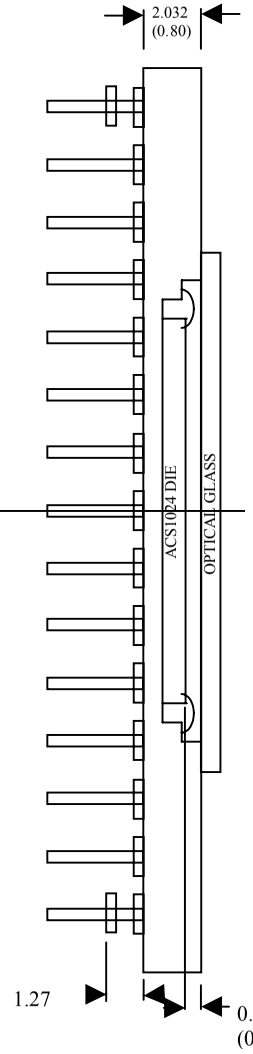




Notes:
1. Package is a 144 pin PGA, 15x15 grid.
2. Pins arrayed on a 2.54 (0.100) grid.
3. Pins located on bottom side.
4. Detail CPGA package info see:
KYOCERA CORP.
DRAWING KD-P86499-B

Tolerances
Dimensions and tolerating in accordance with ASME Y14.5M-1994. All untoleranced dimensions are basic unless otherwise specified. All dimensions are in inches.





Notes:
1. Active Pixel Area: 12312 x 112312 microns
2. See drawing 40017 for die details
3. Die located within +/- (TBD)
4. Detail CPGA package info see: KYOCERA CORP. DRAWING KD-P86499-B
5. Dimensions in millimeters and (inches).
6. Die thickness 419 +/- 25 microns, paste thickness for die mounting TBD.

Tolerances
Dimensions and tolerating in accordance with ASME Y14.5M-1994. All untoleranced dimensions are basic unless otherwise specified. All dimensions are in millimeters.

ACS-XXX-CPGA Package pin-out table

ACS 1K X 1K CPGA PACKAGE

Drawing #: 40016 Rev: 1

Originator: Date:

Checked: Date:

Approved: Date:

Die Bond to Package Bond to Package Pinout

DIE PAD	NAME	PGA BOND PAD	PGA PIN	DIE PAD	NAME	PGA BOND PAD	PGA PIN	DIE PAD	NAME	PGA BOND PAD	PGA PIN
1	REG_DATA_5	1	D3	36	NOT BONDED	71	P14	71	ANALOG_IN	109	C12
2	REG_DATA_6	2	C2	37	EXT_ANALOG_SELECT	72	R15	72	DIG_PAD_PWR	110	B13
3	REG_DATA_7	3	B1	38	CDS1	73	M13	73	DIG_PWR	111	A14
4	REG_DATA_8	4	D2	39	CDS0	74	N14	74	DIG_GB_PWR	112	B12
5	REG_DATA_9	5	E3	40	C1	75	P15	75	DIG_PAD_GND	113	C11
6	REG_DATA_10	6	C1	41	C0	76	M14	76	DIG_GND	114	A13
7	REG_DATA_11	7	E2	42	R1	77	L13	77	ADD0	115	B11
8	DIG_PAD_PWR	8	D1	43	R0	78	N15	78	ADD1	116	A12
9	DIG_PAD_GND	9	F3	44	CRST	79	L14	79	ADD2	117	C10
10	C_DATA_0	10	F2	45	RESET	80	M15	80	ADD3	118	B10
11	C_DATA_1	11	E1	46	PAUSE	81	K13	81	ADD4	119	A11
12	C_DATA_2	12	G2	47	MASTER	82	K14	82	CLK_IN_2X	120	B9
13	C_DATA_3	13	G3	48	GAIN1	83	L15	83	CLK1X	121	C9
14	C_DATA_4	14	F1	49	GAIN0	84	J14	84	N_ACTIVE	122	A10
15	C_DATA_5	15	G1	50	OFFSET1	85	J13	85	N_FRAME	123	A9
16	C_DATA_6	16	H2	51	OFFSET0	86	K15	86	DIG_PAD_PWR_3.3	124	B8
17	C_DATA_7	17	H1	52	DIG_PAD_GND	87	J15	87	DIG_PAD_GND_3.3	125	A8
18	C_DATA_8	18	H3	53	DIG_PAD_PWR	88	H14	88	DIG_DATA_ENA	126	C8
19	C_DATA_9	19	J3	54	N_CS	89	H15	89	DATA_0_LSB	127	C7
20	C_DATA_10	20	J1	55	N_WR	90	H13	90	DATA_1	128	A7
21	C_DATA_11	21	K1	56	SYNC	91	G13	91	DATA_2	129	A6
22	R_DATA_0	22	J2	57	TX	92	G15	92	DATA_3	130	B7
23	R_DATA_1	23	K2	58	COL_LOAD	93	F15	93	DATA_4	131	B6

24	R_DATA_2	24	K3
25	R_DATA_3	25	L1
26	R_DATA_4	26	L2
27	R_DATA_5	27	M1
28	R_DATA_6	28	N1
29	R_DATA_7	29	M2
30	R_DATA_8	30	L3
31	R_DATA_9	31	N2
32	R_DATA_10	32	P1
33	R_DATA_11	33	M3
34	NOT BONDED	69	N12
35	LAST_PIXEL_OUT	70	N13

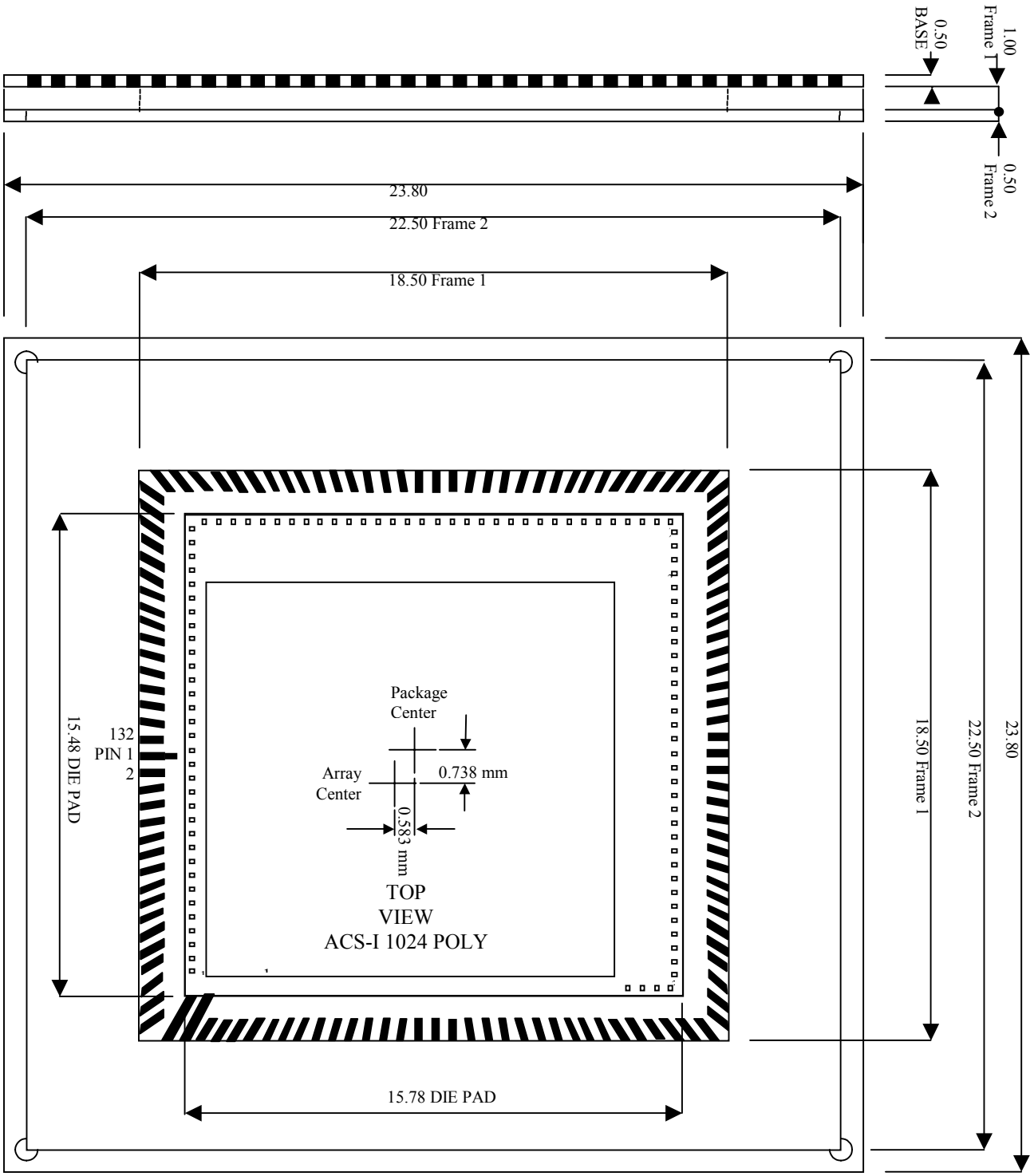
59	ROW_LOAD	94	G14
60	GB_ANA_GND	95	F14
61	ANA_GND2	96	F13
62	ANA_GND1	97	E15
63	ANA_PAD_GND	98	E14
64	GB_ANA_PWR	99	D15
65	ANA_PAD_PWR	100	C15
66	PIX_AMP_ANA_PWR	101	D14
67	ANA_PWR1	102	E13
68	ANA_PWR2	103	C14
69	ANALOG_OUT	104	B15
70	BIAS_PD_EXT	105	D13

94	DATA_5	132	C6
95	DATA_6	133	A5
96	DATA_7	134	B5
97	DATA_8	135	A4
98	DATA_9	136	A3
99	REG_DATA_0	137	B4
100	REG_DATA_1	138	C5
101	REG_DATA_2	139	B3
102	REG_DATA_3	140	A2
103	REG_DATA_4	141	C4

-POLY PACKAGE

Notes:

1. Dimensions in millimeters unless otherwise indicated.
2. Dimension tolerances are +/- 0.2 mm.
3. Die placement rotational error is +/- 0.5 degrees.
4. See Die drawing above for die dimension details.
5. Drawing shown for ACS-I 1024. Drawing for ACS-I 512 and ACS-I 2048 not available at this time.



POLY PACKAGE PINOUT

PIN	BOND	PIN	BOND	PIN	BOND	PIN	BOND	PIN	BOND	PIN	BOND
1	17	23	NC	45	NC	67	54	89	76	111	98
2	18	24	NC	46	NC	68	55	90	77	112	99
3	19	25	NC	47	34	69	56	91	78	113	100
4	20	26	NC	48	35	70	57	92	79	114	101
5	21	27	NC	49	36	71	58	93	80	115	102
6	22	28	NC	50	37	72	59	94	81	116	103
7	23	29	NC	51	38	73	60	95	82	117	1
8	24	30	NC	52	39	74	61	96	83	118	2
9	25	31	NC	53	40	75	62	97	84	119	3
10	26	32	NC	54	41	76	63	98	85	120	4
11	27	33	NC	55	41	77	64	99	86	121	5
12	28	34	NC	56	43	78	65	100	87	122	6
13	29	35	NC	57	44	79	66	101	88	123	7
14	30	36	NC	58	45	80	67	102	89	124	8
15	31	37	NC	59	46	81	68	103	90	125	9
16	32	38	NC	60	47	82	69	104	91	126	10
17	33	39	NC	61	48	83	70	105	92	127	11
18	SG	40	NC	62	49	84	71	106	93	128	12
19	SG	41	NC	63	50	85	72	107	94	129	13
20	NC	42	NC	64	51	86	73	108	95	130	14
21	NC	43	NC	65	52	87	74	109	96	131	15
22	NC	44	NC	66	53	88	75	110	97	132	16

NOTES:

1. SG – Substrate Ground
2. NC – No Connection