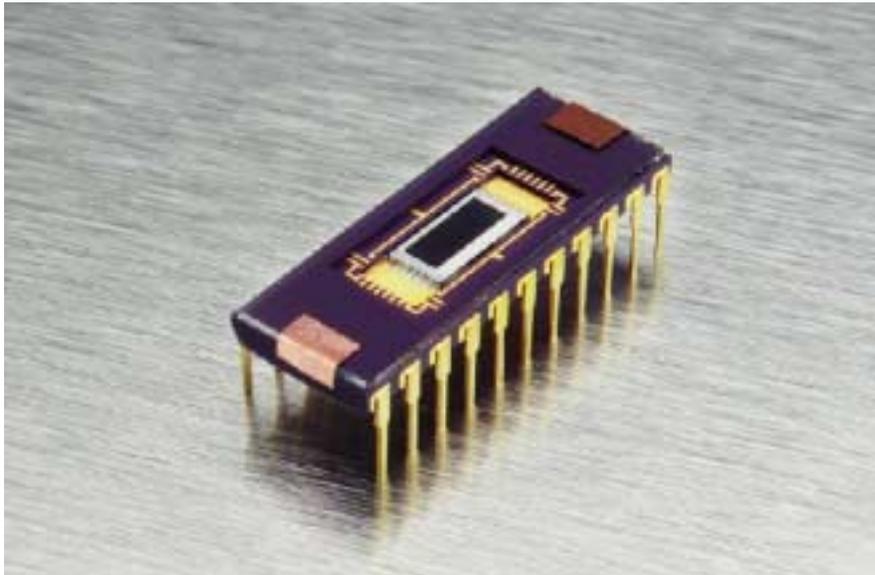


**RETICON®**

# L-Series Linear CMOS Spectroscopy Sensor

25 or 50  $\mu\text{m}$  pitch, 2.5 mm aperture, 128 to 1024 elements

## Description

The PerkinElmer L-series of monolithic self-scanning linear photodiode arrays offers a high quality, low cost solution for spectroscopy and colorimetry applications in the 300 – 1000 nm range. The combination of high sensitivity, low dark current, low switching noise and high saturation charge of the L-series provides excellent dynamic range and great flexibility in setting integration time.

L-series sensors consist of a linear array of silicon photodiodes, each connected to a MOS switch for readout controlled by an integrated shift register scanning circuit. Under external clock control, the shift register sequentially enables each of the switches directing the charge on the associated photodiode to an output line. A dummy output provides clock noise cancellation. The L-series devices are mounted in ceramic side-brazed 22-pin dual-inline packages with ground and polished fused silica windows and are pin-compatible with earlier PerkinElmer SB and TB series sensors.

## Features

- 128, 256, 512 or 1024 photodiode elements with 25  $\mu\text{m}$  center-to-center spacing
- 128, 256 or 512 photodiode elements with 50  $\mu\text{m}$  center-to-center spacing
- 2.5 mm photodiode aperture
- Extremely low dark leakage current
- Low power dissipation
- Clock-controlled sequential readout at rates up to 1 MHz
- Single-supply operation with HCMOS-compatible inputs
- Single shift register design
- Wide dynamic range
- Differential video output for clock noise cancellation
- High saturation charge 10 pC (25  $\mu\text{m}$ ) or 20 pC (50  $\mu\text{m}$ )
- Antiblooming function for low crosstalk
- Line Reset Mode for simultaneous reset of all photodiodes
- Wide spectral response: 300 to 1000 nm
- Polished fused silica window
- On-chip diodes (two) for temperature monitoring

Caution: While the L-Series imagers have been designed to resist electrostatic discharge (ESD), they can be damaged from such discharges. Always observe proper ESD precautions when handling and storing these sensors.



# CMOS Spectroscopy Sensor

## Sensor Characteristics

The L-series self-scanning photodiode arrays are supplied in two versions to meet broad application requirements. The models with 25  $\mu\text{m}$  diode spacing are applied primarily where a compact array is needed while the 50  $\mu\text{m}$  models accommodate applications requiring the highest dynamic range. Both types are available in 128, 256 and 512 pixel lengths and the 25  $\mu\text{m}$  models also include a 1024 pixel version.

The simplified equivalent circuit of an L-series sensor photodiode array is shown in Figure 1. Each cell consists of an active photodiode and a dummy photodiode, both with an associated junction capacitance. These diodes are connected through MOS multiplex switches to active and dummy video lines. The shift register is driven by complementary square wave clocks with periodic start pulses being introduced to initiate each scan. The pixel sampling rate is determined by the clock frequency. Integration time is the interval between start pulses. The output signal obtained from each scan of an N-element array is a train of N charge pulses, each proportional to the light exposure on the corresponding photodiode. In addition to the signal charge, switching transients are capacitively coupled into the active video lines by the multiplex switches. Similar transients are introduced into the dummy video lines and, therefore, can be reduced by reading out the video and dummy lines differentially.

In all models, the diodes are contiguous to collect the maximum amount of incoming light. Charge generated by light incident on the p-type surface between two n-regions will divide between the adjacent diodes to produce the response function shown in Figure 2. The 6  $\mu\text{m}$  interdiode gap is maintained in all models to provide a uniform aperture response function across the product line.

The quantum efficiency of all models is shown in Figure 3. The smooth curve is the basic response of the photodiode array showing a peak quantum efficiency approximately 60% at 650 nm.

Figure 1. Equivalent Circuit

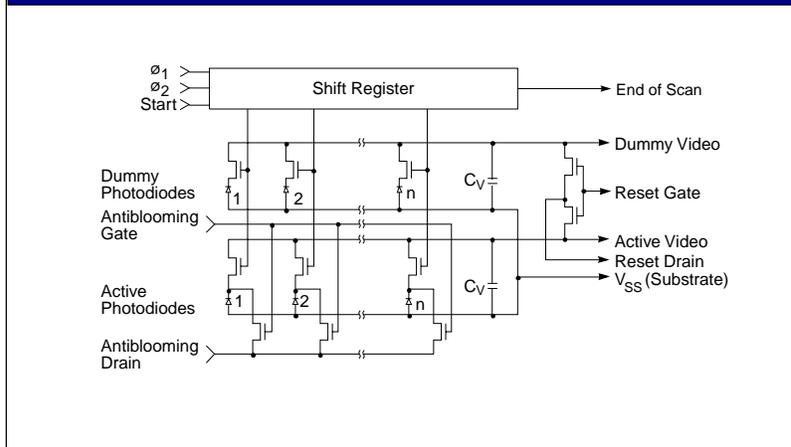


Figure 2. Sensor Geometry and Aperture Response Function

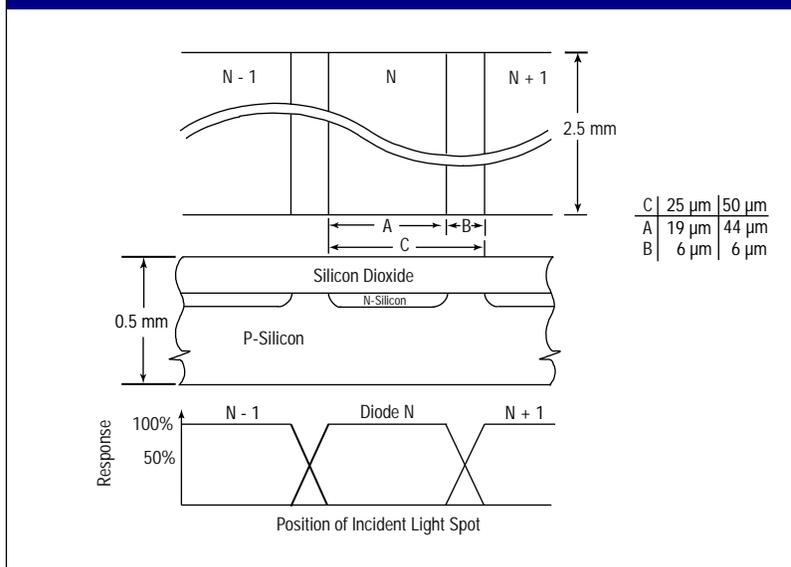
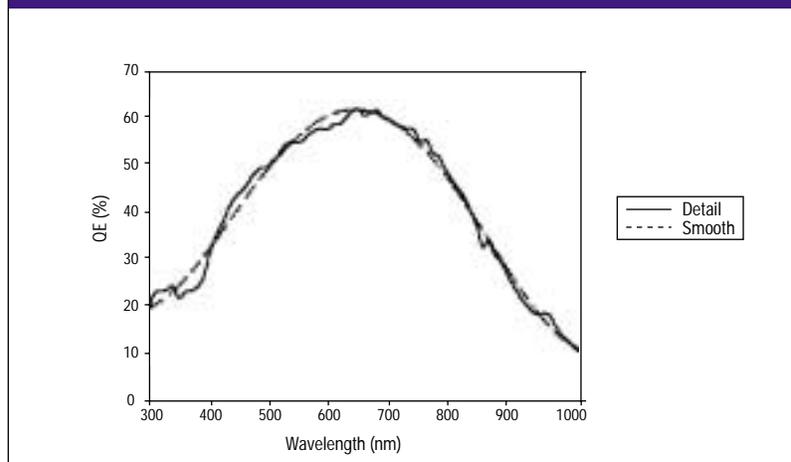


Figure 3. Quantum Efficiency



## Sensor Characteristics (contd.)

Interference effects in the transparent passivation layer over the diodes modulate this response. Since the details of this modulation can vary from sensor to sensor, the curve shown should be taken only as representative of the short-term wavelength-dependent variation in quantum efficiency. The detail curve was taken at 10 nm intervals while the smoothed curve represents an average over a bandwidth of approximately 100 nm.

Figure 4 shows the typical output charge as a function of exposure at 650 nm wavelength for the 25 and 50  $\mu\text{m}$  pitch models. Exposure in  $\text{nJ}/\text{cm}^2$  is calculated by multiplying the irradiance in  $\mu\text{W}/\text{cm}^2$  by the integration time in msec. The response is very linear up to the saturation charge - 10 pC in 25  $\mu\text{m}$  models and 20 pC in the 50  $\mu\text{m}$  models. The dark current of an L-series sensor at 25°C is typically 0.2 pA for the 25  $\mu\text{m}$  models or 0.4 pA for the 50  $\mu\text{m}$ , doubling for every 7°C increase in temperature. See Table 2 for detailed electro-optical characteristics.

## Clock and Voltage Requirements

Scanning is achieved by means of an integrated shift register. The shift register is driven by complementary square wave clocks,  $\emptyset_1$  and  $\emptyset_2$ . Table 1 gives rise and fall times and crossover points for these clock waveforms. The clock amplitude should be equal to  $V_{\text{DD}} - V_{\text{SS}}$ . With  $V_{\text{DD}} = 5\text{ V}$  and  $V_{\text{SS}} = 0\text{ V}$ , the clock inputs will be HCMOS-compatible. Since each photodiode is read out on a negative transition of  $\emptyset_2$  (see Figure 6), the frequency of the clock signal should be set equal to the desired video data rate.

The start pulse of similar amplitude to the clocks is required to load the shift register and initiate each readout period (each scan of the array). The start pulse is loaded when  $\emptyset_2$  is high; the start signal is pulsed high for a minimum of 10 ns during one and only one  $\emptyset_2$  clock high cycle. A timing diagram for the start and clock signals is shown in Figure 6. Caution:  $\emptyset_1$  and  $\emptyset_2$  clocks need to be continuously applied to the

Table 1. Electrical Characteristics (25 C)

(All voltages measured with respect to $V_{\text{SUB}}$ )					
Signal	Sym	Min	Typ	Max	Units
$V_{\text{DD}}$	$V_{\text{DD}}$	4.5	5	5.5	V
$V_{\text{DD}}$ guard	$V_{\text{DDG}}$	-	$V_{\text{DD}}$	-	V
$V_{\text{SS}}$	$V_{\text{SS}}$	-	0	-	V
$V_{\text{SUB}}$	$V_{\text{SUB}}$	-	0	-	V
Antiblooming drain					
RL12xx	$V_{\text{ABD}}$	$V_{\text{DD}}/2 - 0.1$	-	$V_{\text{DD}}/2$	V
RL15xx	$V_{\text{ABD}}$	$V_{\text{DD}} - 0.1$	-	$V_{\text{DD}}$	V
Start	$V_{\text{SH}}$ High	$V_{\text{DD}} - 0.1$	-	$V_{\text{DD}}$	V
	$V_{\text{SL}}$ Low	$V_{\text{SS}}$	-	$V_{\text{SS}} + 0.4$	V
Clock $\emptyset_1, \emptyset_2$	$V_{\text{H1}}, V_{\text{H2}}$ High	$V_{\text{DD}} - 0.1$	-	$V_{\text{DD}}$	V
	$V_{\text{L1}}, V_{\text{L2}}$ Low	$V_{\text{SS}}$	-	$V_{\text{SS}} + 0.4$	V
Reset gate <sup>2</sup>	-	-	$V_{\text{SS}}$	-	V
Antiblooming gate					
RL12xx	$V_{\text{HABG}}$ High	$V_{\text{DD}} - 0.1$	-	$V_{\text{DD}}$	V
	$V_{\text{LABG}}$ Low	$V_{\text{SS}}$	-	$V_{\text{SS}} + 0.4$	V
RL15xx	$V_{\text{HABG}}$ High	$V_{\text{DD}} - 0.1$	-	$V_{\text{DD}}$	V
	$V_{\text{LABG}}$ Low	-3.0	-	-2.0	V
Video bias					
RL12xx	$V_{\text{V}}$	2	$V_{\text{DD}}/2$	$V_{\text{DD}} - 2$	V
RL15xx	$V_{\text{V}}$	4.5	$V_{\text{DD}}$	5.5	V
Reset drain <sup>2</sup>	$V_{\text{RD}}$	-	$V_{\text{SS}}$	-	V
Clock rate	-	0.001	-	1	MHz
Start rise time	$t_{\text{RS}}$	-	10	50	ns
Start fall time	$t_{\text{FS}}$	-	10	50	ns
Start pulse width	$t_{\text{PWS}}$	10	-	-	ns
$\emptyset_1$ Rise time	$t_{\text{R1}}$	-	10	20	ns
$\emptyset_1$ Fall time	$t_{\text{F1}}$	-	10	20	ns
$\emptyset_2$ Rise time	$t_{\text{R2}}$	-	10	20	ns
$\emptyset_2$ Fall time	$t_{\text{F2}}$	-	10	20	ns
Video delay time	$t_{\text{VD}}$	-	20	-	ns
Clock crossing	$X_1$	0	-	50	%
	$X_2$	0	-	50	%
Capacitance $\emptyset_1, \emptyset_2$ at 5 V bias					
RL1201	$C_{\text{C}}$	-	9	-	pF
RL1202	$C_{\text{C}}$	-	50	-	pF
RL1205	$C_{\text{C}}$	-	77	-	pF
RL1210	$C_{\text{C}}$	-	154	-	pF
RL1501	$C_{\text{C}}$	-	30	-	pF
RL1502	$C_{\text{C}}$	-	48	-	pF
RL1505	$C_{\text{C}}$	-	93	-	pF
Capacitance, each video line at 2.5 V bias <sup>1</sup>					
RL1201	$C_{\text{V}}$	-	6.7	-	pF
RL1202	$C_{\text{V}}$	-	10.2	-	pF
RL1205	$C_{\text{V}}$	-	15.4	-	pF
RL1210	$C_{\text{V}}$	-	28.7	-	pF
Capacitance, each video line at 5.0 V bias <sup>1</sup>					
RL1501	$C_{\text{V}}$	-	9.1	-	pF
RL1502	$C_{\text{V}}$	-	14	-	pF
RL1505	$C_{\text{V}}$	-	25	-	pF

Notes:

1. Measured.

2. Clocking of Reset Gate may decrease dynamic range.

# CMOS Spectroscopy Sensor

## Clock & Voltage Requirements (contd.)

sensor. The integration period should be controlled by varying the time between start pulses. For optimum performance and minimum switching noise, it is important that the clocks are exact complements and that their rise and fall times comply with Table 1. A recommended circuit for generating these clocks is shown in Figure 7.

## End of Scan

An output pulse useful primarily for test purposes is provided two clock cycles after the last photodiode is sampled by the shift register scanning circuit. The timing of the EOS output is shown in Figure 6. The voltage levels on the EOS output will be determined by the  $V_{DD}$  and  $V_{SS}$  voltage levels supplied to the photodiode array. When  $V_{DD}$ s at +5V and  $V_{SS}$  is operated at 0 V, the EOS output will be compatible with the HCMOS family of logic devices.

## Amplifier Requirements

The recommended amplifier circuit for use with an L-series sensor is a simple current amplifier. A current amplifier holds the video line at a virtual ground and senses the current pulses flowing into the video line to recharge the diodes through their respective multiplex switches as they are sampled in sequence. These current pulses, which each can contain a charge up to saturation, are converted to a train of voltage pulses corresponding to the light intensity on the various diodes. In this mode of operation, the current amplifier must provide a positive bias voltage to the video line since the photodiode anode (the p-substrate) is biased to 0 V ( $V_{SS}$ ). Figure 8 shows a differential recharge amplifier suitable for use with L-series sensors.

## Line Reset / Antiblooming Control

Under certain operating conditions, it may be desirable to control integration time independent of the line scan time (time between start pulses). This can be accomplished by the use of the antiblooming gate control input. When the antiblooming gate is held high, all photodiodes are simultaneously

**Table 2. Electro-Optical Characteristics (25°C)**

Characteristic	Typ	Max	Units
Center-to-center spacing			
RL12xx	25	-	μm
RL15xx	50	-	μm
Sensitivity <sup>1,2</sup>			
RL12xx	$2 \times 10^{-4}$	-	C/J/cm <sup>2</sup>
RL15xx	$4 \times 10^{-4}$	-	C/J/cm <sup>2</sup>
PRNU <sup>2,3,4</sup>	5	10	±%
Saturation exposure ( $E_{SAT}$ ) <sup>1,2</sup>			
RL12xx	50	-	nJ/cm <sup>2</sup>
RL15xx	50	-	nJ/cm <sup>2</sup>
Saturation charge ( $Q_{SAT}$ ) <sup>5</sup>			
RL12xx	10	-	pC
RL15xx	20	-	pC
Dynamic range			
( $Q_{SAT} / Q_{NOISE(RMS)}$ )			
RL12xx	70,000	-	-
RL15xx	100,000	-	-
Average dark current <sup>6</sup>			
RL12xx	0.20	0.50	pA
RL15xx	0.40	1.0	pA
Spectral response peak	650	-	nm
Spectral response range	300-1000	250-1050	nm

Notes:

1. Measured at specified video line bias.
2. Average 600-700 nm, includes 8% window loss.
3. Photo response non-uniformity (PRNU) is defined as:
  - a.  $+ \% = (V_{MAX} - V_{AVG}) / V_{AVG} \times 100\%$
  - b.  $- \% = (V_{AVG} - V_{MIN}) / V_{AVG} \times 100\%$  where
    - i.  $V_{MAX}$  is the output of the pixel closest to saturation level.
    - ii.  $V_{MIN}$  is the output of the pixel closest to the dark level.
    - iii.  $V_{AVG}$  is the average of all array pixel outputs.

The first and last pixels are not counted in this measurement.
4. Measured at an exposure level of  $E_{SAT}/2$ .
5. Minimum  $Q_{SAT}$  for RL15xx is 15 pC; RL12xx is 8 pC.
6. Maximum dark current  $\leq 1.5 \times$  average dark current.

**Table 3. Absolute Maximum Ratings**

	Min	Max	Units
Voltage applied to any terminal with respect to $V_{SS}$	0	+10	V
Storage or operating temperature	-78	+85	°C

reset to the bias voltage on the anti-blooming drain (typically  $V_{DD}/2$ ). Conversely, when the antiblooming gate is held low, the antiblooming transistor is off and the photodiodes can then integrate photocurrent. Thus, when an active high pulse is applied to VABG, the integration time for diode "N" then becomes the time between the negative-going transition of the anti-

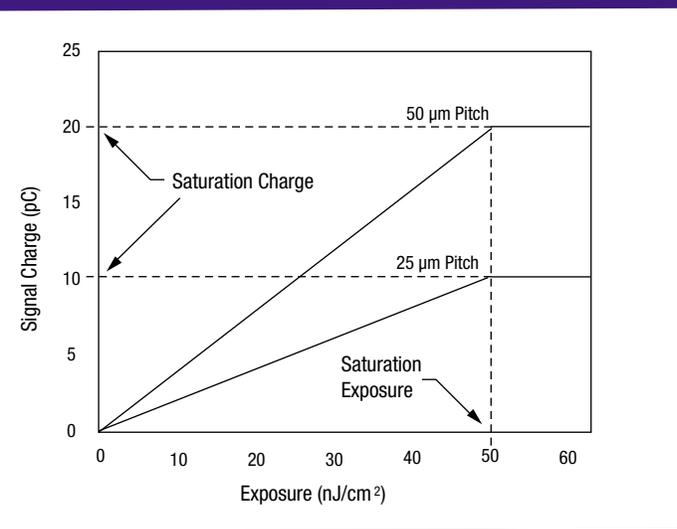
blooming gate to the time in which diode "N" is read out through the diode multiplex switch. Under normal operating conditions, the L-series sensors do not require antiblooming control due to excellent antiblooming characteristics. However, under extremely high exposure conditions, antiblooming control can be implemented to further enhance this performance. In this mode of

# CMOS Spectroscopy Sensors

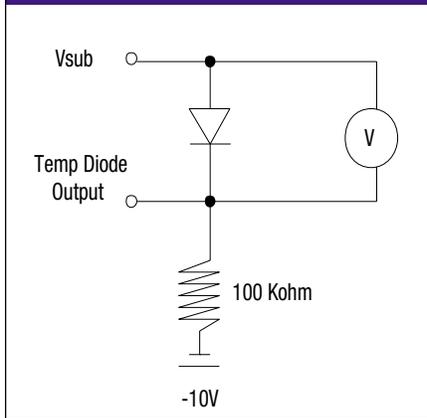
## Line Reset / Antiblooming Control (contd.)

operation, a bias voltage (the same voltage as the video line bias, typically  $V_{DD}/2$ ) is applied to the antiblooming drain. The antiblooming drain is then biased to 1 - 3 V above  $V_{LABG}$ . By adjusting the bias level on the antiblooming gate, excess charge present on the video line is shunted to the antiblooming drain.

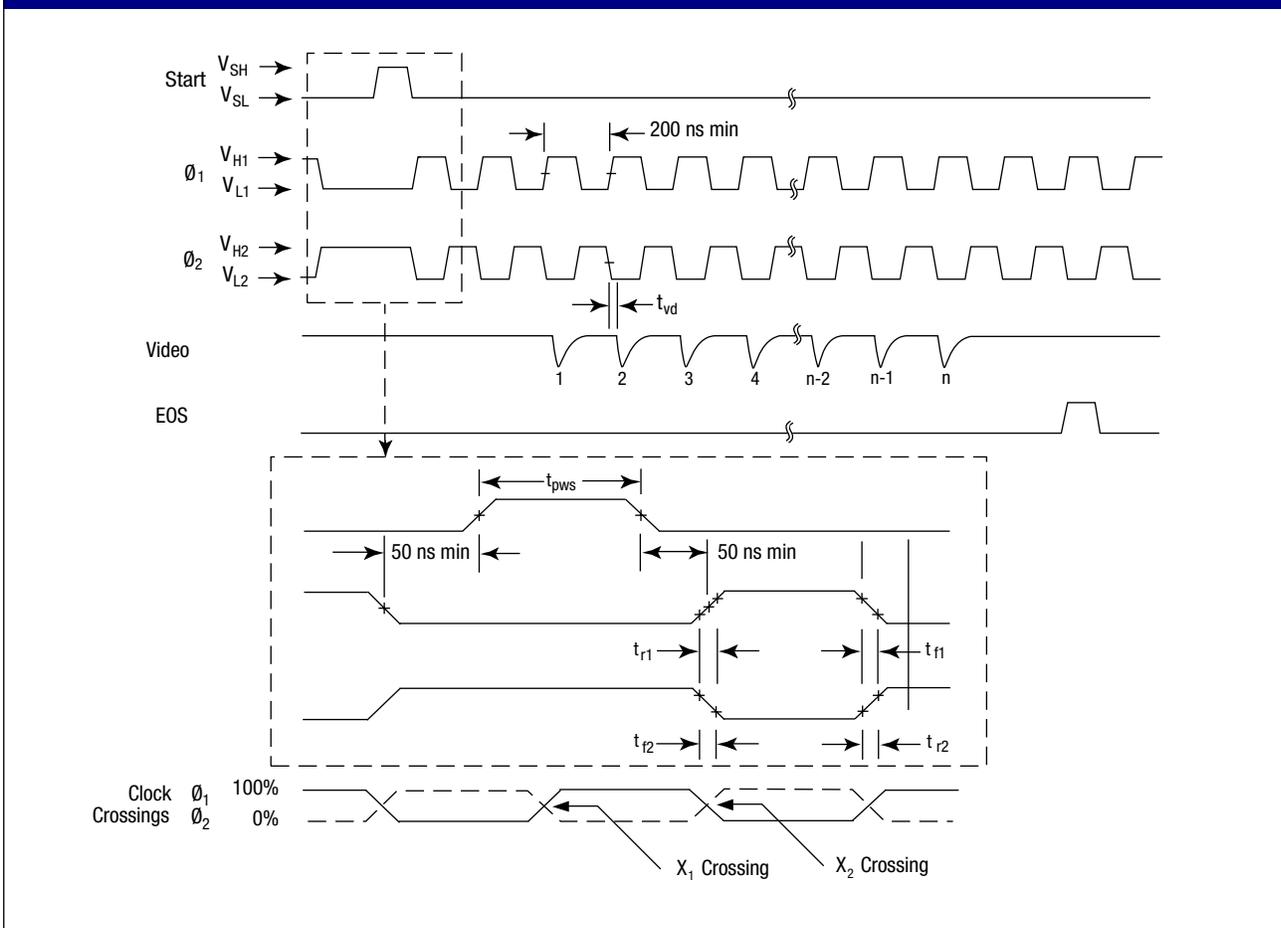
**Figure 4. Typical Signal Charge vs. Exposure at 600 nm**



**Figure 5. Temperature Diode Read Mode**



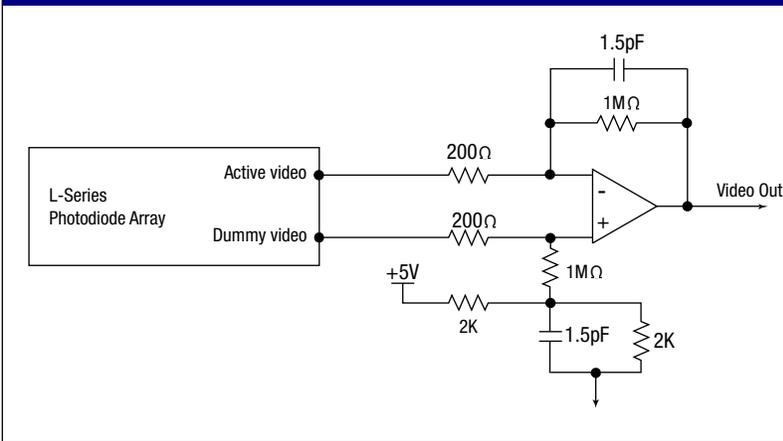
**Figure 6. Timing Diagram**





# CMOS Spectroscopy Sensors

**Figure 8. L-series Readout Amplifier**



Notes:

1. Video Out Amplitude = Signal Charge / Feedback Capacitance

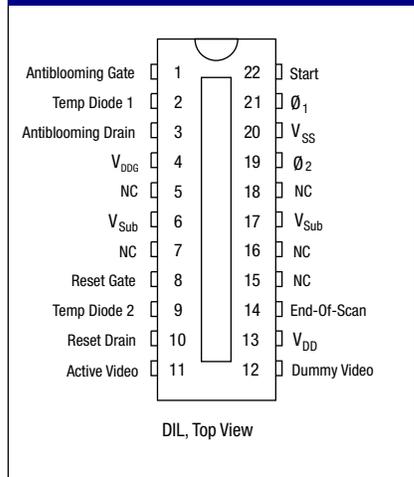
$$\text{Video Amp} = \frac{Q}{C_f} = \frac{10\text{pC}}{1.5\text{pF}} = \frac{t}{1.5\text{pF}} \rightarrow 6.7\text{V}$$

$t = CR = (1.5\text{pF})(1\text{Mohm}) = 1.5 \mu\text{s}$   
 $\leftarrow 2.5\text{V offset}$

\*t = time constant

2. Circuit shown is for a RL12xx device.

**Figure 9. Pinout Configurations**

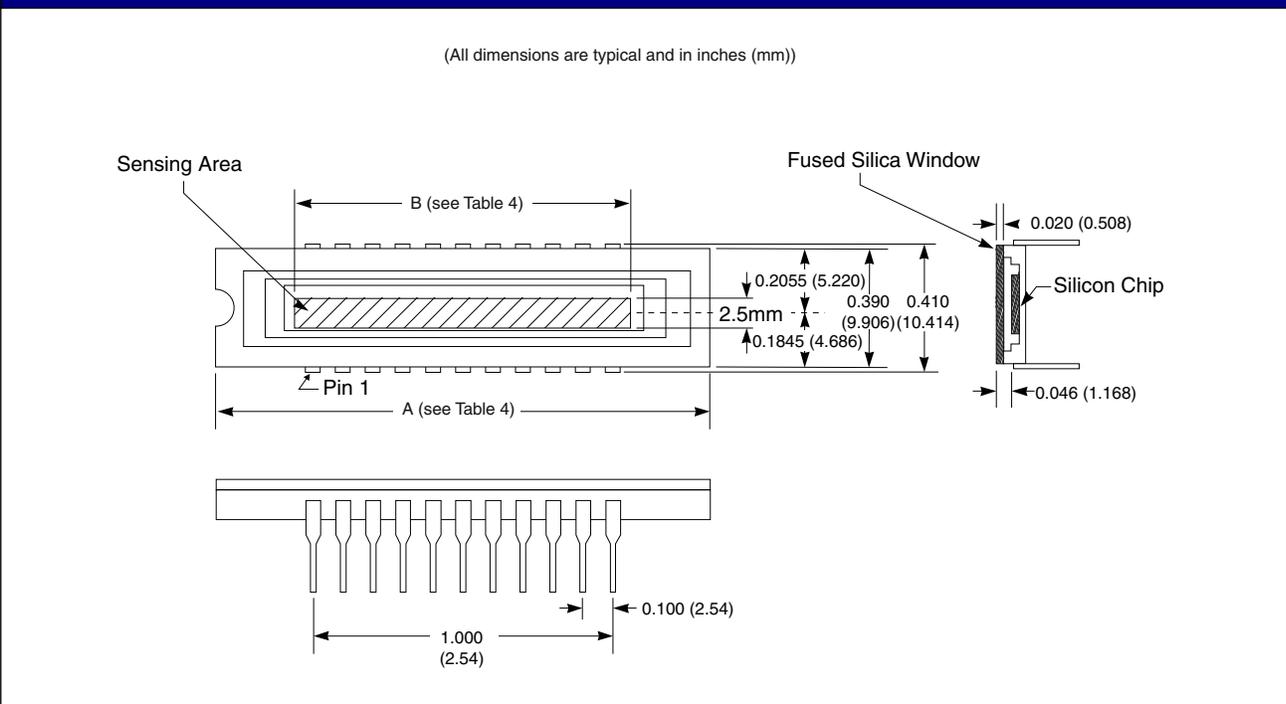


**Table 4. Package Dimensions and Tolerances**

Part Number	A	B
RL1201	1.080 (27.43)	0.126 (3.20)
RL1202	1.080 (27.43)	0.252 (6.40)
RL1205	1.080 (27.43)	0.504 (12.80)
RL1210	1.600 (40.64)	1.008 (25.60)
RL1501	1.080 (27.43)	0.252 (6.40)
RL1502	1.080 (27.43)	0.504 (12.80)
RL1505	1.600 (40.64)	1.008 (25.60)

Note:  
All dimensions in inches (mm)

**Figure 10. Package Dimensions**



# CMOS Spectroscopy Sensor

## Ordering Information

While the information provided in this data sheet is intended to describe the form, fit and function for this product, PerkinElmer reserves the right to make changes without notice.

**Table 5. Stock Part Numbers**

Pixels	Pixel Pitch	
	25µm	50µm
128	RL1201LGQ-711	RL1501LFQ-711
256	RL1202LGQ-711	RL1502LFQ-711
512	RL1205LGQ-711	RL1505LFQ-711
1024	RL1210LGQ-711	-

For more information e-mail us at [opto@perkinelmer.com](mailto:opto@perkinelmer.com) or visit our web site at [www.perkinelmer.com/opto](http://www.perkinelmer.com/opto). All values are nominal; specifications subject to change without notice.

**Table 6. Sales Offices**

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