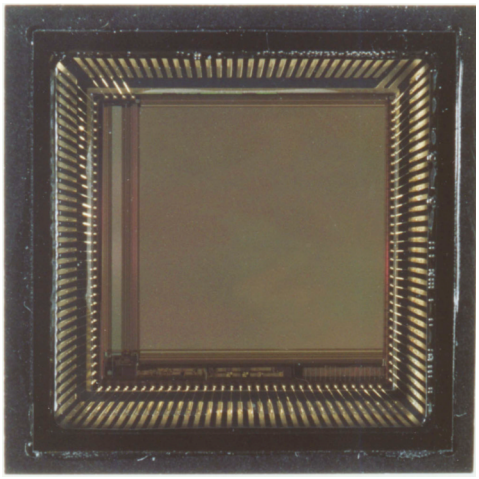
ACS-1024, 1.0 MP High Performance Image Sensor

Key Features:

- **Fast - PVS-Bus™ high speed technology**
  - ***30 Full Frames per second progressive***
  - ***Dual simultaneous high speed sub frames***
    - ***>90 fps at 640 x 480***
    - ***>2000 fps at 100 x 100***
    - ***Real time programmable size and position***
- **High Performance**
  - ***66 dB linear***
  - ***>100dB via averaging***
  - ***Very Low noise with ACS® technology***
  - ***High Sensitivity***
  - ***Very Low Dark Current***
- **Dual output, with programmable gain and offset**
  - ***10 bit digital***
  - ***Analog output***
- **Dual shutter modes**
  - ***Full Frame Snap shot shutter***
  - ***Programmable Rolling Shutter***
- **Multiple Read – out modes**
  - ***Correlated Double Sampling***
  - ***Adaptive Exposure mode – read out while integrating***
  - ***Non-Destructive Read out mode***
    - ***High S/N via signal averaging***
- **Row and Column 'Binning'**
- **Random Pixel Access**
  - ***User addressable***
- **Lower System Cost than CCD based systems**
  - **Reduced BOM vs. CCD systems**
    - ***On-chip Correlated Double Sampling***
    - ***On-chip timing and control***
    - ***Single 5.0 volt supply with 3.3/5 V I/O***
    - ***Integrates directly to standard logic/DSP's/micros***
- **Low power consumption**
- **Choice of Packaging**
  - ***LCC***
  - ***CPGA***
- **Easy CCD retrofit for existing systems**
- **Digital I/O is CMOS/TTL compatible**
- **Cascadable – tri-state busses allow multiple sensors to share common busses**



The Photon Vision Systems ACS 1024 is a high performance area image sensor designed for a wide variety of applications in the scientific, industrial, commercial, and medical markets, including:

Machine Vision
Inspection
Gauging
Spectrometry
Biotech imaging and measurements
Medical imaging
Laser beam profiling
Astronomy
Object tracking
Identification systems
Bar code reading

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Description

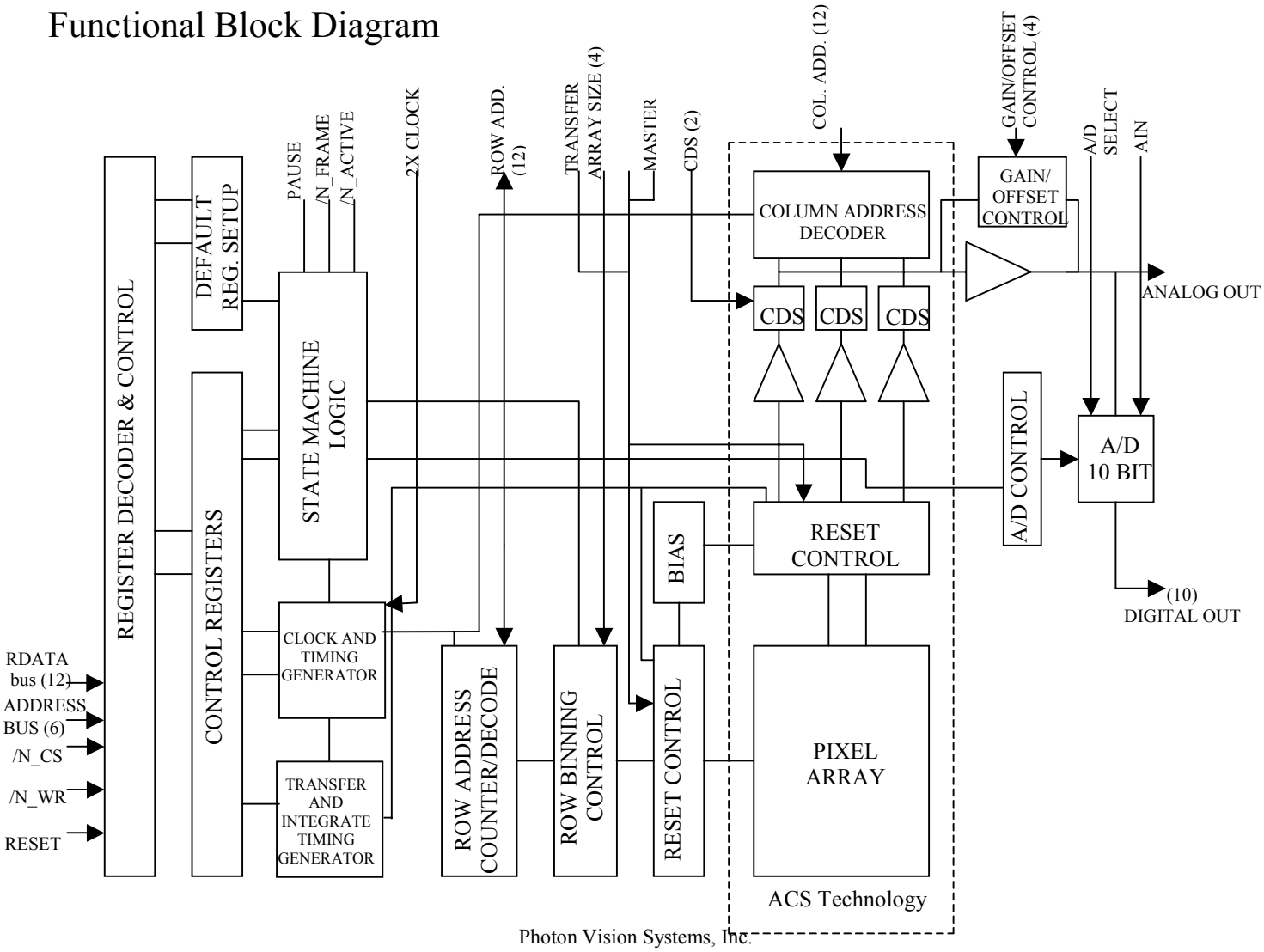
The ACS Image Sensor consists of an array of low dark current photo-diode pixels coupled to patented Active Column Sensor (ACS®)* technology, which provides superior functionality and performance compared to alternative CMOS and CCD image sensors on the market today. Each pixel contains a storage site, allowing electronic shutter or adaptive exposure control. These Imaging systems may be controlled externally, or operate completely autonomously using the on-chip configuration registers and programmable multi-mode controller.

This device is available in 2 package types, Ceramic Pin Grid Array (CPGA) and Leadless Chip Carrier (LCC).

All that is needed to complete a camera is a single power supply and an external oscillator. This minimum configuration will allow the device to run at default settings. A remote control can be used to modify the device settings to control the myriad of on chip capabilities.

*Patent number 6,084,229 and other patents pending apply.

Functional Block Diagram



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Pixel Type	Active Column Sensor ™ photo diode
Array Size	1026 x 1026 (ACS-I 1024)
Pixel Size (Pitch)	
Imaging Active Area	13.21mm X 13.21mm
Output	1K ohm output impedance Analog and 10bit digital
Fill Factor approx.	>60%

Electrical Characteristics/Recommended Operating Conditions

T_A = 25°C, VDD = 5.0V, CLK = 5.0 MHz, Light Source = 5300°K + Infrared blocking filter, Load Impedance = 5pF, and CMOS logic levels unless otherwise noted.

Parameter	Test Conditions	Min	Typical	Max	Units
Supply Voltage		4.75	5.0	5.25	V
Power Consumption			150	300	mW
Input High Level		2.5			V
Input Low Level				0.7	V
Pixel Read Rate - Analog		0.5	30	40	MHz
Pixel Read Rate - Digital		1.2	20		MHz
Analog output External Load			1000		Ohms
Digital Output External Load			1		CMOS Gate
Output Voltage at Saturation	Analog Out.	0.8	0.9	1.1	V
Output Voltage at Dark	Analog Out.	2.6	2.8	3.2	V
Linearity per pixel	5%-70% avg.	0.05	2.5	5.0	%SAT
Dark Signal	1 sec. Integration time		<0.2	<2.0	%SAT
Dynamic Range (RMS)	Vsat/RMS Noise Analog Out.		66		dB
Conversion factor - user selectable	See Note 1	2.5		10	µv/e
Pixel – Pixel FPN	Across array		0.5		rms %
Full Well	See Note 1		300k		electrons
Quantum Efficiency	@500nm		50.0 Nom.		% Norm.
Read Noise			150	250	rms electrons
Spectral response	See curve	350		1100	nm
Image Lag		0.1	1.0	3.0	%SAT
Relative Humidity		0		85	%
Operating Temperature		0		70	°C

Notes: 1. Conversion factor is user selectable via setup registers.

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Absolute maximum ratings, T_A = 25°C unless otherwise noted, see Note †

Supply voltage range, V_{DD} ---------- 0 V to 5.25 V
Digital input current range, I ---------- –16 mA to 16 mA
Operating case temperature range, T_C (see Note 2)---------- –5°C to 70°
Operating free-air temperature range, T_A ---------- 0°C to 60°C
Storage temperature range ---------- –20°C to 85°C
Humidity range, Rh ---------- 0-85%, non-condensing
Lead temperature 1.5 mm (0.06 inch) from case for 10 seconds---------- 235°C

† Exceeding the ranges specified under "absolute maximum ratings" can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated above, is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.

NOTES: 1. Voltage values are with respect to the device GND terminal.

2. Case temperature is defined as the surface temperature of the package measured directly over the integrated circuit.

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Active Column Sensor Series Pixel Operations

This is a review of the ACS pixel operations. Figure #1, is representative of the pixel schematic of the ACS sensor. Normal pixel operation consists of a sequence of steps that involves resetting the pixel and the hold site, an integration period to accumulate the video signal, a sampling of the video signal and a separate sampling of the background information, and then starting the process again for the next frame of video.

The order of steps may change and some steps may be repeated within a cycle, but the fundamental steps are included. There are four allowed operations for sensing the video signal. In the first method, named "Rolling Shutter" with normal CDS, the background is sampled on the Hold capacitor and then the pixel video value is transferred and re-sampled. The background signal is automatically subtracted from the pixel video value to provide clean video with a minimum level of noise. In the second method, "Rolling Shutter" with reverse CDS, the video signal is read out first, and then the pixel is reset and the background read out. The third method named, "Snapshot Shutter" is useful for freeze frame operations. In this method, the video signal is sampled on the Hold capacitor and the pixel is reset and re-sampled for background information. Once again the background is subtracted from the video value to provide clean video. The fourth method, named "Adaptive Exposure Control", allows the pixel to be read without being rest. This allows the video to be sampled and re-sampled until the desired signal has accumulated. Then the pixel is reset and re-read for video background information.

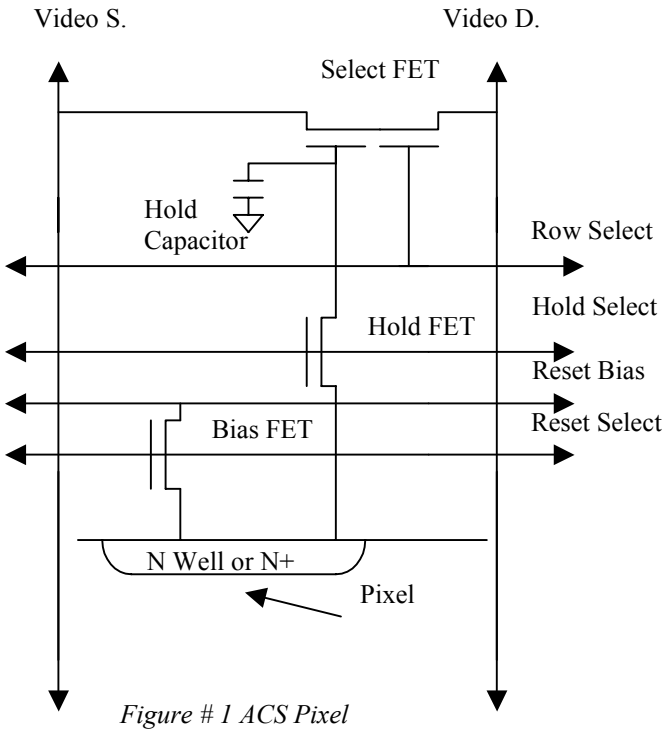

Figure # 1 ACS Pixel

Before we begin the detailed discussion of the pixel operations, the pixel structure and its components will be described. All pixel operations are accomplished on a row-by-row or global basis. A row operation is defined as all pixels in a row as having the same signal or operation performed at the same time. A global operation is defined as the signal or operation is applied to all pixels on the array at the same time. All descriptions herein involve row operations unless otherwise noted. Referring to Figure # 1, at the top of the drawing is the dual gate Select FET of the Active Column Sensor (ACS). This dual gate FET has the dual purpose of selecting a row of pixels as well as sensing the accumulated charge within the pixel. The Row Select line turns each row of Select FETs "on". The select FET is part of a Unity Gain Amplifier, with the remainder of the UGA located at each column and is the reason that the source and drain of the Select FET run the length of the column of pixels. The UGA configuration per pixel eliminates the pixel-to-pixel variations known as Fixed Pattern Noise that plague other image sensors. The next FET below the Select FET is the Hold FET that is controlled by the Hold Select line. When the Hold FET is selected or turned "on" and turned back "off", or deselected, the value in the pixel photodiode is sampled and stored on the capacitor. The value stored could either be the reset value the pixel is reset to or the accumulated pixel value after the pixel has integrated light for a given time period. When the row is selected and the Hold FET is deselected the value stored in the capacitor is the value sensed by the UGA. The next FET is the Bias FET, when selected biases the Pixel to the reset value via the Rest Bias line.

The "Rolling Shutter" CDS method described above reduces KTC noise. This read-out method starts with the Hold FET and the Bias FET selected. This allows for the pixel and the capacitor to be reset to the initial reset bias. The Bias FET and the Hold FET are subsequently released or deselected. The pixel is allowed to integrate for one frame time and the row is selected for reading. The value in the Hold capacitor that was set to the initial reset values is read first. The Hold FET is selected, allowing the Pixel value to be read next. The reset and pixel values are subtracted from each other for virtually pattern noise free video. The process is repeated from frame to frame in normal rolling shutter video and the same can be accomplished in a global frame sequence. Reading or sensing are used interchangeably for the ACS sensors as the accumulated pixel signal is only sensed when read. The signal isn't destroyed as in Charge Coupled Devices (CCD's) and in effect is only sensed and left

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undisturbed for further reading allowing noise elimination or continued signal accumulation for optimal image contrast. The "sensing" of the pixel signal is a key advantage over CCD's.

Snapshot shutter allows video to be temporarily stored on the Hold capacitor. The sequence starts with the Hold FET and the Reset FET turned "on" to bias both the Hold capacitor and the pixel to the same level. The Reset FET and the Hold FET are turned "off". The pixel is allowed to integrate. The Hold FET is selected, the video on the pixel is sampled, and the Hold FET is turned "off" or deselected. When the row is selected for reading, the Row FET is selected and the stored video is read. Then, the Rest FET and Hold FET are selected, re-biasing the pixel to the reset value and both are turned off. The rest value is sampled and subtracted for pattern noise free video.

The "Adaptive Exposure Control" method describes Non Destructive Read Out (NDRO) for ACS sensors. The pixels are biased to the reset value by selecting and deselecting the Hold FET and Reset FET as previously described. The pixels are allowed to integrate. The Hold FET is selected and deselected for sampling the pixel value. The value is read for optimal signal levels. If more integration is desired, the pixels are allowed to integrate longer and pixel value is re-sampled by selecting and deselecting the Hold FET. When the desired signal level has been achieved, a row is selected for reading by selecting the Select FET and sampling the video by selecting and deselecting the Hold FET. The Hold and Bias FETs are then Selected and deselected to re-bias the pixels the reset value and the background.

These are the standard methods allowed and controlled internally by the ACS sensors series. If the imager is operated in the slave mode, greater operator control allows more flexibility, to minimize the number of operations performed per frame of Video and potentially reduce the associated noise generated.

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OPERATIONAL DESCRIPTION:

For simplicity, all of the operational descriptions will specify only signal names not their origin, with the understanding that each signal referenced may originate from the Controller or the user depending upon the Master Slave mode.

CONTROLLER
In the Master mode the ACS utilizes a complex state machine (heretofore the Controller) to control all events and operation. By use of the N_CS, N_WR, ADDX and the REG_DATA_X inputs the user may load configuration and operational information into on chip registers that are accessed by the Controller. The ACS uses a set of shadow registers to store incoming data allowing the user to write data at any time. The data from these registers is transferred to the Controller at the beginning of each frame cycle, therefore any data written to the ACS will take effect and be synchronized with the next frame. Also by use of the aforementioned inputs, the user may read register data out of the Controller.

PIXELS
The ACS pixels are comprised of a Photo Diode (PD) which, when in integration, produces a current proportional to the amount of incident light. The PD is connected through a field effect transistor (FET) switch to a capacitor or Storage Site (SS). Another FET switch connects the PD and SS to a reset bias that is supplied to the pixel. The operation of these two switches controls the integration and reset of the pixel. Reset and integration may be performed on a row-by-row basis or globally. Signals CRST, TX, ROW RST and ROW XFER enable global reset, global transfer; row reset and row transfer respectively.

CDS TIMER
The ACS performs Fixed Pattern Noise (FPN) cancellation by use of on chip Correlated Double Sampling (CDS). The CDS sequence begins by the selection of a given row. Once the data on the Row Address Bus is valid, ROW_LOAD must be strobed to latch the address data. Next, a Row Load Pulse (RLP) must be sent to the CDS timer to begin the CDS process. Upon the completion of CDS, the CDS Timer issues an End Of CDS (EOC) indicating that there is valid data on the video output bus. As the ACS is randomly addressable, the CDS timer has no knowledge of the size of the array area to be readout. The ACTIVE signal must be set TRUE and stay TRUE until readout of the desired pixels is completed. After readout completion releasing the ACTIVE signal, allows the CDS timer to finish end of row events.

PVS BUS OUTPUT/READOUT
After completion of CDS and the issuance of ACTIVE, valid data is available on the video bus. To accomplish readout, an address is placed on the Column Address Bus, COL_LOAD must be strobed, at which time the data from the first pixel in the desired array is available. The address and COL_LOAD sequence are repeated until the last pixel in the row has been read.

CDS/READOUT MODES:

The ACS has 4 modes of integration-readout operation, Mode 0 or standard rolling shutter mode (conventional CDS), Mode 1 or reverse CDS rolling shutter, Mode 2 or adaptive exposure mode (non-destructive readout) mode, and Mode 3 or full frame shutter (snapshot shutter) mode.

MODE 0
This mode is referred to as Standard or Conventional CDS (CCDS). In this mode (recall the pixel structure) after integration the SS is sampled, then the PD value is transferred and the SS re-sampled. The first sample is subtracted from the second in a differential amplifier and the net result is video minus noise.

MODE 1
Mode 1 is referred to as reverse or Quasi-CDS (QCDS). Under high overload conditions, this mode provides superior isolation from saturation artifacts. When performing full frame transfer functions, QCDS is required. In QCDS the global transfer switch is always closed, thus the PD and SS are the same node electrically. During readout, the combined node is sampled, then reset takes place and the node is re-sampled. The differential amplifier yields the first minus the second.

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MODE 2
Mode 2 is transfer and accumulate, or Adaptive Exposure Control (AEC). The objective of this mode is to allow the user to sample the video amplitude in the pixels while integration is occurring. This is useful under lighting conditions that vary from sample to sample. When the user has determined that a sufficient signal level exists, the user will typically change to mode 3 and acquire a frame of useful data.

The differential amplifier requires a "background sample" to operate correctly. However in mode 2 the PD and SS must be electrically connected to sample the video amplitude. When the ACS is switched to mode 2, it stores the background sample from the previous frame for this purpose. While in mode 2 no CDS is actually taking place, to subtract the background during final readout. When a sufficient sample is obtained, it is recommended that the user switch to mode 1 for readout.

MODE 3
Mode 3 is Full Frame Shutter and Destructive Readout. This mode typically would be used in conjunction with the HOLDOFF and TRANSFER registers. At the start of a frame the Controller tests the HOLDOFF register for a non-zero value. If present the Controller waits an amount of time determined by this value, during which the pixels are held in reset. At the end of the holdoff time the pixels are placed into integration. Next the Controller tests the TRANSFER register and waits for that period of time, ending by transferring the PD vale to the SS. The Controller then begins readout. Note that if the HOLDOFF register is zero, no pixel reset will take place. If the TRANSFER register is zero, there will be no integration time.

Signal Description

Signal No.	LCC Pin	CPGA Pin	Name	Signal Type	Description
1	117	D3	REG_DATA_5	Bi-directional I/O See pins 56,57	Setup Register data bit 5. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
2	118	C2	REG_DATA_6	Bi-directional I/O See pins 56,57	Setup Register data bit 6. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
3	119	B1	REG_DATA_7	Bi-directional I/O See pins 56,57	Setup Register data bit 7. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
4	120	D2	REG_DATA_8	Bi-directional I/O See pins 56,57	Setup Register data bit 8. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
5	121	E3	REG_DATA_9	Bi-directional I/O See pins 56,57	Setup Register data bit 9. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
6	122	C1	REG_DATA_10	Bi-directional I/O See pins 56,57	Setup Register data bit 10. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
7	123	E2	REG_DATA_11	Bi-directional I/O See pins 56,57	Setup Register data bit 11, MSB. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
8	124	D1	DIG_PAD_PWR	Digital Pad Power 5.0 VDC	Power in for Digital Pads
9	125	F3	DIG_PAD_GND	Digital Pad Power Ground	Power ground for Digital Pads
10	126	F2	C_DATA_0 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address LSB BIT 0 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
11	127	E1	C_DATA_1 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 1 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
12	128	G2	C_DATA_2 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 2 - If in SLAVE mode, input column Pin must be connected whenever in SLAVE mode, do not float. Address for random access. If in MASTER mode, output for currently addressed pixel.
13	129	G3	C_DATA_3 M/S	Bi-directional I/O Digital In - SLAVE	Column address BIT 3 - If in SLAVE mode, input column Pin must be connected whenever in SLAVE mode, do not float. Address for random access. If in MASTER mode, output for

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				Digital Out - MAST	Address for random access. If in MASTER mode, output for currently addressed pixel.
14	130	F1	C_DATA_4 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 4 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
15	131	G1	C_DATA_5 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 5 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
16	132	H2	C_DATA_6 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 6 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
17	1	H1	C_DATA_7 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 7 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
18	2	H3	C_DATA_8 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 8 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
19	3	J3	C_DATA_9 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 9 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
20	4	J1	C_DATA_10 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address BIT 10 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
21	5	K1	C_DATA_11 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Column address MSB BIT 11 - If in SLAVE mode, input column address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
22	6	J2	R_DATA_0 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address LSB BIT 0 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
23	7	K2	R_DATA_1 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 1 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
24	8	K3	R_DATA_2 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 2 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
25	9	L1	R_DATA_3 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 3 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
26	10	L2	R_DATA_4 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 4 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
27	11	M1	R_DATA_5 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 5 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
28	12	N1	R_DATA_6 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 6 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
29	13	M2	R_DATA_7 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 7 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
30	14	L3	R_DATA_8 M/S	Bi-directional I/O Digital In - SLAVE	Row address BIT 8 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE

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				Digital Out - MAST	addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
31	15	N2	R_DATA_9 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 9 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
32	16	P1	R_DATA_10 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address BIT 10 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
33	17	M3	R_DATA_11 M/S	Bi-directional I/O Digital In - SLAVE Digital Out - MAST	Row address MSB BIT 11 - If in SLAVE mode, input Row address for random access. If in MASTER mode, output for currently addressed pixel. Pin must be connected whenever in SLAVE mode, do not float.
34	44	P13	ROW RESET	Digital Input	In slave mode when TRUE LOW resets the selected row. Pin must be connected whenever in SLAVE mode, do not float.
35	45	R14	ROW TRANSFER	Digital Input	In slave mode when TRUE LOW this signal transfers charge from the collection site to the storage site for the selected row Pin must be connected whenever in SLAVE mode, do not float.
36	46	N12	EOC	Digital Output	In slave mode when TRUE LOW CDS is completed for the selected row Pin must be connected whenever in SLAVE mode, do not float.
37	47	N13	ACTIVE	Digital Input	In slave mode this signal must go TRUE LOW within 1 1X clock cycle after EOC goes true in order to begin readout of the selected row Pin must be connected whenever in SLAVE mode, do not float.
38	48	P14	RLP IN	Digital Input	In slave mode this signal must go TRUE LOW for 1 1X clock to initiate CDS on the selected row Pin must be connected whenever in SLAVE mode, do not float.
39	49	R15	EXT ANA SEL	Digital Input 0 Internal Video 1 External Input	This signal selects between the internal video and the external analog input Pin must be connected whenever in SLAVE mode, do not float.
40	51	M13	CDS1	Digital Input CDS1 CDS0 Mode 0 0 Full CDS 0 1 Quasi CDS 1 0 No CDS 1 1 Transfer and Readout	Standard readout mode Readout mode used for snapshot Accumulate and Transfer – This is output without CDS, the user is advised to change to CDS mode 1 to readout when sufficient signal level is achieved. Transfer and Readout. Pin must be connected whenever in SLAVE mode, do not float.
41	52	N14	CDS0	Digital Input See table, pin 40	Use in conjunction with pin 40. Pin must be connected whenever in SLAVE mode, do not float.
42	53	P15	C1	Digital Input C1 C0 0 - 1X 1 - 2X X - 4X	Col Binning 1X - Device outputs full horizontal pixel resolution 2X - Every 2 rows are binned, horizontal resolution is divided by 2 Pin must be connected whenever in SLAVE mode, do not float. 4X - Every 4 rows are binned, horizontal resolution is divided by 4 Pin must be connected whenever in SLAVE mode, do not float.
43	54	M14	C0	Digital Input	See Above Pin must be connected whenever in SLAVE mode, do not float.
44	55	L13	R1	Digital Input R1 R0 0 0 – 1X 0 1 – 2X 1 0 – 4X	Row Binning control 1X - Device outputs full vertical pixel resolution 2X - Every 2 rows are binned, vertical resolution is divided by 2 4X - Every 4 rows are binned, vertical resolution is divided by 4 Pin must be connected whenever in SLAVE mode, do not float.
45	56	N15	R0	Digital Input	See Above Pin must be connected whenever in SLAVE mode, do not float.
46	57	L14	CRST	Digital Input	In slave mode when TRUE LOW CRST performs a global reset on all pixel Note: TX must also be TRUE. Pin must be connected whenever in SLAVE mode, do not float.
47	58	M15	RESET	Digital Input	TREU LOW Forces master reset of state machine to default values.

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					Pin must be connected whenever in SLAVE mode, do not float.
48	59	K13	PAUSE	Digital Input 0 - Transfer and read 1 - Transfer and pause	In master mode if PAUSE Control bit Control Register 1 bit 7 is set TRUE the controller will wait for Pin 48 to go TRUE LOW before readout will begin. Pin must be connected whenever in SLAVE mode, do not float.
49	60	K14	MASTER	Digital Input 1 - SLAVE Mode 0 - MASTER Mode	MASTER/SLAVE Mode select. When OFF, device is in MASTER mode. When ON, device is in SLAVE Mode. When in MASTER mode, those signals indicated with the 'M/S' symbol indicate that the function of these signals is depends on the selected Mode. Typically when the device is in MASTER mode, the 'M/S' signals like the row and column address buses output the currently accessed pixel. When in SLAVE mode, the 'M/S' signals are used to externally access these buses for random access.
50	61	L15	GAIN1	Digital Input Value (Hex) of G0, G1, F0, F1. See Control Register 0.	GAIN and OFFSET control. Works in conjunction with pins 51 - 53. Default is 1X gain and no offset. Pin must be connected whenever in SLAVE mode, do not float.

	GAIN SETTING (Volts)	OFFSET SETTING
0	S1 - 1.00	0.00
1	S2 - 1.33	0.30
2	S3 - 2.00	0.60
3	S4 - 4.00	0.90
4	S5 - 1.00	0.00
5	S6 - 1.33	-0.60
6	S7 - 1.33	-0.90
7	S8 - 1.00	0.00
8	S9 - 2.00	-0.60
9	S10 - 1.33	-0.30
A	S11 - 2.00	-0.90
B	S12 - 4.00	-0.90
C	S13 – 1.00	0.00
D	S14 - 1.00	-0.60
E	S15 - 2.00	-0.90
F	S16 - 4.00	-0.90

51	62	J14	GAIN0	Digital Input See table, pin 50.	GAIN and OFFSET control. Works in conjunction with pins 50, 51, and 52 Pin must be connected whenever in SLAVE mode, do not float.
52	63	J13	OFFSET1	Digital Input See table, pin 50.	GAIN and OFFSET control. Works in conjunction with pins 50, 51, and 52 Pin must be connected whenever in SLAVE mode, do not float.
53	64	K15	OFFSET0	Digital Input See table, pin 50.	GAIN and OFFSET control. Works in conjunction with pins 50,51 and 52 Pin must be connected whenever in SLAVE mode, do not float.
54	65	J15	DIG_PAD_GND	Digital Pad Power Ground	Ground for Digital Pads
55	66	H14	DIG_PAD_PWR	Digital Pad Power 5.0 VDC	Power for Digital Pads
56	67	H15	$\overline{\text{N\_CS}}$	Digital Input	Controls direction of REG_DATA lines, pins 112 - 116 and pins 1-7, by reading or writing to setup registers. Works in conjunction with pin 57. See SETUP REGISTER TIMING diagrams for details. Pin must be connected whenever in SLAVE mode, do not float.
57	68	H13	$\overline{\text{N\_WR}}$	Digital Input	Controls direction of REG_DATA lines, pins 112 - 116 and pins 1-7, by reading or writing to setup registers. Works in conjunction with pin 54. See SETUP REGISTER TIMING diagrams for details. Pin must be connected whenever in SLAVE mode, do not float.
58	69	G13	SYNC	Digital Input	In master mode if Register 0 bit 4 is set controller will wait for pin 58 to go TRUE LOW before leaving state 0 and beginning a new cycle. Pin must be connected whenever in SLAVE mode, do not float.
59	70	G15	TX	Digital Input	In slave mode, when TRUE LOW TX performs a global transfer of the charge from the collection site to the storage site Pin must be connected whenever in SLAVE mode, do not float.

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60	71	F15	COL_LOAD	Digital Input SLAVE only	Load Column Address that is loaded onto C_DATA bus (pins 10-21) into imager. Only Works in SLAVE mode. Pin must be connected whenever in SLAVE mode, do not float.
61	72	G14	ROW_LOAD	Digital Input SLAVE only	Load Row Address that is loaded onto the R_DATA bus (pins 22-33) into imager. Only works in SLAVE mode. Pin must be connected whenever in SLAVE mode, do not float.
62	73	F14	GB_ANA_GND	Guard Band analog	Ground for Analog guard band
63	74	F13	ANA_GND2	Analog Circuits 2 Ground	Ground input for the A/D
64	75	E15	ANA_GND1	Analog Circuits 1 Ground	Ground input for the A/D.
65	76	E14	ANA_PAD_GND	Analog Pad Ground	Ground input for analog pads.
66	77	D15	GB_ANA_PWR	Guard Band analog POWER 5.0 VDC	Power in for Analog Guard Band.
67	78	C15	ANA_PAD_PWR	Analog Pad POWER 5.0 VDC	Power in for analog pads.
68	79	D14	PIX_AMP_ANA_PWR	Analog Power 5.0 Volts	Power to Column amplifier
69	80	E13	ANA_PWR1	Analog Circuits 1 POWER 5.0 VDC	Power in for the A/D.
70	81	C14	ANA_PWR2	Analog Circuits 2 POWER 5.0 VDC	Power in for the A/D.
71	82	B15	ANALOG_OUT	Analog Video Out	Video output – analog, requires 1.0k ohm pull-up to VDD
72	83	D13	BIAS_PAD_EXT	Analog pixel Bias	Tie a 10-30pF capacitor from this pin to analog ground.
73	84	C12	ANALOG_IN	Analog input, Range 0.9-3.2 VDC	Referenced to pin 63. Use this pin to input an external analog signal for referencing the A/D and/or calibration. Note that the last pixel of each frame read is the converted value of this reference, not the value of the pixel, when Control Reg. 1 bit 6 is set high.
74	85	B13	DIG_PAD_PWR	Digital Pad Power 5.0 VDC	Power in for Digital Pads
75	86	A14	DIG_PWR	Digital Circuits Power 5.0 VDC	Power in for Digital circuits
76	87	B12	DIG_GB_PWR	Digital Guard Band Power 5.0 VDC	Power in for Digital Guard Band.
77	88	C11	DIG_PAD_GND	Digital Pad Ground	Power in for Digital Pads
78	89	A13	DIG_GND	Digital Ground	Ground input for Digital circuits.
79	90	B11	ADD0	Digital Input Setup Register Address Bit 0 - LSB.	Setup register address bit 0 - LSB. Address bus for access to the SETUP REGISTERS.
80	91	A12	ADD1	Digital Input Setup Register Address Bit 1.	Setup register address bit 1. Address bus for access to the SETUP REGISTERS.
81	92	C10	ADD2	Digital Input Setup Register Address Bit 2.	Setup register address bit 2. Address bus for access to the SETUP REGISTERS.
82	93	B10	ADD3	Digital Input Setup Register Address Bit 3.	Setup register address bit 3. Address bus for access to the SETUP REGISTERS.
83	94	A11	ADD4	Digital Input Setup Register Address Bit 4 - MSB.	Setup register address bit 4. Address bus for access to the SETUP REGISTERS.
84	95	B9	CLK_IN_2X	Digital Input Master Clock	Input for Master Clock, must be 2X desired pixel read rate.
85	96	C9	CLK1X	Digital Output	Output Pixel Clock Rate. Note that this pin is referenced to pin 90.
86	97	A10	$\overline{\text{LINE\_ACTIVE}}$	Digital Output Row video Valid	Output goes TRUE LOW when an active line of video is output.
87	98	A9	$\overline{\text{FRAME}}$	Digital Output Frame Valid	Output goes TRUE LOW when an active frame of video is output.
88	99	B8	DIG_PAD_PWR	Digital Video output pad power	This value may be between 5.0v and 3.3v, the result is that all the digital video output pads will have the selected vdd at the true high level
89	100	A8	DIG_PAD_GND	Digital Video output pad ground	Ground digital video output pads.

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90	101	C8	DIG_DATA_ENA	Digital Input Digital video Data enable.	When true low digital video, 1X clock, ACTIVE and FRAME are output. When false theses outputs are tri-stated
91	102	C7	DATA_0_LSB	Tri-state Output Digitized video Bit 0 LSB	Digital video is output as Bit 0, LSB.
92	103	A7	DATA_1	Tri-state Output Digitized video Bit 1	Digital video is output as Bit 1.
93	104	A6	DATA_2	Tri-state Output Digitized video Bit 2	Digital video is output as Bit 2.
94	105	B7	DATA_3	Tri-state Output Digitized video Bit 3	Digital video is output as Bit 3.
95	106	B6	DATA_4	Tri-state Output Digitized video Bit 4	Digital video is output as Bit 4.
96	107	C6	DATA_5	Tri-state Output Digitized video Bit 5	Digital video is output as Bit 5.
97	108	A5	DATA_6	Tri-state Output Digitized video Bit 6	Digital video is output as Bit 6
98	109	B5	DATA_7	Tri-state Output Digitized video Bit 7	Digital video is output as Bit 7.
99	110	A4	DATA_8	Tri-state Output Digitized video Bit 8	Digital video is output as Bit 8.
100	111	A3	DATA_9	Tri-state Output Digitized Video Bit 9	Digital video is output as Bit 9.
101	112	B4	REG_DATA_0	Bi-directional I/O	Setup Register data bit 0, LSB. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
102	113	C5	REG_DATA_1	Bi-directional I/O	Setup Register data bit 1. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
103	114	B3	REG_DATA_2	Bi-directional I/O	Setup Register data bit 2. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
105	115	A2	REG_DATA_3	Bi-directional I/O	Setup Register data bit 3. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.
105	116	C4	REG_DATA_4	Bi-directional I/O	Setup Register data bit 4, MSB. See Register setup table for more information Pin must be connected whenever in SLAVE mode, do not float.

When the device is in MASTER mode, the on-chip state machine uses the information in the setup registers to control the imager. These registers are 12 bits wide. The register data can be accessed via the bi-directional REG_DATA 12 bit wide parallel bus, pins 1-7 and 112-116. These are accessed via a 5 bit address bus ADD, pins 80, 82, 84, 86, and 88. See figures 3 and 4 for access timing.

REGION OF INTEREST REGISTERS:

The device has the ability to control 2 regions of interest simultaneously. This allows for faster sub frame readout. The ROI Registers must contain a valid non-zero value for that ROI to operate. Note that at least one of the ROI's must be setup in order to scan video. The ROI's can overlap, but note that the pixels read in the first ROI are valid in the overlap region. When the second ROI is read, the same pixels when read for the other region will not be valid.

SETUP REGISTERS:

REGISTER ADDRESS (Hex)	NAME	DESCRIPTION	DEFAULT VALUE
0	ROI 0 Row Start	Row Address of pixel for ROI 0 to Start – must be less than REG. 1.	0
1	ROI 0 Row Stop	Row Address of pixel for ROI 0 to Stop – Must be greater than REG. 0.	1024
2	ROI 0 Col. Start	Column Address of pixel for ROI 0 to Start – must be less than REG. 3.	0
3	ROI 0 Col. Stop	Column Address of pixel for ROI 0 to Stop – Must be greater than REG. 2.	1024
4	ROI 1 Row Start	Row Address of pixel for ROI 1 to Start – must be less than REG. 5.	0

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5	ROI 1 Row Stop	Row Address of pixel for ROI 1 to Stop – Must be greater than REG. 4.	0
6	ROI 1 Col. Start	Column Address of pixel for ROI 1 to Start – must be less than REG. 7.	0
7	ROI 1 Col. Stop	Column Address of pixel for ROI 1 to Stop – Must be greater than REG. 6.	0
8	Reserved	Do not write to this register	0
9	Reserved	Do not write to this register	0
A	Reserved	Do not write to this register	0
B	Reserved	Do not write to this register	0
C	Reserved	Do not write to this register	0
D	Reserved	Do not write to this register	0
E	Reserved	Do not write to this register	0
F	Reserved	Do not write to this register	0
10	HOLDOFF	Full Frame Shutter Mode Holdoff Control Register. This register contains the 'hold off' time from the start of the state machine logic until the pixel site is allowed to accumulate charge. The pixels are held in reset for this time period. The register default is 0 for full frame integration.	0
11	TRANSFER	Transfer Control Register. The charge is transferred from the pixel to the storage site when the state machine logic reaches the value of this register. This value must be greater than FFS HOLDOFF	0
12	CONTROL 0	Control Register 0 – See Register 0 bit description, below.	See Below
13	CONTROL 1	Control Register 1 – See Register 1 bit description, below.	See Below
14	ROLLING HOLDOFF	Rolling Shutter mode Holdoff Control Register, controls exposure time in rolling shutter mode. This register determines the number of rows back from the current row being read to reset and put back into integration that row. Units are in rows.	0
15-1F	Reserved	Do not write to these Registers.	0

CONTROL REGISTER 0 and 1 are broken into separate control bits, as described below. Note that some of these bits have a corresponding I/O pin. The I/O pin is used for the described function whenever the device is in SLAVE mode, otherwise, the I/O pin is ignored in MASTER mode. See the bond out table above for more information.

CONTROL REGISTER BIT DESCRIPTIONS

CONTROL REGISTER	BIT #	NAME	DESCRIPTION	DEFAULT
0	0	G0	See gain and offset table at pin 50	0
0	1	G1	See gain and offset table at pin 50	0
0	2	F0	See gain and offset table at pin 50	1
0	3	F1	See gain and offset table at pin 50	1
0	4	SYNC	When SYNC bit is set true high state machine waits for sync pulse on pin 58	0
0	5	TM	This register bit has become un-used in the latest revision, the modes Formerly controlled by this bit are now under the control of the CDS Bits Do not write to this bit	0
0	6	CS2	CS2 works in conjunction with CS1 to select the system clock speed. See table below.	0
0	7	CS1 CS2 CS1 0 – SR1 1 – SR2 0 – SR3 1 1 – SR4	Clock Select bit 1, in conjunction with CS2, selects the clock rate for pixel read out. Frequency is based on 40 MHz Master clock. Frequency will vary with varying Master clock. SR1 is 20Mhz. (Master clock/2) SR2 is 10Mhz. (Master clock/4) SR3 is 5Mhz. (Master clock/8) SR4 is 2.5Mhz. (Master clock/16)	0
0	8	CS0 CS0 - 0 250us CS0 - 1 1ms	CS0 set to 0 selects 250us clock period (4 kHz). Max. integration is 1 second. CS0 set to 1 selects 1ms clock period (1 kHz). Max. integration is 4 seconds.	0
0	9	CDS1	See CDS table at pin 40	0
0	10	CDS0	See CDS table at pin 41	0

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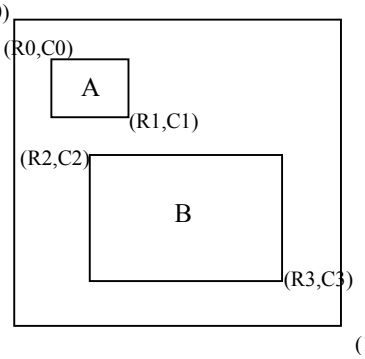
0	11	!STOP	STOP bit, this is a true low bit. When this bit is set to 0, the state machine logic will halt the device at the end of the next read cycle. When set to 1, the state machine allows continuous cycles.	0

CONTROL REGISTER	BIT #	NAME	DESCRIPTION	DEFAULT
1	0	REV0	Device Revision. Bits 4,3,2,and 1 form the revision level for the device.	1
1	1	REV1		0
1	2	REV2		0
1	3	REV3		0
1	4	REV4		0
1	5	RSH	Rolling Shutter Holdoff enable bit. When set to 1, Holdoff is enabled.	0
1	6	AUX-BYPASS	Same as bond pad 39. When set to 1, the analog input that is connected to bond pad 73 is digitized and output as the last pixel of each frame. When set to 0, the last pixel is digitized and output.	1
1	7	PAUSE	Same as I/O pin 48, used only in MASTER mode. See BOND OUT table above for more information.	0
1	8	R1	Same as I/O pin 40, used only in MASTER mode. See BOND OUT table above for more information.	0
1	9	R0	Same as I/O pin 41, used only in MASTER mode. See BOND OUT table above for more information.	0
1	10	C1	Same as I/O pin 42, used only in MASTER mode. See BOND OUT table above for more information.	0
1	11	C0	Same as I/O pin 43, used only in MASTER mode. See BOND OUT table above for more information.	0

REGION OF INTEREST OR SUB-FRAME READOUT:

Figure shows two ROI's can be programmed anywhere on the array. If the a portion of the second region occupies the same rows as the first region, the video output of the shared rows of the second region will be invalid.

Figure 2.



ROI Reg. Set Registers	Values
Row Start 0	R0
Row Stop 0	R1
Col Start 0	C0
Col Stop 0	C1
Row Start 1	R2
Row Stop 1	R3
Col Start 1	C2
Col Stop 1	C3

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TIMING DIAGRAMS: SETUP REGISTER WRITE AND READ

The following timing diagrams illustrate setup register writing and reading. It is important to note that the writing and reading of the setup registers is asynchronous, that is these operations are not clock dependant.
CAUTION: Do not change the state of N_WR whenever N_CS is low. Register reading and writing can only occur when the device is in MASTER mode. Note minimum pulse duration is 1 master clock pulse.

Note that a register write cycle will occur on the rising edge of N_CS while N_WR is low. A register read cycle occurs on the falling edge of N_CS whenever N_WR is high. Data is written to, or read from, the registers, within 50ps of the edge transition. This simplifies timing of signals to access the registers. You only must have valid address and data on the buses during a N_CS transition, therefore the timing diagrams below do not show actual times. For simplicity of operation, you can use the CLK1X as an event, if desired. For example, write the Address and data to the ADD and DATA buses, then while holding those values, on subsequent clocks, strobe the N_CS and N_WR lines.

READ CYCLE: Figure 4. Apply valid address, 0-15 (hex) to address bus lines ADD0-ADD4. Data will be output to the REG_DATA Bus, REG_DATA_0 - REG_DATA_11 on the high to low transition of N_CS, and will remain valid until N_CS is taken high again. Note diagram shows setting N_WR signal high only while N_CS is high.

WRITE CYCLE: Figure 4. Apply valid address, 0-15(hex) to address bus lines ADD0-ADD4, and valid data (12 bits) to the REG_DATA bus, REG_DATA_0 - REG_DATA_11. Note diagram shows setting N_WR signal low only while N_CS is high.

Minimum tsu – 5ns, Minimum tcs – 5ns, minimum th – 10ns. The maximum time for these signals is that the summation of all three must be less than one frame time.

Figure 3.

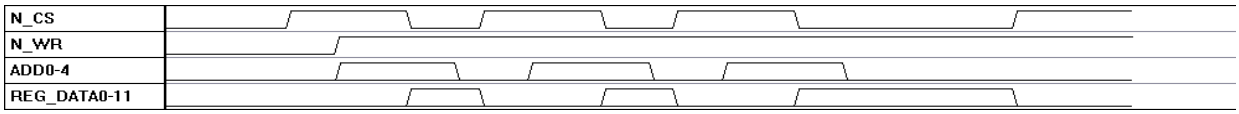
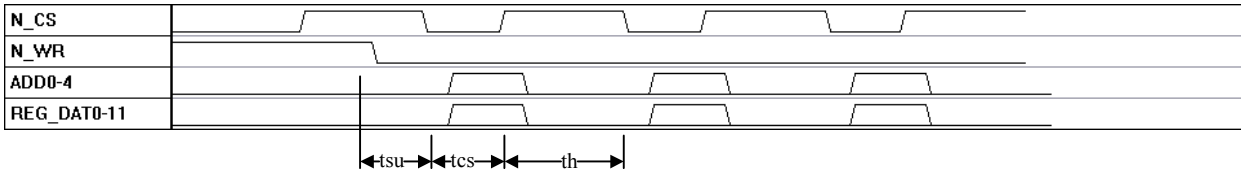
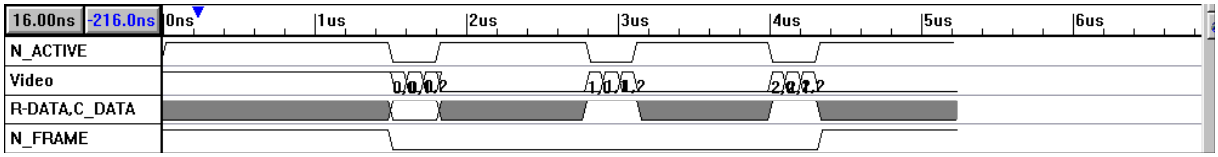


Figure 4.



FRAME TIMING DIAGRAM

Figure 5 shows video output for a 3 by 3 ROI, again with a 40MHz CLK2X.



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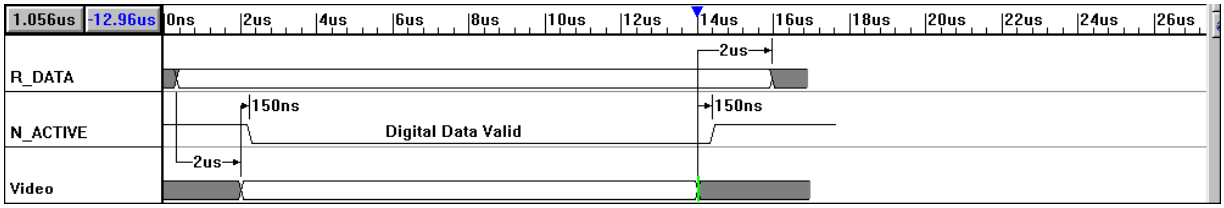
REGION OF INTEREST READOUT: Regions of Interest are read out in the order that they are programmed. Once a row stop value of zero is encountered, readout ends. The only delay between readouts is the regular retrace.

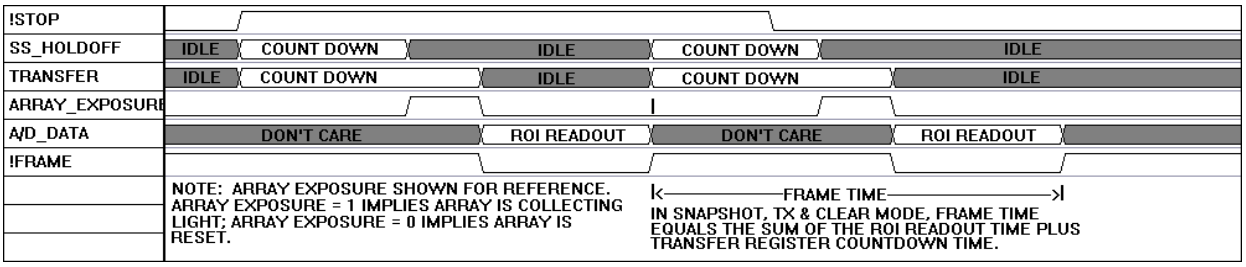
Figure 6 shows row timing



TIMING DIAGRAMS FOR MODES OF OPERATION (MASTER MODE)

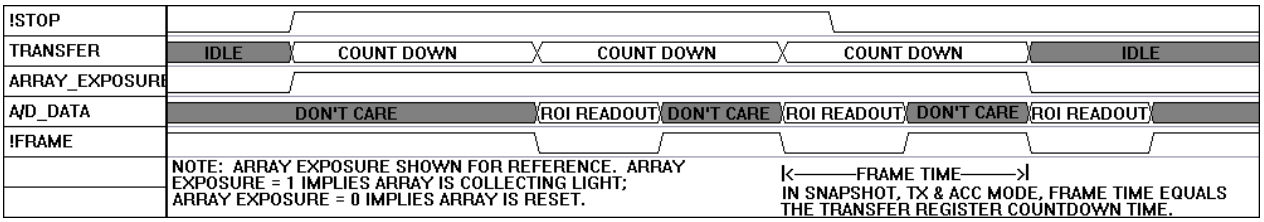
SNAPSHOT SHUTTER, DESTRUCTIVE:

Figure 7, The Snapshot and Transfer shutters begin the count down together at the start of every cycle. Pixels are reset when snapshot is zero and transferred to hold when transfer is zero, immediately reading the data. Cycles cannot be interrupted by the !stop bit.



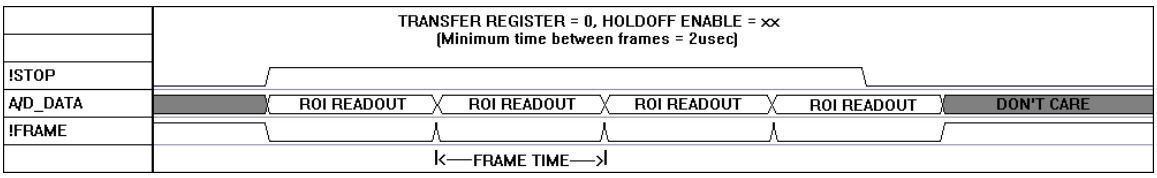
SNAPSHOT SHUTTER, NON-DESTRUCTIVE:

Figure 8 Readouts occur immediately after the transfer countdown reaches zero. The hold sites are not reset, allowing for non-destructive readout. The array will continue to transfer charge to the hold site and increase the brightness of the image. This can be sampled anytime.



ROLLING SHUTTER, DESTRUCTIVE:

In figure 9, transfer is equal to zero. The frame time is the time it takes the read a region, and each read takes place immediately after the last one. Rolling hold-off would reduce integration time, but have no effect on frame time. In the second case, where transfer is not zero, each read would not occur until the transfer countdown reached zero, extending the integration time.



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ADAPTIVE EXPOSURE FOLLOWED BY SNAPSHOT DESTRUCTIVE:

In figure 10, the ACS acquires 3 frames in non-destructive adaptive exposure followed by a final frame of destructive readout. This sequence is the preferred method of performing adaptive exposure control. During the 3 frames the user may be reading the video simultaneous to integration, when sufficient signal is present change CDS mode to readout.

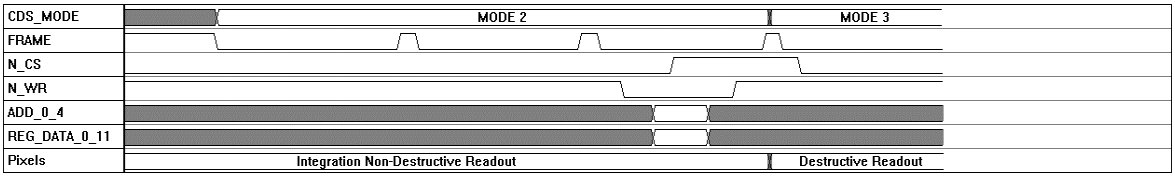


Figure 11 shows the start of row overhead in MASTER mode

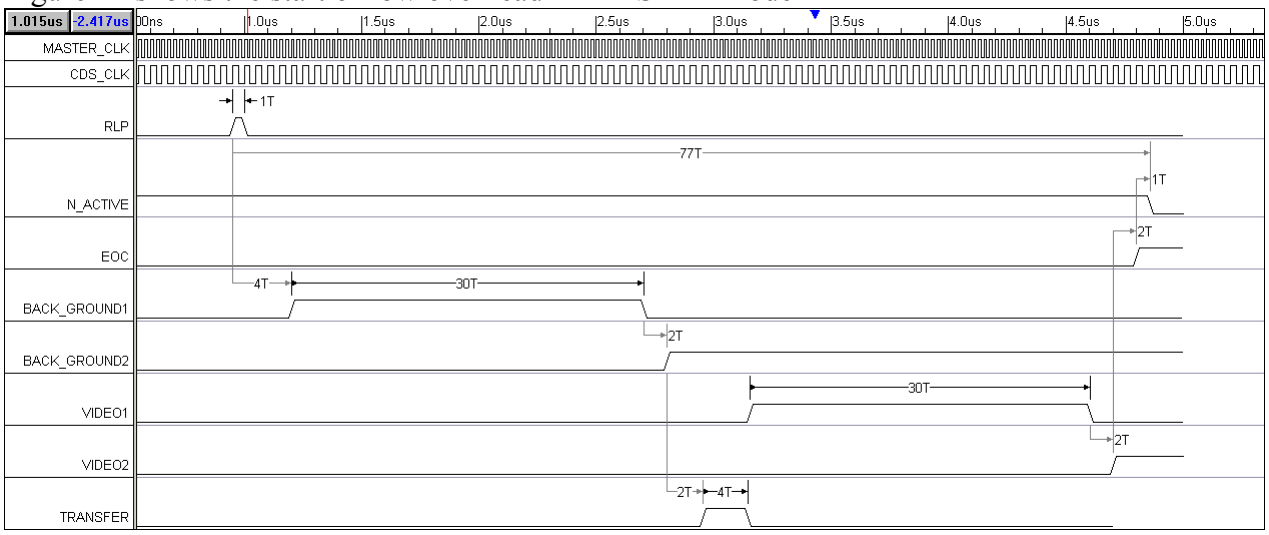
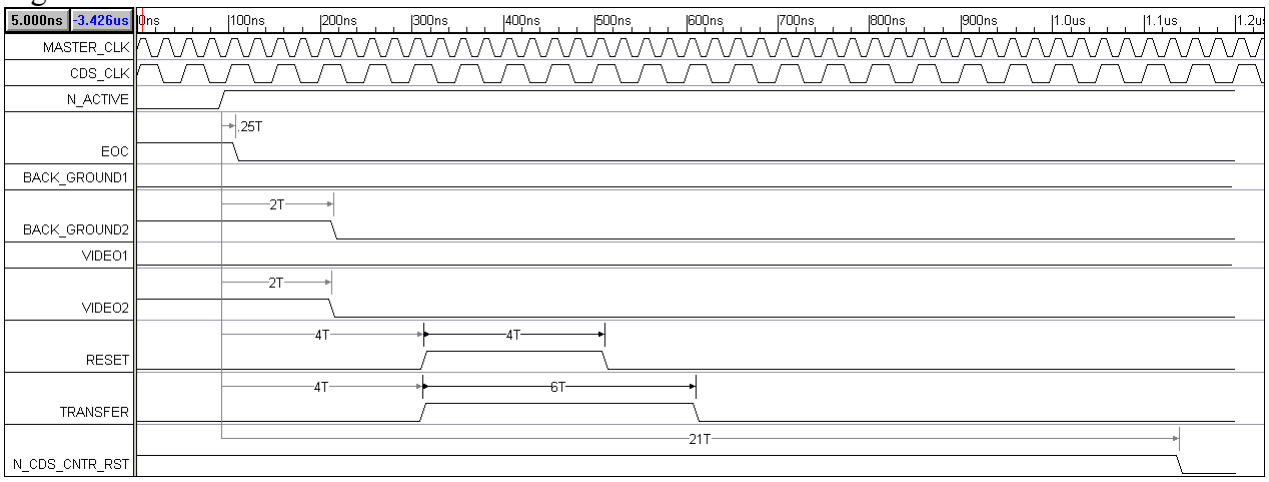


Figure 12 indicates end of row overhead in MASTER mode



The 2 above figures can be used to calculate frame and integration time.

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SLAVE MODE OPERATION:
Figure 13 shows an example of slave mode operation for QCDS, rolling shutter. Note: timing will differ slightly in MASTER mode as apposed to SLAVE mode.

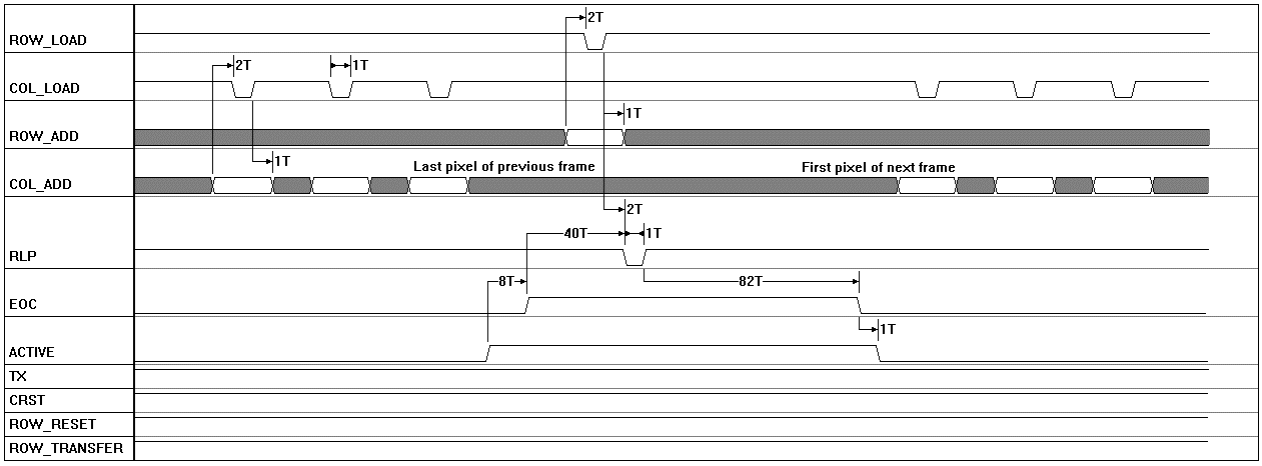
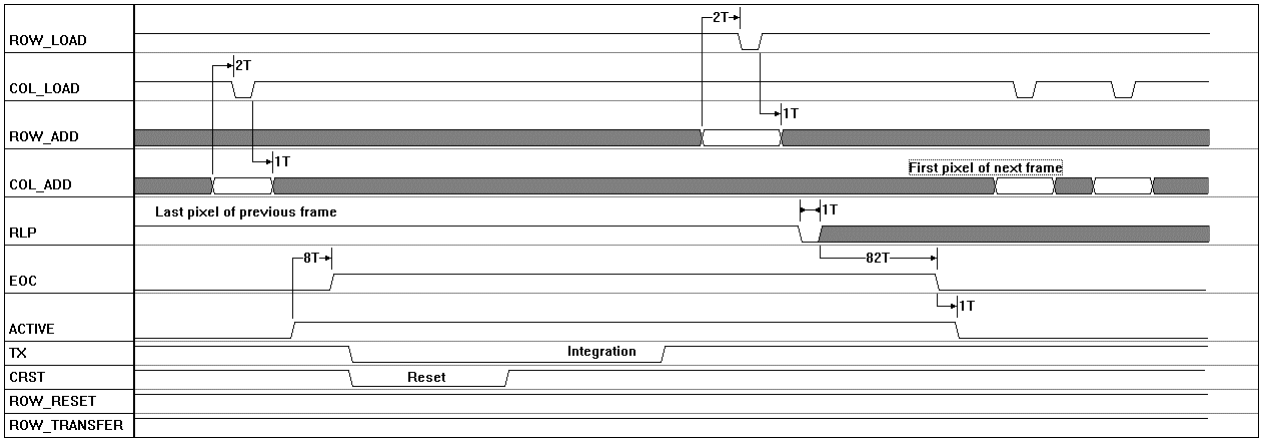


Figure 14 demonstrate the use of the TX and CRST signals to vary reset and integration time



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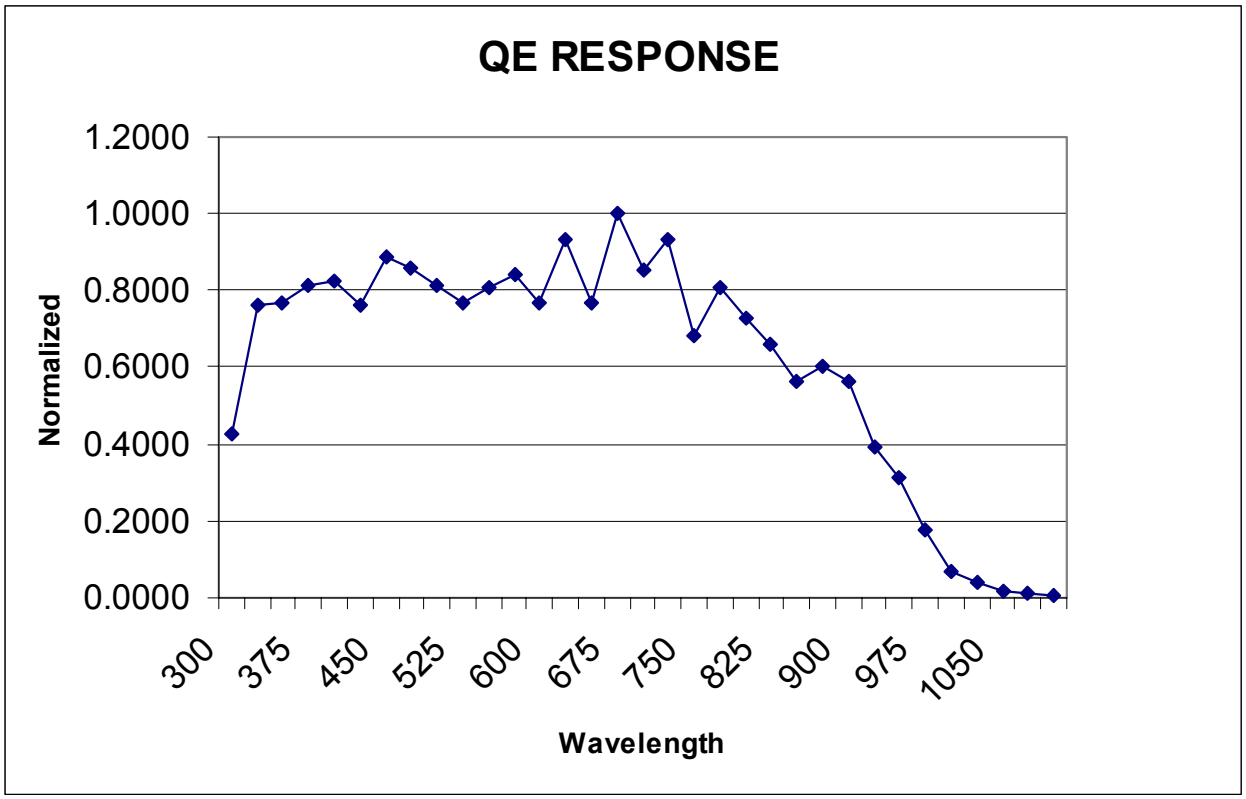

Normalized QE Response, monochrome image senor, no filter or cover glass.

ORDERING INFORMATION

DEVICE PACKAGING OPTIONS:

The device is available in 2 packaging options:

144 pin CPGA P/N ACS-1024-PG
132 pin LCC P/N ACS-1024-LG

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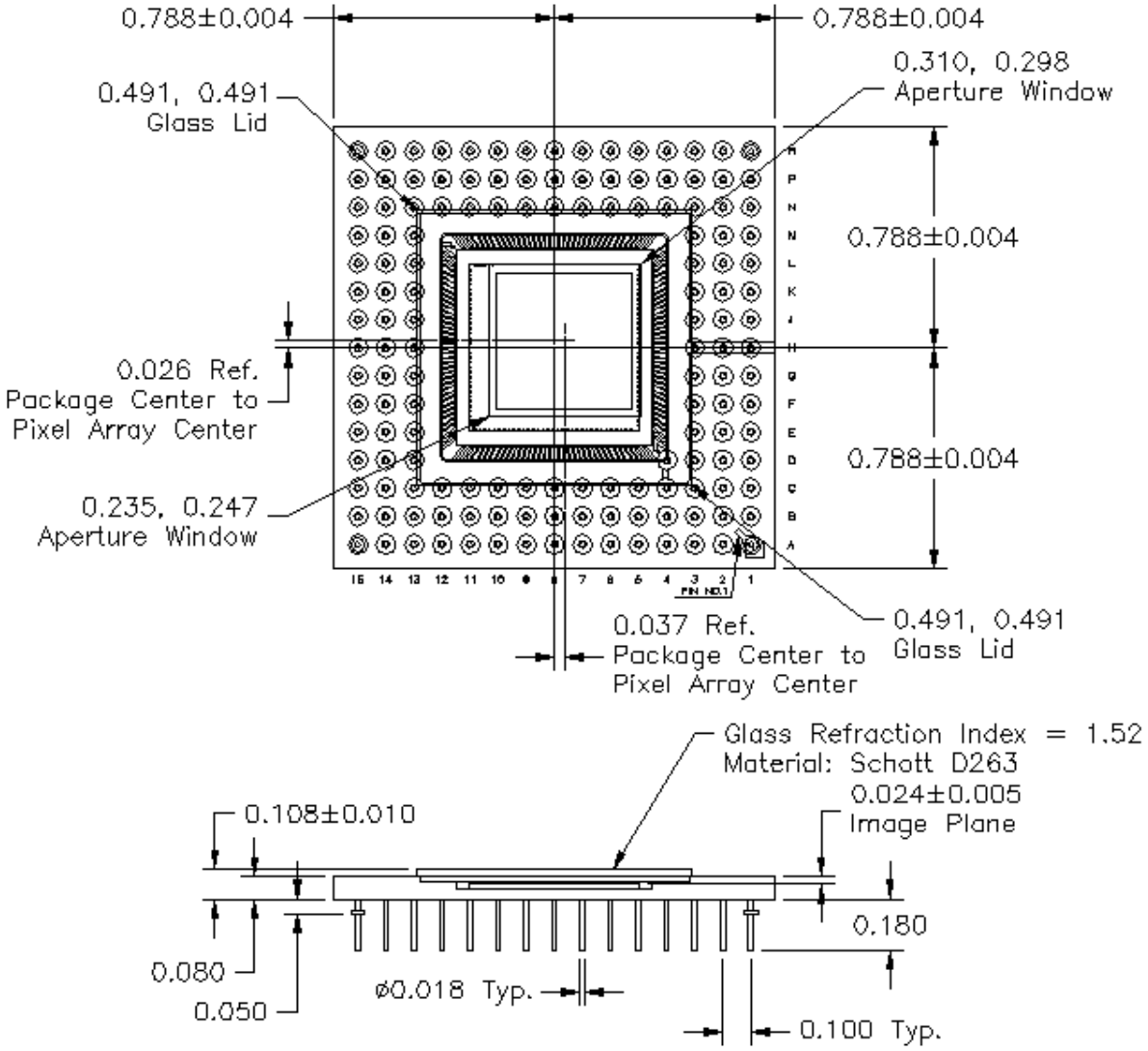
144 pin CPGA



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ACS-1024-CPGA Package pin-out table

DIE PAD	NAME	PGA BOND PAD	PGA PIN	DIE PAD	NAME	PGA BOND PAD	PGA PIN	DIE PAD	NAME	PGA BOND PAD	PGA PIN
1	REG_DATA_5	1	D3	43	C0	76	M14	85	CLK1X	121	C9
2	REG_DATA_6	2	C2	44	R1	77	L13	86	N_ACTIVE	122	A10
3	REG_DATA_7	3	B1	45	R0	78	N15	87	N_FRAME	123	A9
4	REG_DATA_8	4	D2	46	CRST	79	L14	88	DIG_PAD_PWR	124	B8
5	REG_DATA_9	5	E3	47	RESET	80	M15	89	DIG_PAD_GND	125	A8
6	REG_DATA_10	6	C1	48	PAUSE	81	K13	90	DIG_DATA_ENA	126	C8
7	REG_DATA_11	7	E2	49	MASTER	82	K14	91	DATA_0_LSB	127	C7
8	DIG_PAD_PWR	8	D1	50	GAIN1	83	L15	92	DATA_1	128	A7
9	DIG_PAD_GND	9	F3	51	GAIN0	84	J14	93	DATA_2	129	A6
10	C_DATA_0	10	F2	52	OFFSET1	85	J13	94	DATA_3	130	B7
11	C_DATA_1	11	E1	53	OFFSET0	86	K15	95	DATA_4	131	B6
12	C_DATA_2	12	G2	54	DIG_PAD_GND	87	J15	96	DATA_5	132	C6
13	C_DATA_3	13	G3	55	DIG_PAD_PWR	88	H14	97	DATA_6	133	A5
14	C_DATA_4	14	F1	56	N_CS	89	H15	98	DATA_7	134	B5
15	C_DATA_5	15	G1	57	N_WR	90	H13	99	DATA_8	135	A4
16	C_DATA_6	16	H2	58	SYNC	91	G13	100	DATA_9	136	A3
17	C_DATA_7	17	H1	59	TX	92	G15	101	REG_DATA_0	137	B4
18	C_DATA_8	18	H3	60	COL_LOAD	93	F15	102	REG_DATA_1	138	C5
19	C_DATA_9	19	J3	61	ROW_LOAD	94	G14	103	REG_DATA_2	139	B3
20	C_DATA_10	20	J1	62	GB_ANA_GND	95	F14	104	REG_DATA_3	140	A2
21	C_DATA_11	21	K1	63	ANA_GND2	96	F13	105	REG_DATA_4	141	C4
22	R_DATA_0	22	J2	64	ANA_GND1	97	E15				
23	R_DATA_1	23	K2	65	ANA_PAD_GND	98	E14				
24	R_DATA_2	24	K3	66	GB_ANA_PWR	99	D15				
25	R_DATA_3	25	L1	67	ANA_PAD_PWR	100	C15				
26	R_DATA_4	26	L2	68	PIX_AMP_ANA_PWR	101	D14				
27	R_DATA_5	27	M1	69	ANA_PWR1	102	E13				
28	R_DATA_6	28	N1	70	ANA_PWR2	103	C14				
29	R_DATA_7	29	M2	71	ANALOG_OUT	104	B15				
30	R_DATA_8	30	L3	72	BIAS_PD_EXT	105	D13				
31	R_DATA_9	31	N2	73	ANALOG_IN	109	C12				
32	R_DATA_10	32	P1	74	DIG_PAD_PWR	110	B13				
33	R_DATA_11	33	M3	75	DIG_PWR	111	A14				
34	ROW RESET	67	P13	76	DIG_GB_PWR	112	B12				
35	ROW TRANSFER	68	R14	77	DIG_PAD_GND	113	C11				
36	EOC OUT	69	N12	78	DIG_GND	114	A13				
37	ACTIVE IN	70	N13	79	ADD0	115	B11				
38	RLP IN	71	P14	80	ADD1	116	A12				
39	EXT ANA SEL	72	R15	81	ADD2	117	C10				
40	CDS1	73	M13	82	ADD3	118	B10				
41	CDS0	74	N14	83	ADD4	119	A11				
42	C1	75	P15	84	CLK_IN_2X	120	B9				

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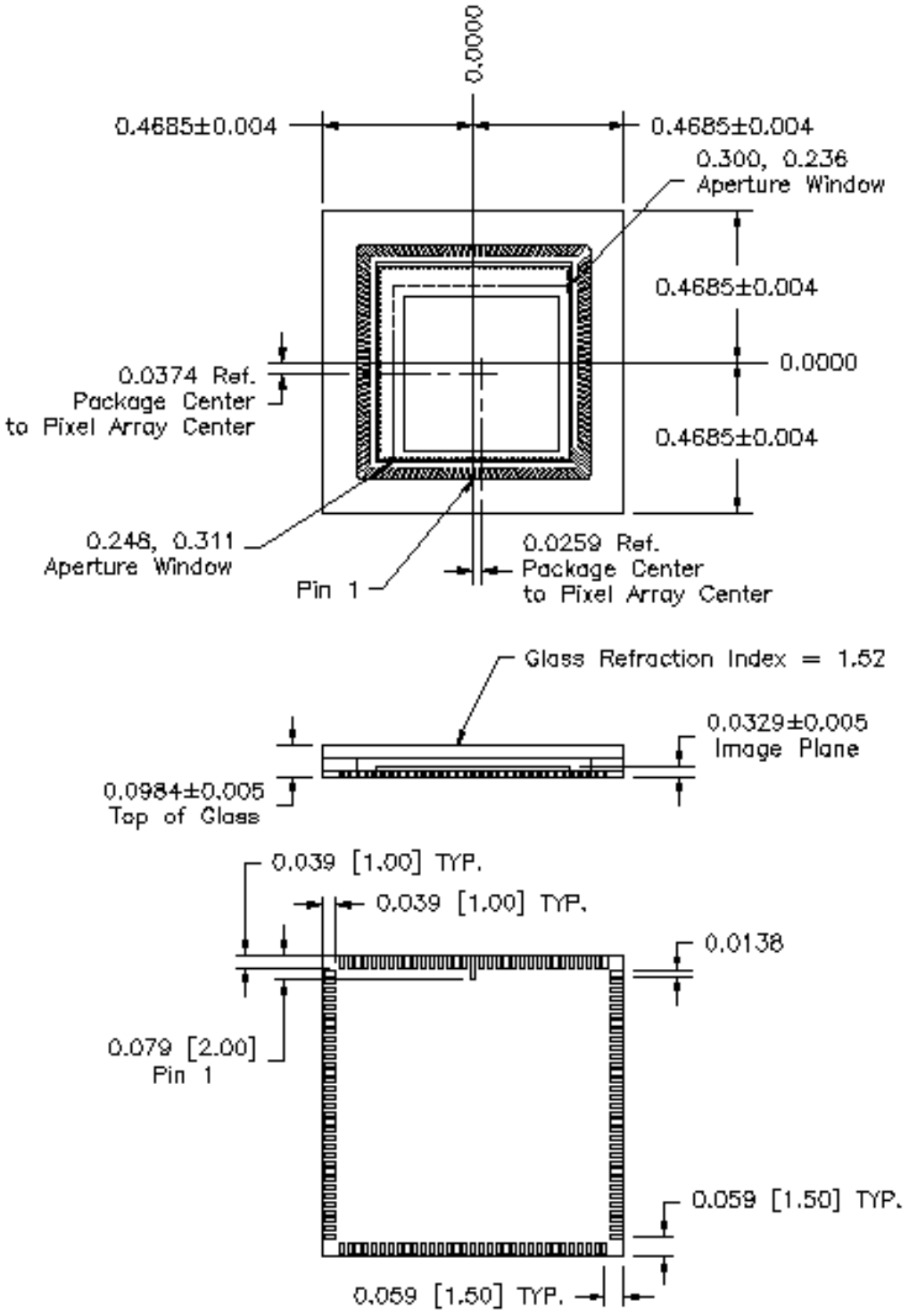
132 pin LCC



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ACS-1024-LCC Package pin-out table

POLY PAD	NAME	DIE PAD	POLY PAD	NAME	DIE PAD	POLY PAD	NAME	DIE PAD
1	C_DATA_7	17	49	EXT ANA SEL	39	97	N_ACTIVE	86
2	C_DATA_8	18	No Pad			98	N_FRAME	87
3	C_DATA_9	19	51	CDS1	40	99	DIG_PAD_PWR	88
4	C_DATA_10	20	52	CDS0	41	100	DIG_PAD_GND	89
5	C_DATA_11	21	53	C1	42	101	DIG_DATA_ENA	90
6	R_DATA_0	22	54	C0	43	102	DATA_0_LSB	91
7	R_DATA_1	23	55	R1	44	103	DATA_1	92
8	R_DATA_2	24	56	R0	45	104	DATA_2	93
9	R_DATA_3	25	57	CRST	46	105	DATA_3	94
10	R_DATA_4	26	58	RESET	47	106	DATA_4	95
11	R_DATA_5	27	59	PAUSE	48	107	DATA_5	96
12	R_DATA_6	28	60	MASTER	49	108	DATA_6	97
13	R_DATA_7	29	61	GAIN1	50	109	DATA_7	98
14	R_DATA_8	30	62	GAIN0	51	110	DATA_8	99
15	R_DATA_9	31	63	OFFSET1	52	111	DATA_9	100
16	R_DATA_10	32	64	OFFSET0	53	112	REG_DATA_0	101
17	R_DATA_11	33	65	DIG_PAD_GND	54	113	REG_DATA_1	102
18	SG		66	DIG_PAD_PWR	55	114	REG_DATA_2	103
19	SG		67	N_CS	56	115	REG_DATA_3	104
20	NC		68	N_WR	57	116	REG_DATA_4	105
21	NC		69	SYNC	58	117	REG_DATA_5	1
22	NC		70	TX	59	118	REG_DATA_6	2
23	NC		71	COL_LOAD	60	119	REG_DATA_7	3
24	NC		72	ROW_LOAD	61	120	REG_DATA_8	4
25	NC		73	GB_ANA_GND	62	121	REG_DATA_9	5
26	NC		74	ANA_GND2	63	122	REG_DATA_10	6
27	NC		75	ANA_GND1	64	123	REG_DATA_11	7
28	NC		76	ANA_PAD_GND	65	124	DIG_PAD_PWR	8
29	NC		77	GB_ANA_PWR	66	125	DIG_PAD_GND	9
30	NC		78	ANA_PAD_PWR	67	126	C_DATA_0	10
31	NC		79	PIX_AMP_ANA_PWR	68	127	C_DATA_1	11
32	NC		80	ANA_PWR1	69	128	C_DATA_2	12
33	NC		81	ANA_PWR2	70	129	C_DATA_3	13
34	NC		82	ANALOG_OUT	71	130	C_DATA_4	14
35	NC		83	BIAS_PD_EXT	72	131	C_DATA_5	15
36	NC		84	ANALOG_IN	73	132	C_DATA_6	16
37	NC		85	DIG_PAD_PWR	74			
38	NC		86	DIG_PWR	75			
39	NC		87	DIG_GB_PWR	76			
40	NC		88	DIG_PAD_GND	77			
41	NC		89	DIG_GND	78			
42	NC		90	ADD0	79			
43	NC		91	ADD1	80			
44	RST ROW IN	34	92	ADD2	81			
45	TRANSFER	35	93	ADD3	82			
46	EOC OUT	36	94	ADD4	83			
47	ACTIVE IN	37	95	CLK_IN_2X	84			
48	RLP IN	38	96	CLK1X	85			

NOTES:

1. SG – Substrate Ground NC – No Connection

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CHARACTERIZATION CRITERIA

Pixel Read Rate

Read rate is the frequency at which adjacent pixels can be read. Specification requires maximum operation at 5.0 MHz as a limit. Testing pixel rate at 5.0 MHz. Therefore, CLK_IN_2X will be at 10.0 MHz at 50% duty cycle.

Full Well

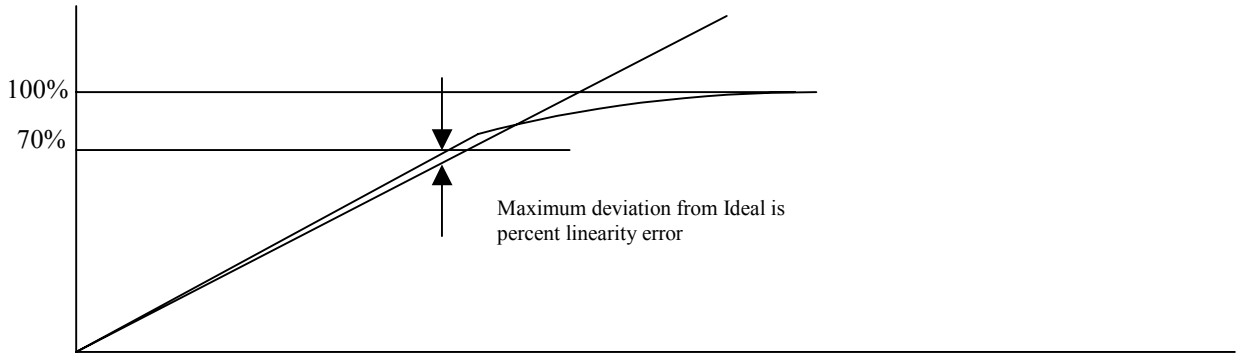
Full well (or Saturation Exposure) is the maximum number of photon and/or dark current generated electrons a pixel can hold. Full well is based on the capacitance of the pixel at a given bias. Full well is made by measuring the capacitance of all pixels for the operational bias.

Quantum Efficiency

Quantum Efficiency is a measurement of the pixel ability to capture photon generated charge at a given wavelength. This is measured at 25nm increments over the 300 to 1100 nm range. Measurements are taken using a stable light source that is filtered using a monochromator. The exiting light from the monochromator is collimated to provide a uniform flux that overfills a portion of the sensor area. The flux at a given wavelength is measured using a calibrated radiometer and then the device under test is substituted.

Linearity

Linearity is an equal corresponding output signal of the sensor for a given amount of photon incident on the pixel active area. Linearity is measured numerous ways. The most straight forward method is plotting the saturation exposure measurement from 5% to 70% of full well and applying a "best fit" straight line plot and finding the greatest deviation (error) in terms of percent of full well.



Dark Signal

Dark signal is the accumulated electrons for a given integration period, that were not photon generated. There are a few sources in CMOS circuits for the dark current and the dark current levels will vary even for a given process. Dark current will be measured at 1.0 sec. integration time at 25 degrees C.

Read Noise

Read noise is the temporal or time variant noise in the analog signal. Read noise does not include Fixed Pattern Noise (FPN) or dark current. FPN and dark current are fixed levels per pixel for a given temperature, illumination and pixel. Read noise will be measured at the output of the imager with proper loading and Bandwidth limitations. A high gain probe will be used twice. One measurement will be to measure the background noise of the test setup. The second will be to measure the video noise using the test setup. The noise of the imager will be calculated by dividing out the gain back to 1X and subtracting the test setup noise from the measured signal. Since noise sources add in quadrature, the test setup noise will be subtracted accordingly.

Image lag

Image lag is the amount of residual signal in terms of percent of full well on the current frame of video after injecting the previous frame of video. Image lag will be measured by illuminating a number of pixels (TBD) to 50% of saturation for one frame and then rereading those pixels for the next and subsequent frames without light exposure. Any remaining residual signal will be measured and recorded in terms of percent of full well.

Dynamic Range

Dynamic range is normally calculated by taking the full well value and dividing by the Root Mean Squared (rms.) of the temporal read noise. In terms of dB it is twenty times the log of the calculated value.

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Photon Vision Systems, Inc.
One Technology Place
Homer, NY 13077
Tel: +1 607-756-5200
Fax: +1 607-756-5319
www.photon-vision.com
sales@photon-vision.com

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