

SB53-C THRU SB54-C

**SURFACE MOUNT SCHOTTKY
BARRIER RECTIFIER**
VOLTAGE:30 TO 40V CURRENT: 5.0A

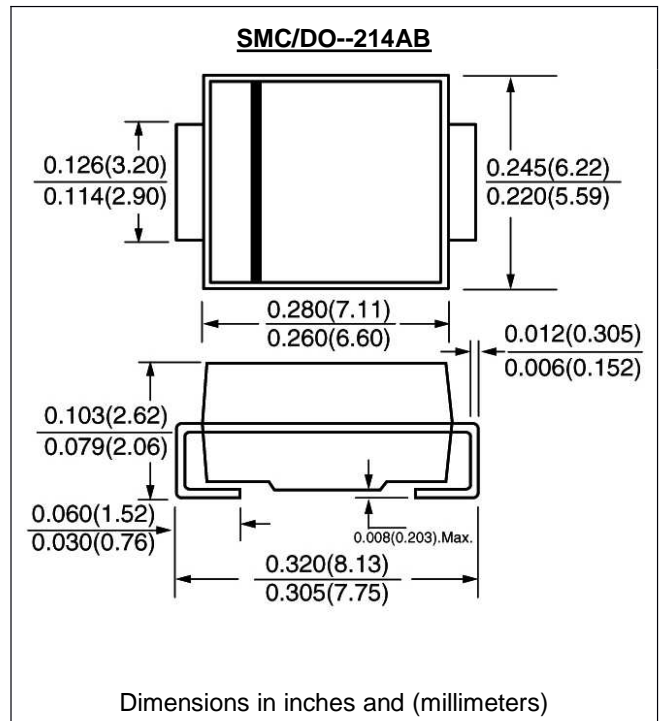


FEATURE

Plastic package has Underwriters Laboratory Flammability Classification 94V-0
For surface mounted applications
Low profile package
Built-in strain relief
Low power loss, high efficiency
High current capability, low forward voltage drop
High surge capability
For use in low voltage high frequency inverters, free wheeling, and polarity protection applications
Guarding for over voltage protection

MECHANICAL DATA

Case: JEDEC DO-214AB molded plastic body
Terminals: Solder plated, solderable per MIL-STD-750, Method 2026
High temperature soldering guaranteed:
250°C /10 seconds at terminals
Polarity: Color band denotes cathode end
Weight: 0.007 ounce, 0.25gram



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

(single-phase, half-wave, 60HZ, resistive or inductive load rating at 25°C, unless otherwise stated, for capacitive load, derate current by 20%)

	SYMBOL	SB53-C	SB54-C	units
Device marking code		SB53	SB54	
Maximum Recurrent Peak Reverse Voltage	V _{rrm}	30	40	V
Maximum RMS Voltage	V _{rms}	21	28	V
Maximum DC blocking Voltage	V _d	30	40	V
Maximum Average Forward Rectified Current 3/8" lead length at T _c (See Fig.1)	I _{f(av)}	5.0		A
Peak Forward Surge Current 8.3ms single half sine-wave superimposed on rated load	I _{fsm}	175.0		A
Maximum Forward Voltage at rated Forward current at 5.0A T _J =25°C (Note 1)	V _f	0.50		V
Maximum DC Reverse Current T _J =25°C at rated DC blocking voltage T _J =125°C	I _r	0.7	0.5	mA
		65	60	
Typical Thermal Resistance (Note 2)	R(ja)	60.0		°C /W
	R(jl)	20.0		
Storage and Operating Temperature Range	T _{stg}	-50 to +150		°C

NOTES:

- (1) Pulse test: 300µs pulse width, 1% duty cycle
- (2) Aluminum substrate mounted

Fig. 1 – Forward Current Derating Curve

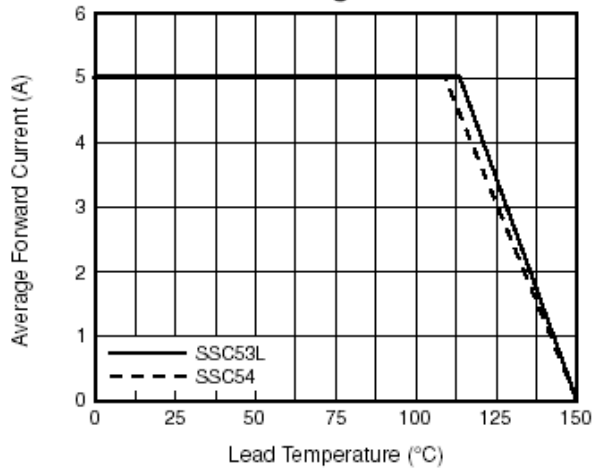


Fig. 2 – Maximum Non-Repetitive Peak Forward Surge Current

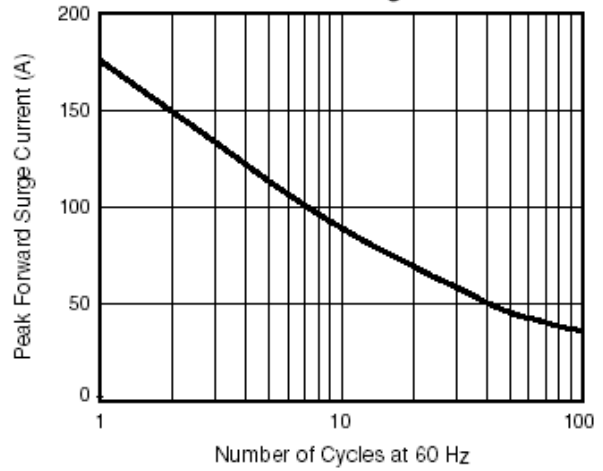


Fig. 3 – Typical Instantaneous Forward Characteristics

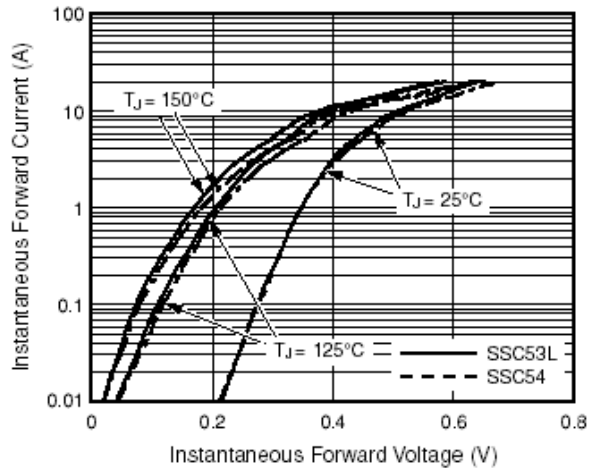


Fig. 4 – Typical Reverse Characteristics

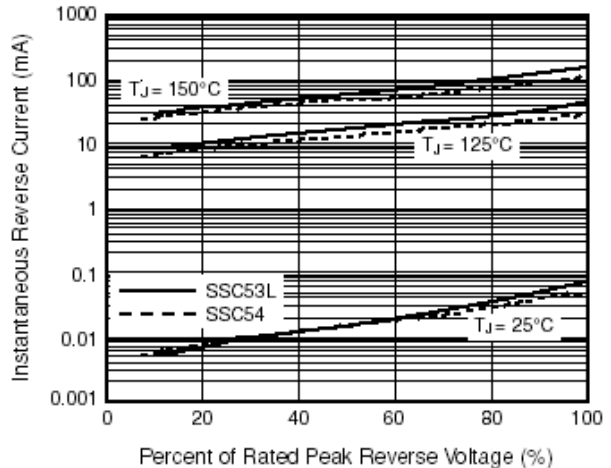


Fig. 5 – Typical Junction Capacitance

